RL-TR-97-185
Final Technical Report
October 1997

MACROMODELING ELECTROMAGNETIC EFFECTS IN CIRCUITS

CALSPAN - UB Research Center

Daniel J. Kenneally

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REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	Oct 97	Final Oct 94 - Jul 96

4. TITLE AND SUBTITLE

MACROMODELING ELECTROMAGNETIC EFFECTS IN CIRCUITS

5. FUNDING NUMBERS

C - F30602-93-D-0075/Task 19
PE - 62702F
PR - 2338
TA - 03
WU - P7

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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Buffalo, NY 14225

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Rome Laboratory/ERST
525 Brooks Rd
Rome, NY 13441-4505

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

RL-TR-97-185

11. SUPPLEMENTARY NOTES

Rome Laboratory Project Engineer: Michael F. Seifert, ERST, 315-330-4758

12a. DISTRIBUTION AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

N/A

13. ABSTRACT *(Maximum 200 words)*

This report presents results of an investigation to develop CAD macromodels for simulating and assessing electromagnetic (EM) effects in linear and digital ICs. The effects of interest are any unintended IC responses due to inadvertently (or intentionally) coupled EM energy entering into any accessible ports on the victim circuit. Assessments of possible EM effects require robust methodology to encompass a variety of coupling waveforms and conditions. In this study, both Thevenin and Norton sources were used as equivalent circuits for coupling the intrusive EM fields. Both digital and linear ICs were used as victim circuits to determine and benchmark performance of the candidate macros. Three ICs of representative families, however, were specifically selected for bench marking because they are used in current and planned Air Force Systems. In addition, other contemporary linear ICs and OpAmp's were used in various circuit configurations to demonstrate use of the (EM) assessment macromodels.

14. SUBJECT TERMS

Electromagnetic Effects , CAD, Modeling, Simulation, Electromagnetic Susceptibility

15. NUMBER OF PAGES

294

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

ACKNOWLEDGMENTS

A special thanks to the Rome Laboratory personnel of the Electronic Systems Engineering Division: Mr. Michael F. Seifert (Project Leader) and Mr. John C. Cleary (Chief, Systems Technology and Integration Branch) for their valued technical assistance and guidance; Mr. Carmen J. Luvera (Chief, Electronic Systems Engineering Division) who wisely continues to advocate electromagnetic measurements and modeling of new Air force Systems; and Mr. James Wasielewski (Manager, Expert Science and Engineering Programs Office) for his help and patience with administrative details; and, finally, Mr. Kenneth R. Siarkiewicz who generously provided the singularly appreciated and very timely use of his printer facilities as well as his assistance in using them. The CALSPAN-UB Research Center and this author, in particular, thank each of you.

DANIEL J. KENNEALLY

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ABSTRACT

This report presents results of an investigation to develop CAD macromodels for simulating and assessing electromagnetic (EM) effects in linear and digital ICs. The circuit simulator used is PSPICE*, Version 6.2. The effects of interest are any unintended IC responses due to inadvertently (or intentionally) coupled EM energy entering into any accessible ports on the victim circuit. Assessments of possible EM effects require a robust methodology to encompasses a variety of coupling waveforms and conditions.

In this study, both Thevenin and Norton sources were used as equivalent circuits for coupling the intrusive EM fields. Both digital and linear ICs were used as victim circuits to determine and benchmark performance of the candidate macros. Three ICs of representative families, however, were specifically selected for bench marking because they are used in current and planned Air Force T/R (transmit/receive) Modules. In addition, other contemporary linear ICs and OpAmp's were used in various circuit configurations to demonstrate use of the (EM) assessment macromodels.

The macromodels (macros or sub-circuits) developed here were used to "measure" or compute circuit responses at the output and at other ports when any other (as arbitrary input) ports were cw driven by EM sources. These macromodels were designed to measure average power, peak power, scattering parameters, digital eye patterns, bit error thresholds, noise figure, and other device performance metrics related to the resulting electromagnetic degradation. Demonstrations using a PSPICE simulator and selected ICs, under a variety of coupling scenarios, suggest good evidence that macromodels developed in this program, in fact, perform as intended. The shortfall, if any, in these demonstrations is that they were limited in frequency range due to time constraints. While the macromodels presented in this report were tailored for the PSPICE Version 6.2 circuit simulator, it is felt that they are general enough in format and application to be easily adapted into most any other

* PSPICE is a registered trademark of the MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718.

contemporary circuit simulator.

From our performance data on EM assessment macros developed and demonstrated in this program, we conclude that macromodels in PSPICE can provide sub-circuits, analog behavioral models, and algorithms that enable assessments of EM related effects in ICs. Among these are EM effects related macros that can:

a) combine desired signal power with EM coupled power,

b) compute or "measure" average, rms, and peak power levels,

c) generate tailored noise spectra,

d) compute or "measure" noise spectral densities and noise figures,

e) generate eye patterns to determine upset thresholds,

f) compute or "measure" S-parameters of passive and active devices, and

g) compute or "measure" input impedance, VSWR, insertion loss, and gain.

It is recommended that Rome Laboratory continue this and related work to focus on the following (EM) macromodeling initiatives:

a) widen the current frequency range at least up to 6 GHz,

b) develop and verify "realistic" EM field coupling models,

c) include IC gain compression and expansion (EM)effects,

d) refine and exploit eye patterns as EM diagnostic tools,

e) develop noise modeling as an EM effects diagnostic tool,

f) include an electrostatic discharge model in the suite of EM assessment tools,

g) investigate "packaging" the macros into a software suite of EM assessment tools,

h) investigate and select appropriate macros as candidates for technology transfer.

Details for these conclusions and related rationale for our recommendations are found elsewhere in section 10.

PROGRAM OBJECTIVES

Subcontract C/UB-1756A between the CALSPAN-University of Buffalo Research Center (CUBRC) and Mr. Daniel J. Kenneally, an independent consultant, began on October 26, 1994 and ended on July 26, 1996. The objectives of this 1140 hours effort were to assist and to advance several CAD modeling efforts on-going at the Rome Laboratory; specifically to "...to develop and verify techniques needed to enhance electromagnetic (EM) effects' circuit modeling and simulation, ...related methodologies to determine and to quantify EM susceptibility and attendant reliability effects of electronic circuits and systems will also be developed."

The task reported here entitled "Macromodeling Electromagnetic Effects in Circuits" is one of the two tasks in the CUBRC prime contract effort - "EM Effects Measurements and Modeling Technology". The other partner task in this prime contract is entitled "Measurements Technology" and is reported elsewhere (see, for example, the final technical report on the measurements task submitted to the Rome Laboratory by J. Quine of CUBRC).

The objectives of the Circuit Modeling Technology task are to develop CAD related, circuit modeling techniques needed to evaluate EM effects on electronic systems' operability and reliability. Specifically, this task will develop the necessary CAD techniques and related algorithms (in the form of circuit macromodels) which are needed to enhance EM effects' modeling and simulation of digital and linear IC's which operate in stressful EM environments. This task will also develop and demonstrate the methodologies needed to model, determine and assess EM effects' susceptibility and reliability impacts on victim electronic systems and circuits.

In addition to the Air force requirements and objectives stated above, and with the assistance and concurrence of our Rome Laboratory sponsor, we further refined the above objectives to focus on and address the following specific subtasks:

1. Develop and implement EM assessment metrics in PSPICE models.

2. Develop and implement EM sources and attendant coupling ports as Thevenin and Norton equivalents.
3. Parametize EM sources and attendant coupling topologies to determine EM driven, upset threshold sensitivities.
4. Develop PSPICE macromodels and attendant methodology to accomplish performance assessments of victim IC's due to EM waveforms at any device port.
5. Demonstrate use of candidate assessment macromodels in various EM coupling scenarios.
6. Verify macromodels' performance and predictions with measured or simulated test data for selected IC devices.

The results of both of these measurements and modeling tasks will assist Rome Laboratory's on-going programs to identify, measure, and model electromagnetic environmental effects that can degrade functional performance and reliability of Air Force electronic systems and circuits: and further, these results will help to identify, implement, test, and verify appropriate design fixes where needed.

SUMMARY AND CONCLUSIONS

Measuring and modeling electromagnetic effects on USAF electronic systems' reliability are current initiatives in the Electromagnetic Systems Engineering Division (ERS) of the Rome Laboratory. This work includes electromagnetic measurements and computer-aided modeling of system and circuit susceptibilities to the EM environmental effects on both functional and susceptibility performance. In this context, degraded functional performance and reliability effects are caused by the unintended coupling of electromagnetic fields and signals from the EM environment directly through intended (and unintended) apertures and antennas on operating systems, by coupling onto intrasystem cabling, and subsequently, by coupling into the ports of victim circuits and devices. In either case, the resulting effects are distorted waveforms, digital upsets and latch-ups, raised noise floors, bit errors, instability, and other related performance degradation.

Metrics for circuit assessments of these EM effects include several likely measures. Computational metrics tailored to EM assessments require developing, adapting or redesigning time domain PSPICE macromodels (or algorithms) in order to compute and track responses of interest. For example, we need PSPICE macros in PROBE format that can determine:

a) RMS power and energy at selected ports and nodes;

b) Input impedances looking towards load or generator;

c) Power gain referred to some source or node pair;

d) Insertion Loss between selected ports or node pairs;

f) Harmonic distortion;

g) S-parameters from time domain waveform data;

h) VSWR at selected ports;

i) Noise generators and noise figure;

j) Eye Pattern generators to threshold bit errors rates;

k) Signal power combiners.

Macromodels that enhance CAD assessments of EM effects were developed and tested. Thevenin and Norton source configurations were used as equivalent circuits to model coupling of intrusive EM fields into victim device ports. Both digital and linear ICs were used as victims to benchmark performance of the candidate macros. Three ICs of representative families, however, were specifically selected for bench marking because they are used in current and planned Air Force T/R Modules. In addition, other contemporary linear ICs and OpAmp's were used in various circuit configurations to demonstrate use of (EM) assessment macromodels developed here.

These macromodels (i.e., macros or sub-circuits) were used to simulate and "measure" circuit responses at output and other ports when any other (arbitrary) ports were cw driven by EM sources. Specific macros were designed that measure average power, peak power, scattering parameters, digital eye patterns, digital bit error thresholds, noise figure, and other metrics of EM induced degradation. Demonstrations of these macros using the PSPICE simulator and selected ICs, under a variety of EM fields coupling scenarios, suggest convincing evidence that macromodels developed in this program perform as intended. A shortfall in these demonstrations is that they were limited in frequency range due to program time constraints. While the macromodels presented in this report were tailored for a PSPICE (Version 6.2) circuit simulator, it is felt that they are general enough in format and in application to be easily adapted to most other contemporary simulators.

From our performance data on these EM assessment macros, we conclude that these EM macromodels in PSPICE provide useful sub-circuits, analog behavioral models, and related algorithms to enable assessments of EM environmental effects in ICs. Among these are macros that can:

a) combine desired signal power with EM coupled power,

b) measure average, rms, and peak power levels,

c) simulate and shape noise spectra,

d) measure noise spectral densities and noise figure,

e) generate eye patterns to determine digital thresholds,

f) measure S-parameters of passive and active devices, and

g) measure input impedance, VSWR, insertion loss, and gain.

Of special interest to Rome Laboratory and its technology transfer initiatives is our invention disclosure based on the work performed under this contract. The particular invention is the design of a Wilkinson Power Combiner as described in section 8. Simulated performance of this circuit indicates that it has considerable merit for both military and commercial applications. For example; phased array, receiving and signal processing antennas used extensively by both the military and the telecommunications industry require high performance, high fidelity rf combiners. It is recommended that Rome Laboratory initiate appropriate actions to implement and exploit this invention disclosure, and to initiate technology transfer related actions.

It is recommended this or related work be continued and focus on the following macromodeling related initiatives:

a) widen the macro frequency range of interest up to 6 GHz,

b) develop and verify realistic EM field coupling models,

c) include IC gain compression and expansion (EM)effects,

d) refine and exploit eye patterns as EM diagnostic tools,

e) develop noise modeling as an EM effects diagnostic tool,

f) select and exploit macros for technology transfer.

1. INTRODUCTION

This report presents results of an investigation to develop CAD macromodels specifically tailored to simulating and assessing EM effects in linear and digital ICs. The circuit simulator used for this purpose is PSPICE, Version 6.2. Degradation effects of interest here are any unintended IC responses (in a functional design sense) that can result from extraneous, environmental EM signals which inadvertently (or intentionally as jamming) are wire or field coupled into or otherwise enter any "accessible" ports on the victim circuit. While accessible ports used in this investigation are those intentionally designed into commercial packages, they can also be any aperture, seam, slot, wire pair, or EM porous dielectric on the package which allow EM energy to effectively get into the package interior, couple onto die associated wiring busses or traces, and eventually, induce extraneous voltage and/or current sources in functional circuits where none are intended.

In this work, Thevenin and Norton sources were both used as equivalent circuits to provide the coupled sources as drivers of the intrusive EM fields. Both digital and linear ICs were used as victim circuits to benchmark performance of candidate macros developed here. Three digital ICs of representative families (and attendant data), however, were specifically selected for bench marking because they were previously tested for application in Air Force developmental T/R Modules. In addition, contemporary linear ICs and OpAmps were used in various circuit configurations to demonstrate use of the (EM) assessment macromodels developed. These circuits include noise generators, active band pass filters, UHF power amplifiers, and UHF low noise amplifiers,

The macromodels (some times called macros or sub-circuits) developed here were used to "measure" or compute circuit responses at the intended output and at other ports of the IC device when one or more of its other ports (as arbitrary "inputs") were cw driven by EM sources. The EM sources were series and parallel connected to victim ports to simulate both electric and magnetic field coupling. Macromodels were designed to measure average power, peak power, scattering

parameters, digital eye patterns, bit error thresholds, noise figure, and other device performance metrics related to electromagnetic induced degradation. Demonstrations of these macros using a PSPICE simulator and selected ICs under a variety of EM coupling scenarios, suggest good evidence that the macromodels developed in this program, in fact, perform as intended. While they were developed and tailored for the PSPICE Version 6.2 circuit simulator, it is felt that they are general enough to be easily adapted to most other contemporary simulators. All the simulation runs were performed on a Compaq Deskpro, XL 566 PC. A PC system summary is shown in figure 1-1.

This report is organized as follows. In preamble sections we present an abstract, statements of program requirements and objectives, and a summary and conclusions with recommendations for further work in this area. Section 1 is the introduction and describes what is in the report. The main results of this work are presented beginning in the section 2 on RF power meters which develops and "calibrates" a variety of macro configurations to compute average, rms, and peak powers. Next in section 3, these power macros are used extensively to determine threshold levels of EM susceptibility in advanced, low power Schottky NAND gates. Section 4 continues this threshold sensitivity analyses for DS7820 differential line receivers, as does section 5 on 74S00, quadruple 2-input positive NAND gates.

Next in section 6, we present digital eye pattern generators and indicate how they can be used to determine sensitivity of digital waveforms to EM signals. Section 7 introduces random noise sources and several related applications. Section 8 presents several new configurations of OPAMPs as combiners of desired signals with undesired EM signals. This section also presents a new application of the conventional Richardson power divider; in this case, its electrical dual - a new form of power combiner for desired and undesired signals. In section 9, we present more accurate methods and related macros to determine the S-parameters of active and passive ICs. Several circuit examples are presented which include S-parameter derived, performance.

In section 10, we present the conclusions and recommendations that seem warranted by this work. Finally, in section 11, we present a current bibliography of CAD and EM modeling related literature. Some of this material came from a formal literature search using facilities and personnel of the Rome Laboratory Technical Library. Most came from informal, on-going, ad hoc literature searches by the author and from other personal sources and contacts.

```
**********************
*  System Summary  *
**********************

Computer
     Computer Name: Compaq
          ROM BIOS: Compaq, 10/26/94
    Main Processor: Pentium, 67MHz
 Numeric Processor: (Built-In)
          Bus Type: EISA
     Video Adapter: Video Graphics Array (VGA)
      Serial Ports: 2: COM1, COM2
    Parallel Ports: 1: LPT1
     Keyboard Type: IBM Enhanced (101- or 102-key) keyboard
        Mouse Type: PS/2 Mouse, Version 8.01

Disks
Floppy Disks: 1.44M (3½"), None
  Hard Disks: 523M (SCSI)

Memory
      Windows: 40377K
          DOS: 496K
         Base: 640K
     Extended: 15360K
   Low Memory: 113K
    Swap File: Temporary (37344K)

Environment
   Windows Version: 3.10 (Win32s 1.25)
              Mode: 386 Enhanced
       DOS Version: 6.20 (Microsoft)
          Language: English (American)
           Network: No Network Installed
```

Figure 1-1 Computer System Summary

2. POWER METERS

Accurate determination of power levels at suspected ports and nodes is indispensable to performing meaningful EM susceptibility assessments. It is akin to doing accurate, repeatable measurements in the lab. Since PSPICE is a time domain simulator, power meter macros derive from observed time waveforms provided by its PROBE feature. PROBE is the graphics analyzer which processes nodal waveform data generated on all components, nets, and built-in device models of a schematic in response to tailored directives prescribed by the analyst. PROBE provides the results of the simulation as video graphics and optional printouts. It is essentially a "virtual oscilloscope" to directly view and interact with nodal response data from a simulation run, very similar to probing an electronic breadboard in the lab. PROBE features menus for easy manipulation of simulation data to tailor display plots of power levels using intrinsic arithmetic functions. In particular, the "rms" and "avg" functions compute both kinds of running averages of power over the specified range of the time axis.

The idea behind power macros in PSPICE is the computation of power from basic voltage and current response waveforms at ports of interest. In PSPICE, waveforms are peak-to-peak levels. Thus, average (sinusoidal) power is found by the product of rms voltage and rms current, or alternatively, by taking the avg of the product of the voltage and current waveforms. Of course, average power could also be expressed as 1/2 [(voltage_{pp}) x (current_{pp})]. It is important to recognize that at most ports or nodes of interest there may be significant levels of dc present in the observed waveforms. These usually come from dc bias and rectified ac sources. Filtering these dc levels is required before doing any rms or avg operations.

Waveform filtering can be done using tailored PSPICE ABMs (analog behavioral models) of high pass filters inserted directly into the schematic. Another way to remove the dc level is to use a low impedance, blocking capacitor. This may also require a large resistor (T ohm) in parallel,

providing a return path to ground and satisfying the schematic ERC (electrical rule check); i.e., every node in PSPICE must have a direct path to ground. An even simpler way is to implement dc filters is to write them as mathematical filters (macros) in PROBE. While the latter approach is favored, all three above schema were used in this work. For example, analytical filtering of the dc level from an observed PROBE waveform (i.e., its average value) needs a simple macro to compute a filtered waveform as $v(t)_{clean} = v(t) - avg[v(t)]$. PROBE does the required data processing to effect an ideal high pass filter.

Computing accurate rms and avg values of periodic waveforms is straightforward - the time range used by default is simply the waveform period. However, with non-periodic or other transient waveforms some consideration should be given to which time ranges are best, if any. PROBE will automatically use the time range of the "sweep" selected by the analyst. This may or may not be acceptable. The computed avg and rms data presented here used the minimum sweep range that contained "all" (or, at least 90 %) of the spectral energy in the waveform. While it is not rigorously justified, good engineering judgement is still the compelling factor in most cases.

Another caveat in accurately determining power levels is to be sure that the voltage and current waveforms displayed are the ones required to compute power at the port of interest. This is not a trivial concern. In some cases, there may be some ambiguity in deciding just which node belongs to which port and even, "where" is the port of interest. Unfortunately, PSPICE does not at present have an automatic node numbering feature in its schematic that is displayed on the monitor screen. In these cases, it helps to recall the definition of a port as an aperture through which EM energy can pass; for discrete component circuits, a port is simply a discrete wire pair in which current into one wire equals current out of the other wire. It may also help to redraw the schematic with an ambiguous port. In some cases, especially using device models from the simulator library, it may help to purposely omit a wire connection using the schematic editor. PSPICE will then fail the ERC and

display an error message that states which pin or node is floating. As a last resort, which some analysts may prefer from the start, there is always the option of turning on a node numbering table and viewing it on the netlist in the notepad. This is done by accessing "options" in the analysis setup menu and selecting node Y. Of course, even without the convenience of a node table, the netlist always provides node identification and is also easily accessible through the notepad. However, inspecting netlists to determine nodes does add some more steps and windows, and may inconvenient.

In processing power level data, the analyst is also reminded that while PSPICE provides a "dB" operator as part of PROBE's analog arithmetic functions, it is valid only for voltage or current waveforms. That is, dB = 20 log (whatever ratio). To compute power, one must premultiply it by a factor of (0.5). Also, when printing schematics or data plots, be sure to highlight the area you want printed. To do this, first view the entire page and then select the print area desired by placing the cursor in one corner and then dragging it to form a bounded rectangle. In the print dialogue, check the box for "print only selected area".

In the following figures, we present various configurations of power meters to illustrate the ideas. Figure 2-1 shows a power meter using E and H devices (voltage dependent, voltage sources and current dependent, voltage sources - respectively) to sample the respective voltage and current waveforms. This meter also uses high pass ABMs to filter the dc basebands. Note that the product of filtered voltage and current waveforms is implemented with a multiplier ABM, so that the output1 "voltage" is really dc filtered, time-varying power. Figure 2-2 shows response data for the previous power meter. Note the error in (c): doing an rms of the product of voltage and current is incorrect power - average power is the product of rms voltage and rms current. Figured 2-2 (b) and (h) are correct. Figures 2-3 and 2-4 show more calibrations. Figure 2-5 shows a power meter which does not use ABM filters: it uses blocking capacitors, instead. Note the R10 is set equal to 1 T ohm to satisfy ERC. Figure 2-6 show its relevant response waveforms. Figures 2-7 and 2-8 show more data.

Doing EM assessments on systems and circuits requires EM sources to be effectively wired into victim ports as both series and parallel drivers to approximate electric and magnetic coupling. It is of interest to see how the respective powers combine in those cases. Figure 2-9 shows two identical voltage sources in parallel and each having the same available power. A simple exercise using Millman's theorem will show that these combined voltage sources should deliver double their available powers to the load R3. This occurs when the load conductance is twice the source conductances. Figured 2-10 and 2-11 show the results of the parametric variation of load R3, and clearly indicate a maximum power delivered when G3 is equal to 40 mS, consistent with the power transfer theorem. Figures 2-12 thru 2-14 show the dual case - identical voltage sources in series. Now, maximum power is delivered when the R3 load resistance is twice the source resistances. Figures 2-15 and 2-16 show the same sources in series but now use a special kind of independent voltage source - a "dead" source - to measure current through its branch load. A "dead" voltage source is simply a source with a zero voltage attribute. PSPICE will still compute a response current through it, so that a dead source becomes, in effect, an ideal ammeter. This ruse only works with PSPICE independent voltage sources; an independent current source cannot have a zero ampere attribute. Figures 2-17 and 2-18 show "dead" sources can also be dc sources and function equally well as ammeters.

These power meter macros and variations will be used throughout this report. In some sections that follow where it is not apparent from the schematic how power levels were determined, they were very likely determined using tailored mathematical macros directly in PROBE, as discussed previously. In these cases, the plots should be annotated as such.

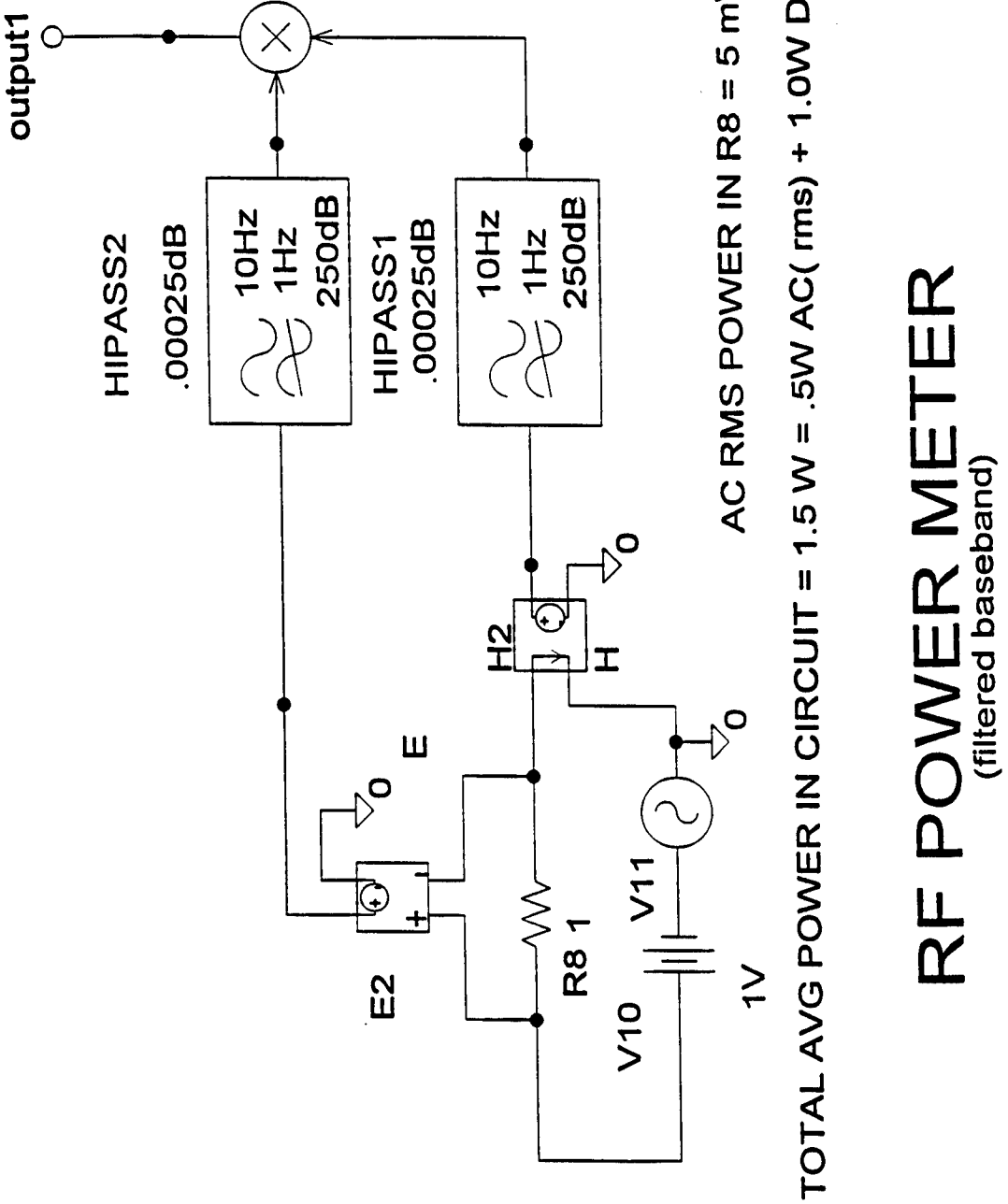


Figure 2-1 RF Power Meter with Baseband Filters

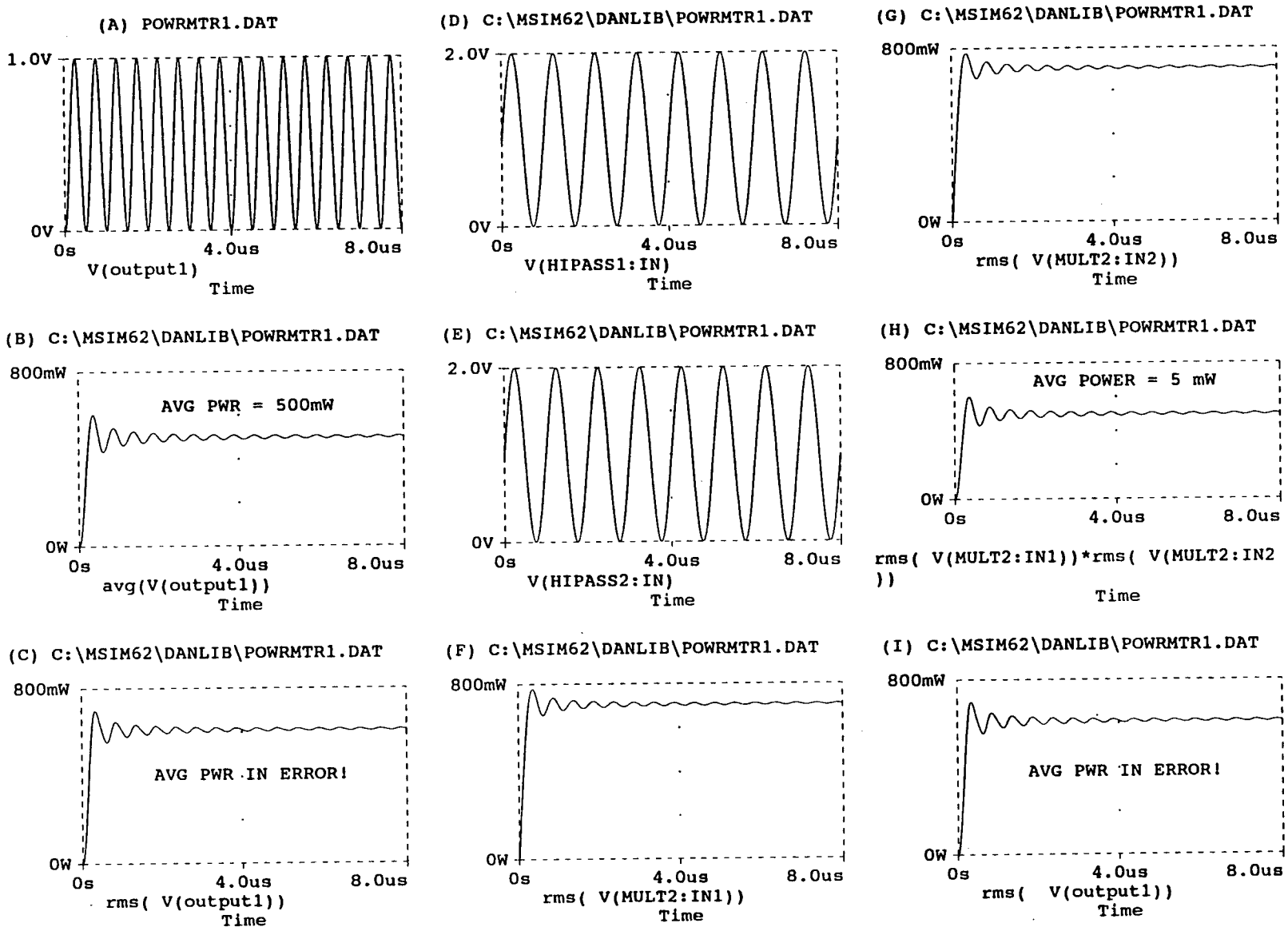


Figure 2-2 Baseband Power Meter Responses

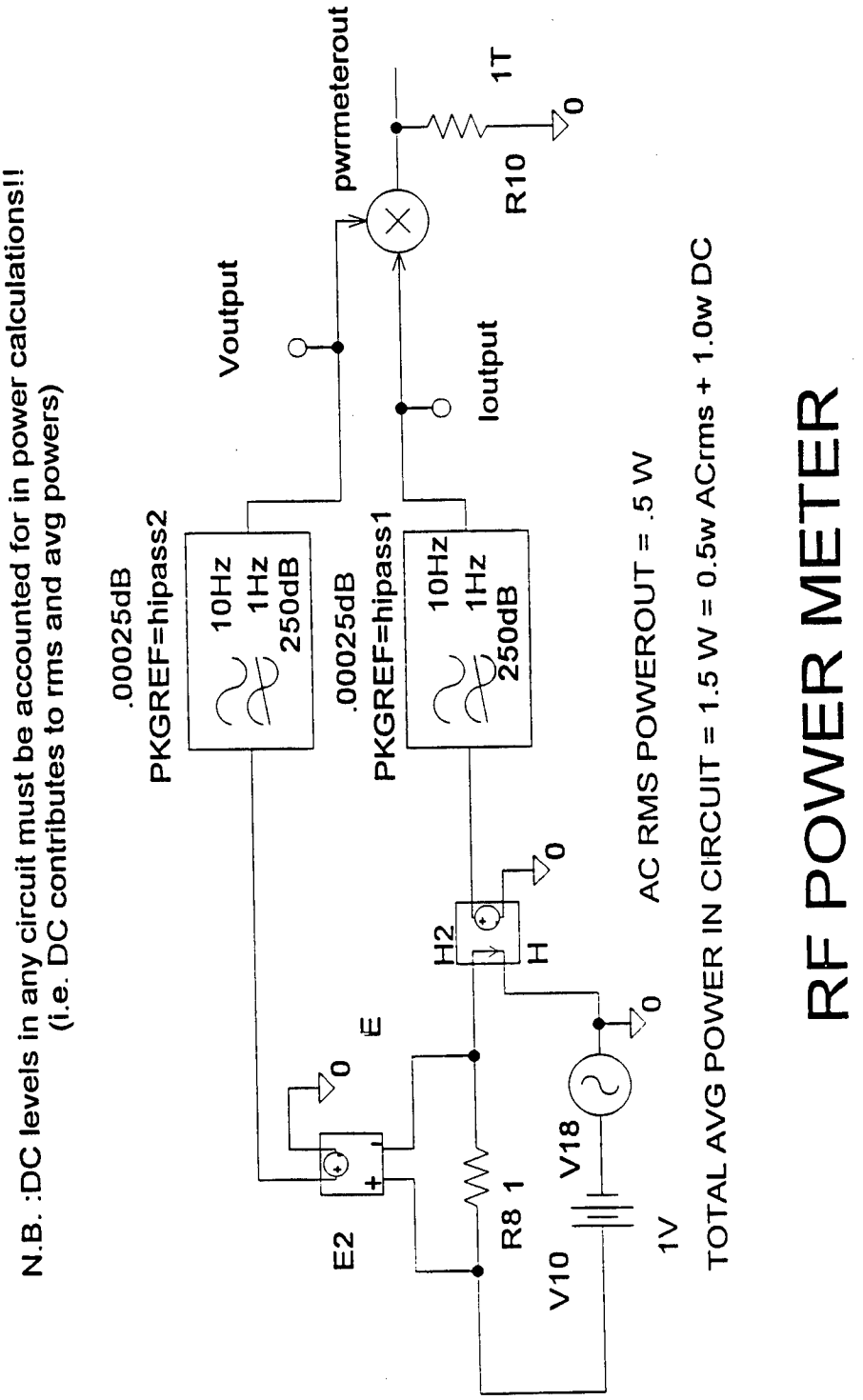


Figure 2-3 RF Power Meter for Calibrations

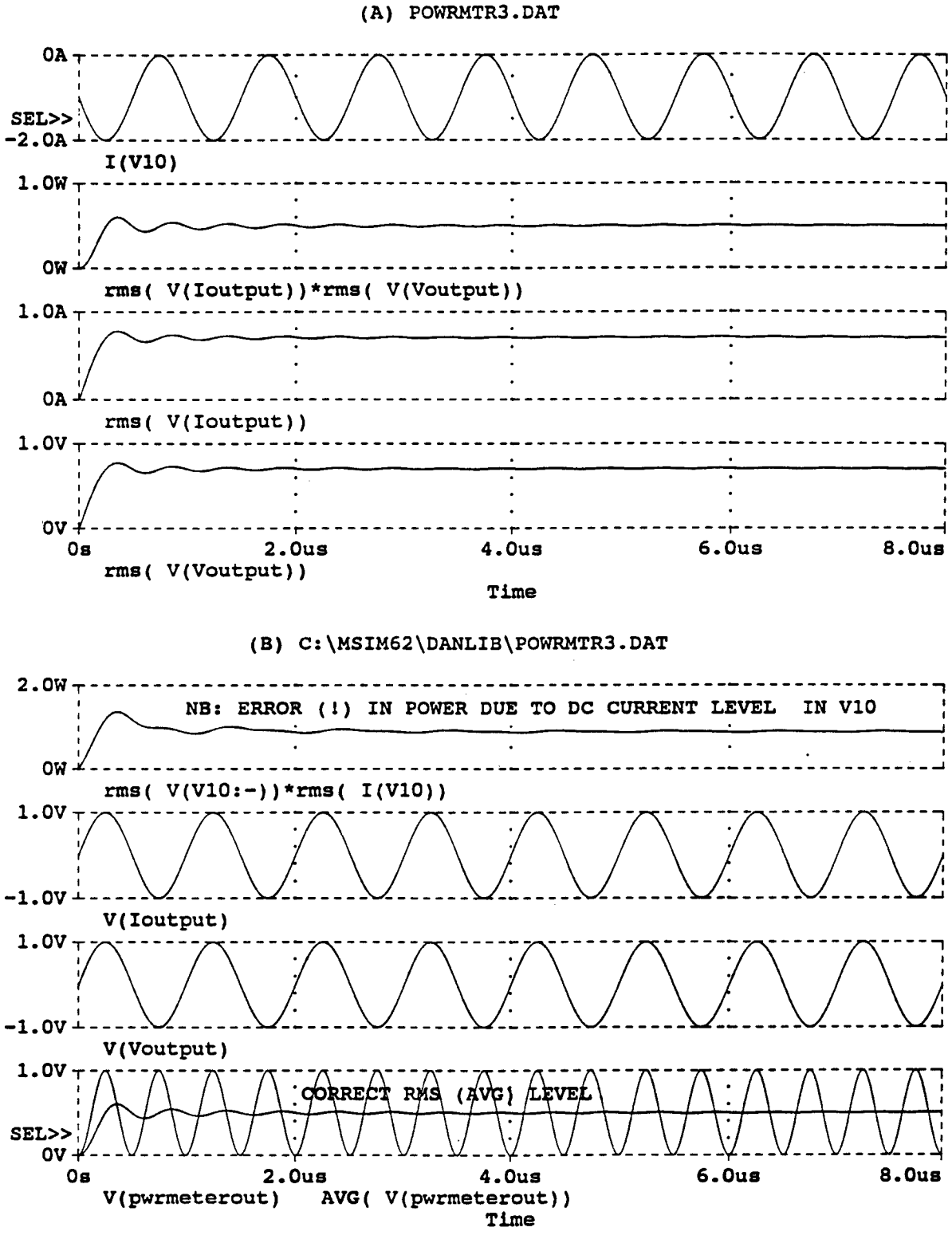


Figure 2-4 Calibration Responses

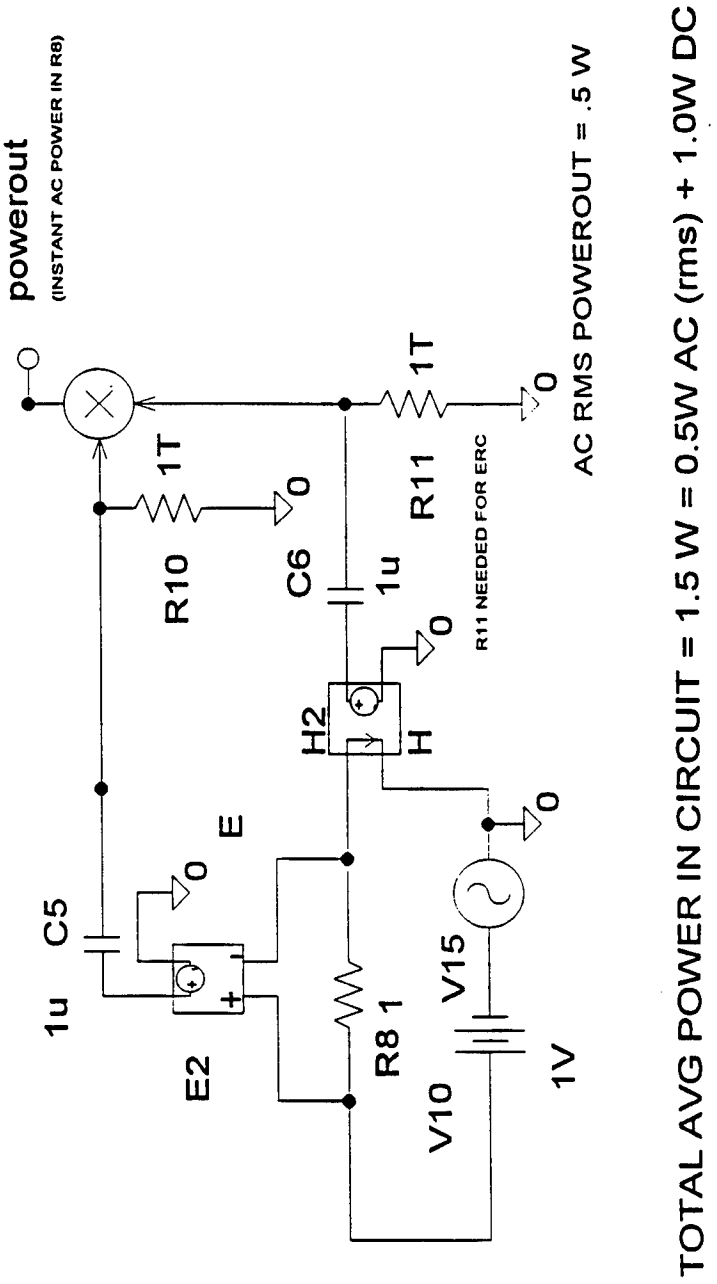


Figure 2-5 RF Power Meter with DC Blocking Capacitors

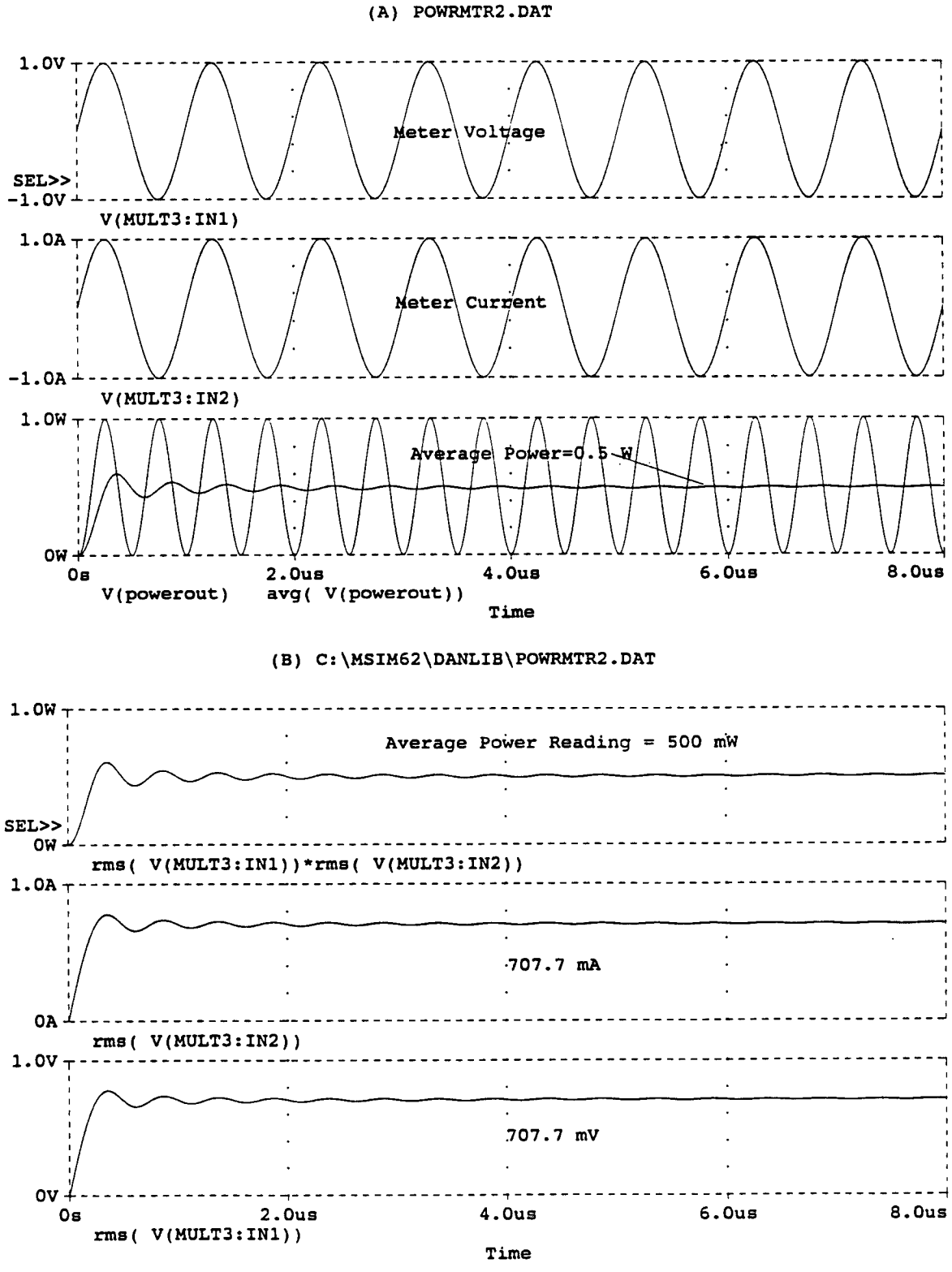


Figure 2-6 Blocking Capacitor Responses

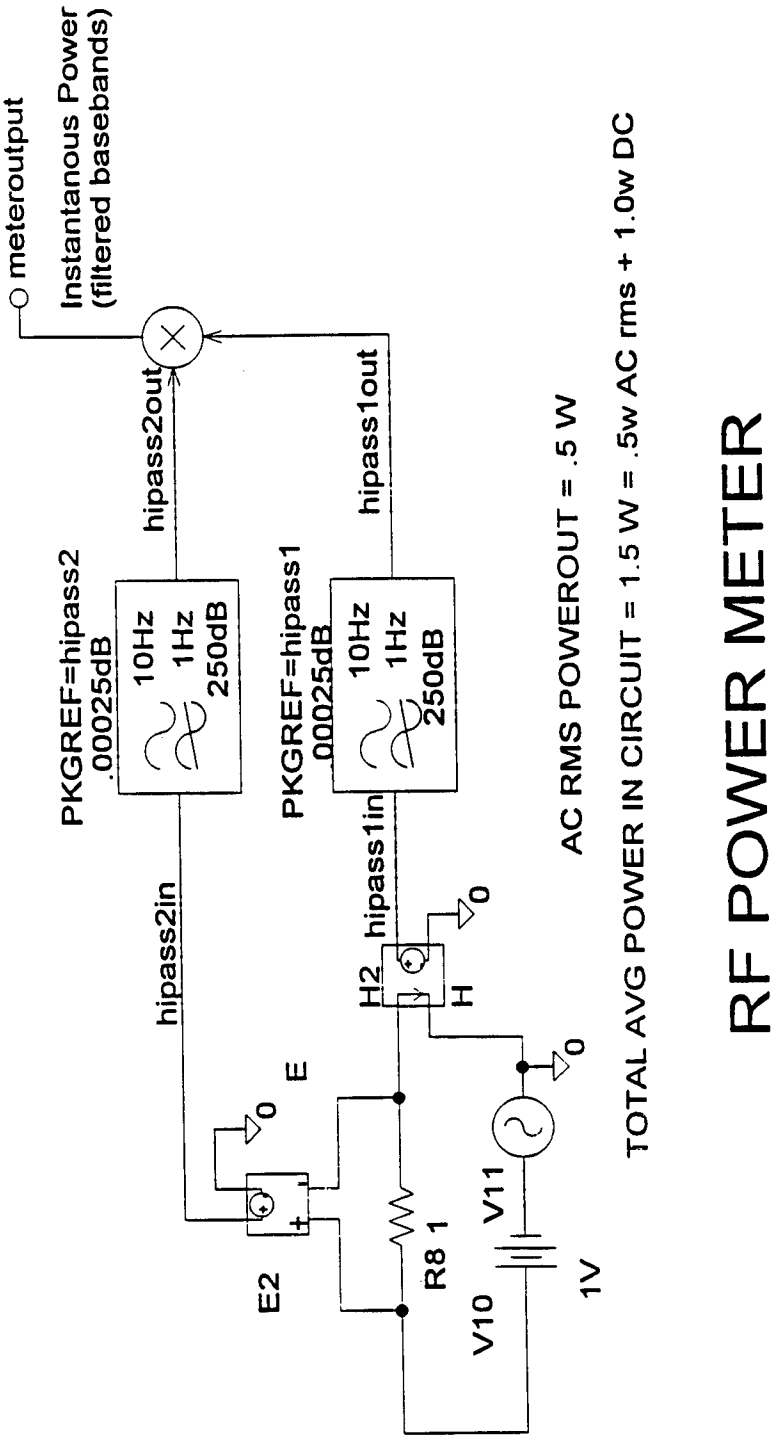


Figure 2-7 RF Power Meter for DC Blocking Capacitor Calibrations

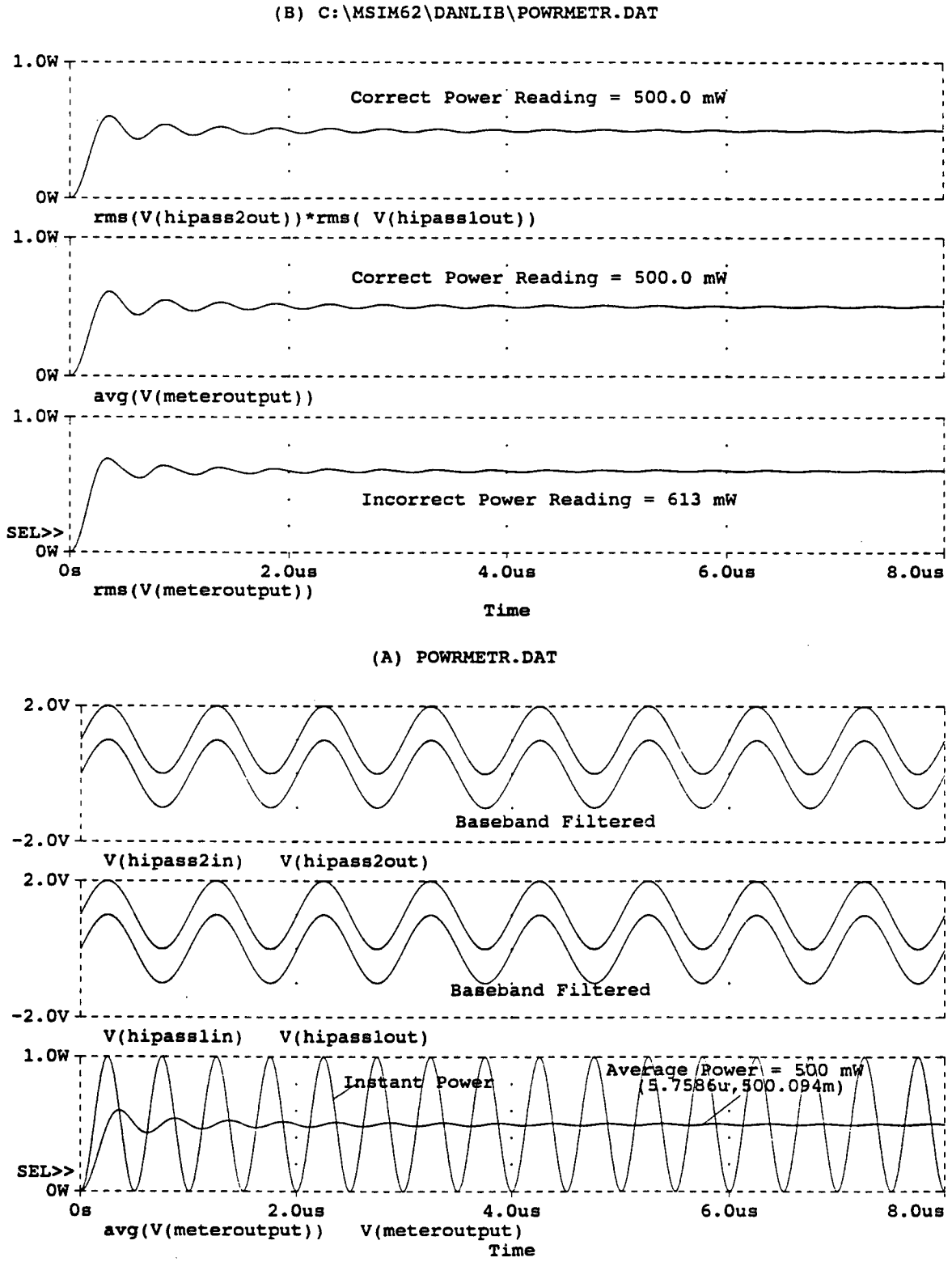


Figure 2-8 Blocking Capacitor Calibrations

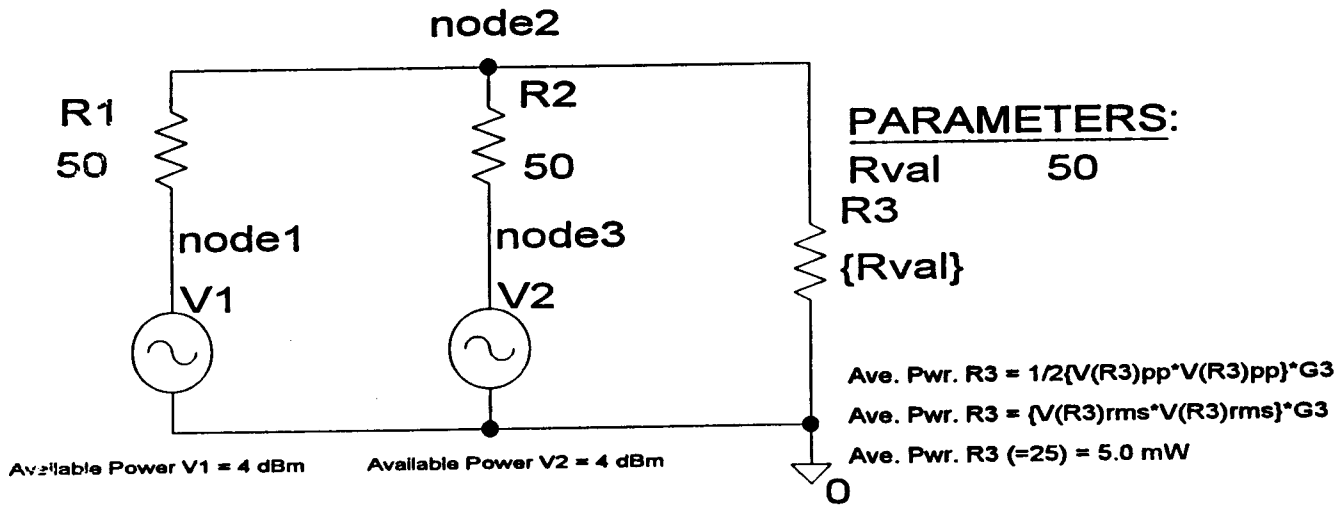


Figure 2-9 Voltage Sources in Parallel

CALIBRATES OK: MAX PWR IN R3 REQUIRES G3=2G1=2G2 = 40 mS

MAX AVAILABLE POWER V1 AND V2 = 2.5 mW

HAND CALCULATIONS SAY POWER R3 = 5.0 mW
PSPICE SAY POWER R3 = 5.0 mW

2 VOLTAGE SOURCES IN PARALLEL

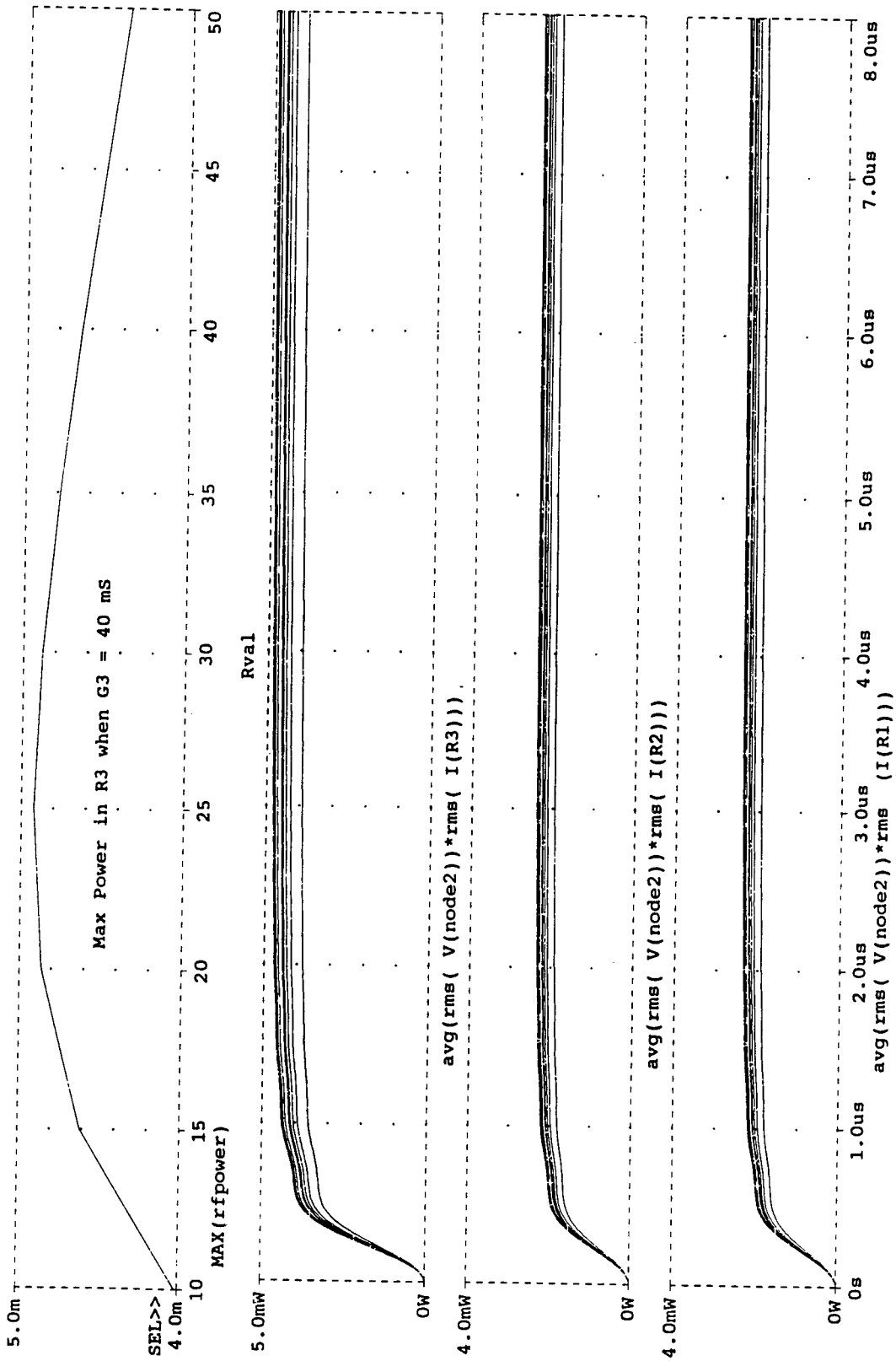


Figure 2-10 Power Levels of Sources in Parallel

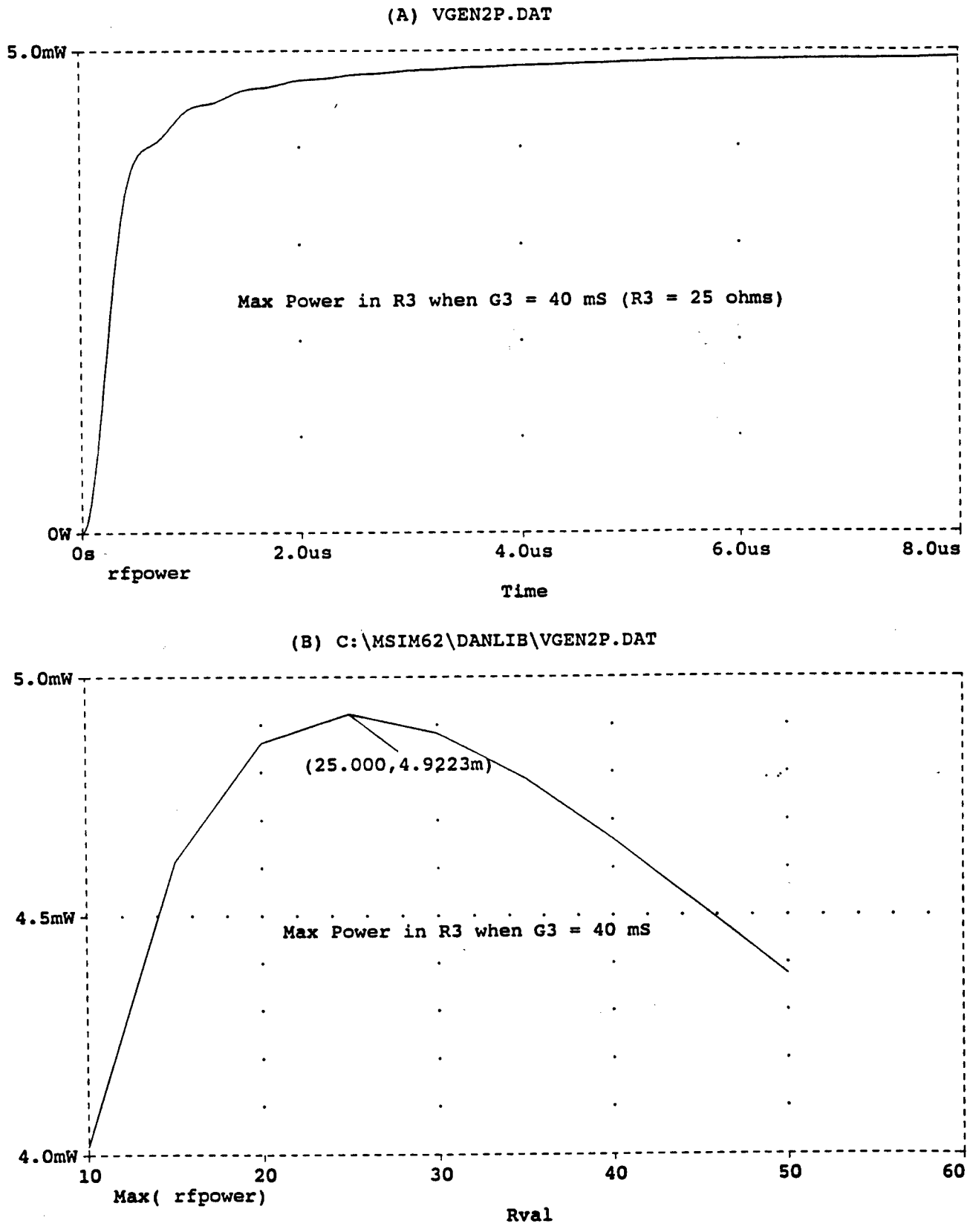


Figure 2-11 Maximum Power Theorem for Sources in Parallel

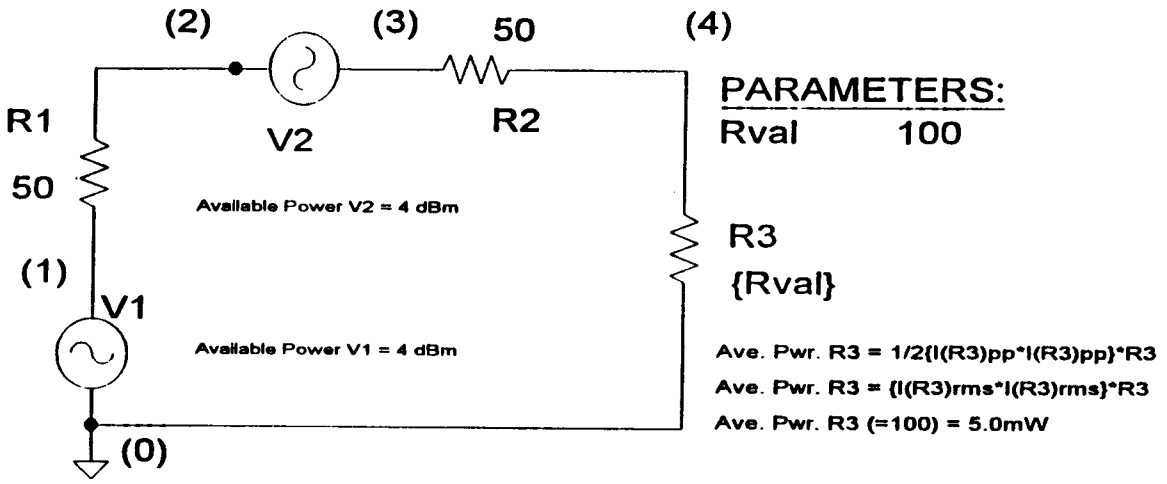


Figure 2-12 Voltage Sources in Series

max power in R2=5.0mW=2Pa1=2Pa2=2(2.5mW)

requires RL=2R1=2R2 = 100

2 VOLTAGE SOURCES IN SERIES

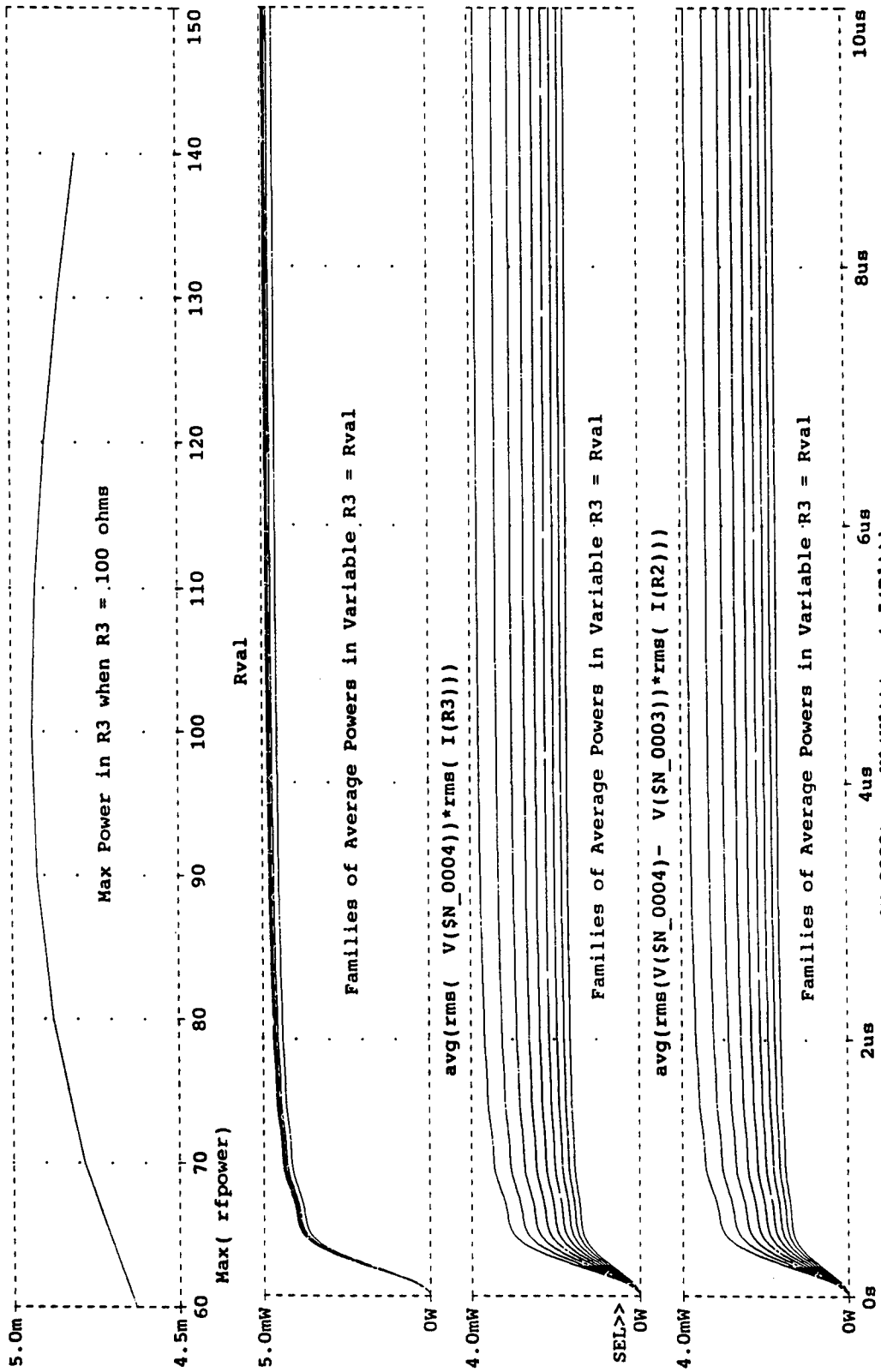


Figure 2-13 Power Levels for Sources in Series

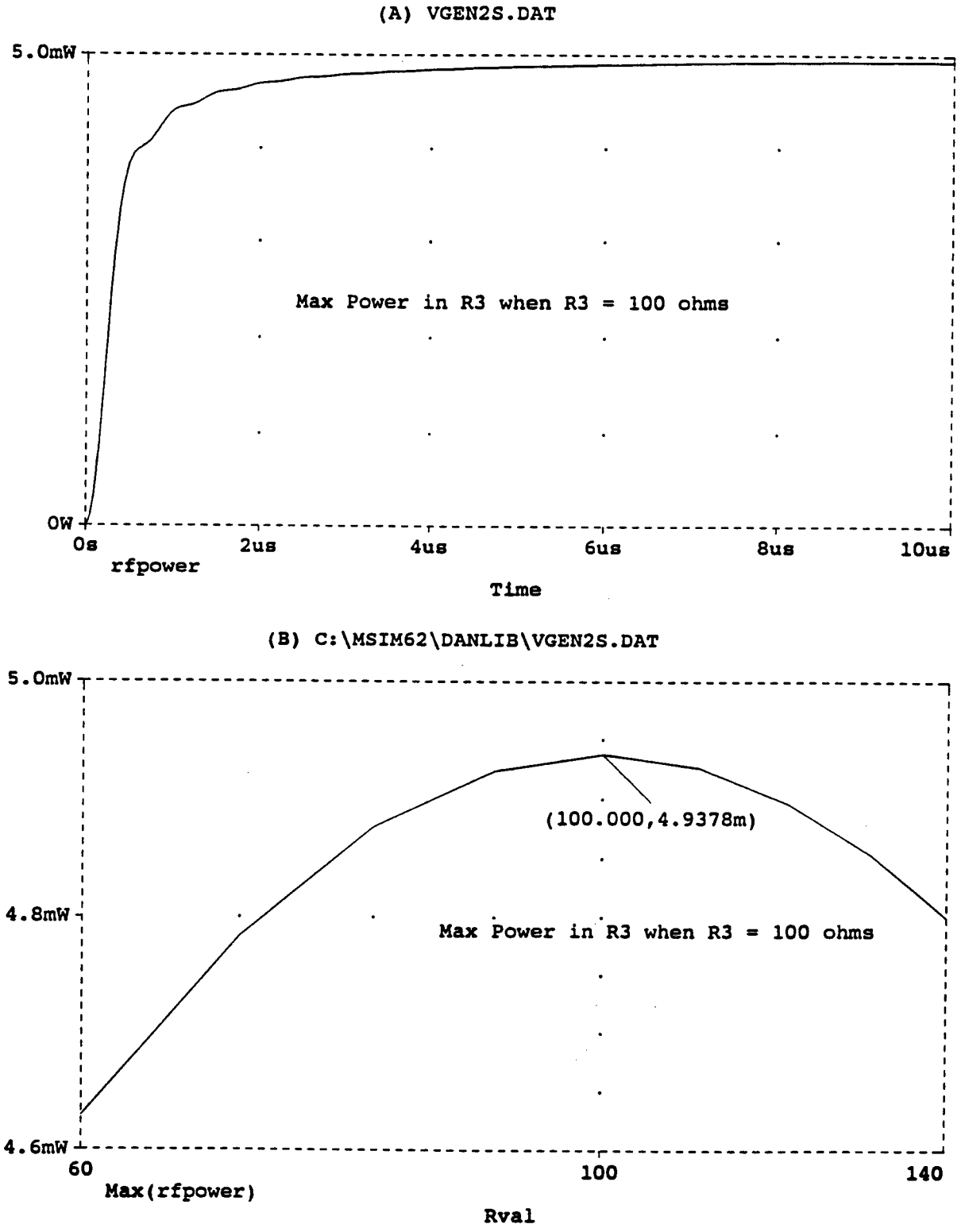
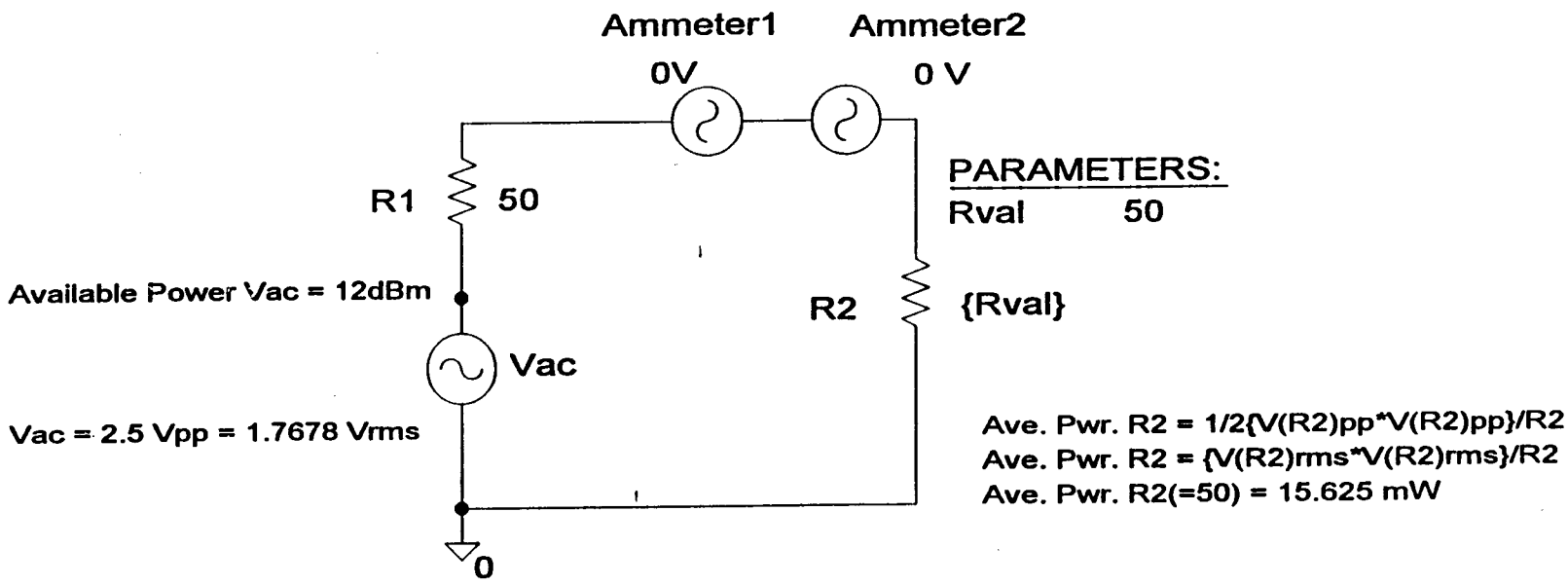


Figure 2-14 Maximum Power Theorem for Sources in Series

NOTE: Dead Sources (voltages only) used as current meters



Correct (!) avg pwr algorithm = rms(V(R2))*rms(I(R2))

NOTE: rms{(V(R2)*I(R2)} is error!

Figure 2-15 "Dead" AC Sources as Ammeters

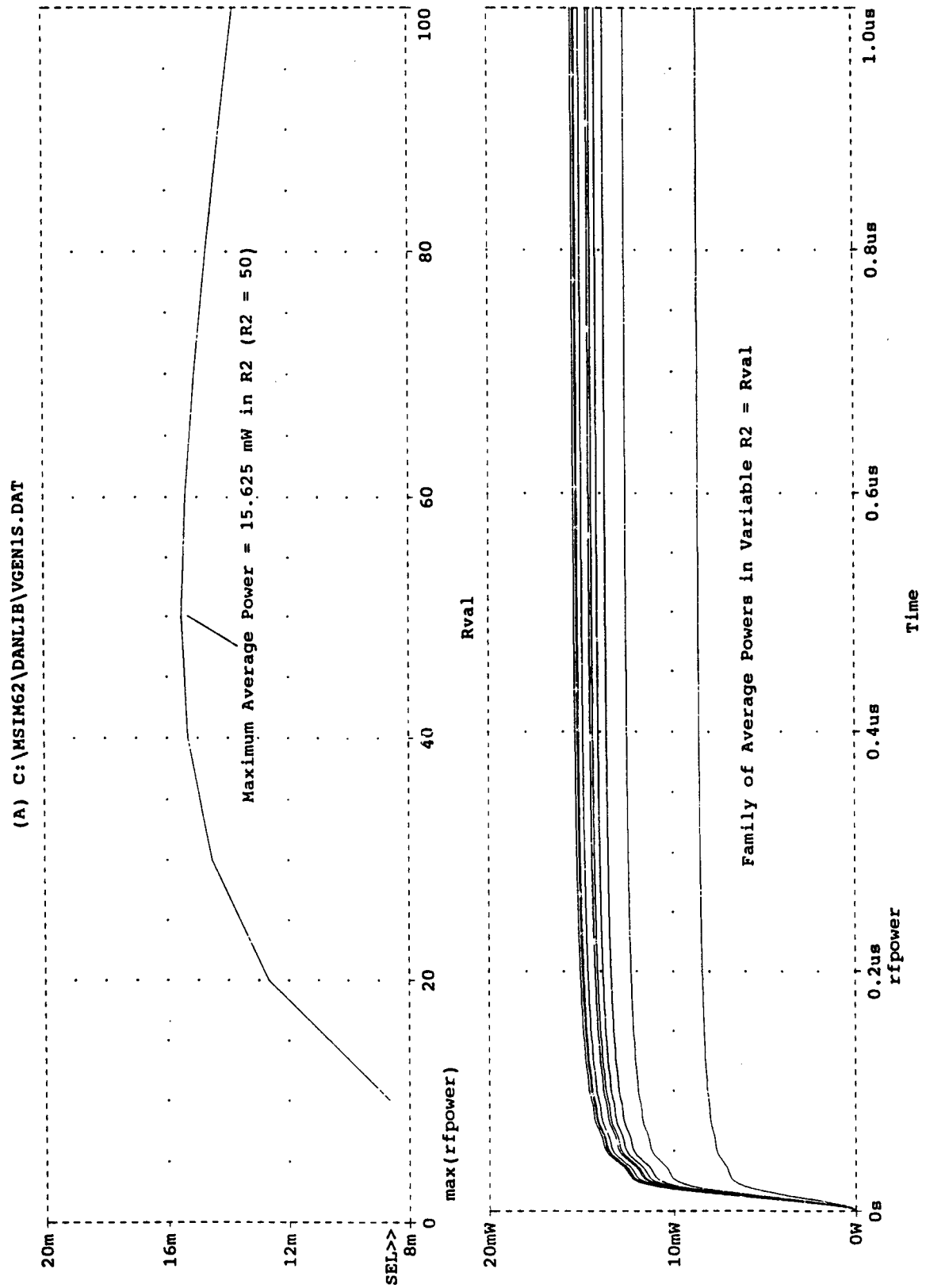
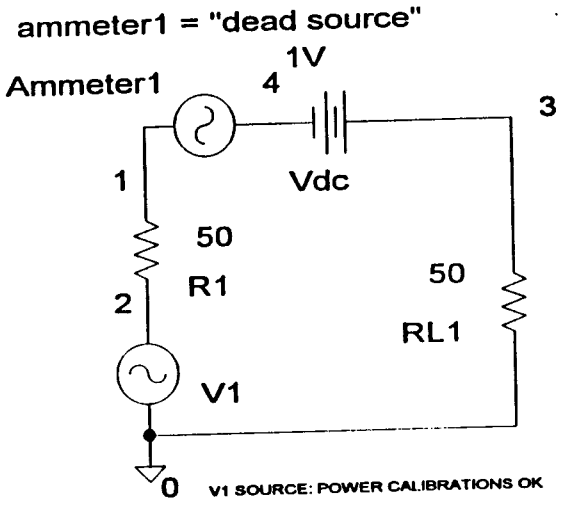
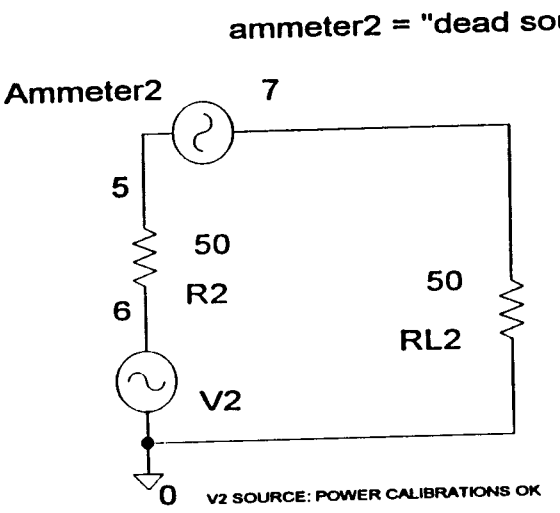


Figure 2-16 "Dead" AC Sources: Ammeter Responses





V1 Source Pwr AvaiL=4 dBm;

Total Pwr in RL1=7.5mW (8.75dBm)

V2 Source Pwr AvaiL=4 dBm;

Total Pwr in RL2=2.5mW (4 dBm)

Total Pwr in RL1=2.5 mW AC rms pwr + 5.0mW DC pwr

RMS Power Calibrations

Figure 2-17 "Dead" DC Sources as Ammeters

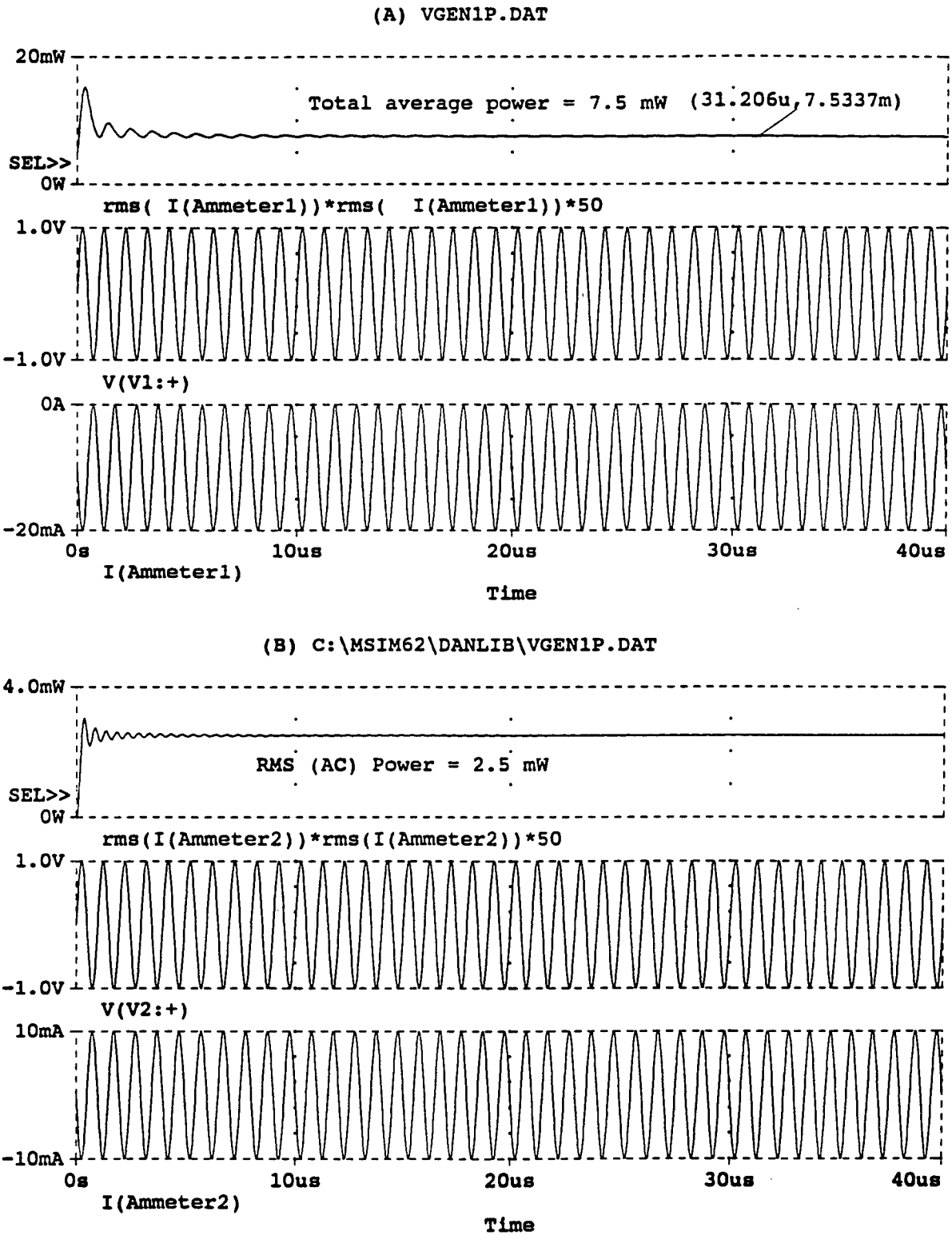


Figure 2-18 "Dead" DC Sources: Ammeter Responses

3. 54ALS03 NAND GATES

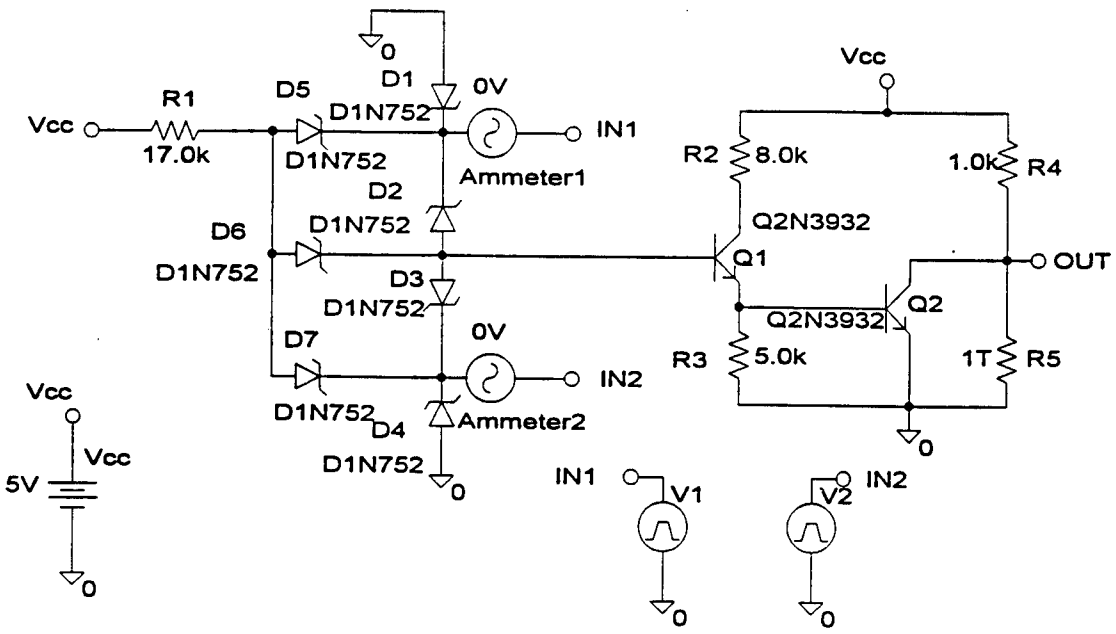
This section presents susceptibility threshold data on advanced, low power Schottky NAND gates packaged as quadruple, 2-input, positive logic with open collector outputs. During these runs some difficulty was encountered with convergence. First, the error message "unable to run PROBE" usually meant that the notepad window was open. Using some library models with DC (battery symbol) bias sources may require a very small resistor (<< 1 ohm) in series with the DC sources to permit bias point convergence. Otherwise, the simulator will not run for some unknown reason(s). In using DC batteries as bias supplies, recall that two minus polarities make a positive: for example, counting the minus plate of the battery as negative and counting the minus attribute of the battery part means that the battery will supply positive voltage. The numerical sign of attribute values for simulation-specific parts in the symbol library count in determining part polarity as well as the graphic polarity shown on the schematic. Also, to assure reasonable convergence at some nodes may require a step ceiling in the setup for transient analysis. A step ceiling of 1 ps seemed to be adequate.

Figure 3-1 shows the baseline gate and its logic response to two overlapping input pulses. Figure 3-2 shows the gate being driven with 10 MHz voltage source in parallel with its Vcc bias rail. Also shown are responses where no logic upset was observed for input cw levels up to about 180 mW. Figure 3-3 shows the gate being driven with a 10 MHz current source in parallel with its Vcc bias rail. Again, no logic upset was observed for very low input cw levels up to 40 uW. Figure 3-4 shows the gate being driven with a 10 MHz voltage source in series with its Vcc bias rail. While there does not seem to be a logic upset (i.e., output is still low), there is considerable ripple that may effect the noise margin of the succeeding gates. Figure 3-5 presents detail data on the ripple build-up for input cw powers levels from 5.3 dBm to 11.5 dBm. Figure 3-6 shows the gate being driven with a 30 MHz current source in series with its logic in1. Figure 3-7 shows the build-up of threshold susceptibility for cw levels from 4.6 dBm to 19.4 dBm with advent of bit errors around 12 dBm.

Figure 3-8 shows the gate being driven with a 10 MHz voltage source in parallel with logic in1. As indicated, on upset was observed for cw input levels from about 80 mW to 120 mW. Figure 3-9 shows the gate being driven with a 10 MHz voltage source in series with its logic in1. Upset levels are apparent. Figure 3-10 shows detail build-up of susceptibility for cw levels from 5.5 dBm to 11.5 dBm. Some output noise and digital upset is apparent at threshold levels between 5 and 7 dBm. Figure 3-11 shows the gate being driven with a 20 MHz voltage source in series with its logic in1. Again, upset levels are apparent only higher than before. Figure 3-12 shows the detail build-up of susceptibility for cw levels from 10.7 dBm to 16 dBm. Note that the upset thresholds seem to now be higher at around 10 dBm as compared to those at 10 MHz. It seems that the gate needs more EM power to cause upset as frequency increases. Figure 3-13 shows the gate now driven at 30 MHz. Again, upset threshold levels seem to require more cw power at around 12.5 dBm. Figure 3-14 gives more detail of the build-up. Figure 3-15 shows the gate being driven with a 10 MHz voltage source in parallel with logic in2 to compare with Figure 3-8. Again, no logic upset was observed for cw input levels from about 50 mW to 100 mW.

Figures 3-16 (a-q) presents the total simulation output file for the gate shown in Figure 3-17. It is being driven by a 10 MHz voltage source at the base of Q3 transistor inverter. Note the "RFameter" dead source to monitor input current into the inverter input port defined by the Vrfin label. Figure 3-17 shows apparent upset in the range of input cw level between 5 and 70 mW. Figure 3-18 shows first cull detail of the susceptibility build-up for data between - 8 dBm and 15.6 dBm. Note that when the EM source levels drop very low below 6.9 dBm down to - 8 dBm, the EM source is now essentially short circuiting the Q3 inverter input to ground and causes the gate to latch to Vcc. This does not seem realistic. Simulating very low level EM signals by simply lowering the equivalent source amplitude in this manner gives questionable results. Figure 3-19 shows further culled detail of the susceptibility build-up for data between 12.8 dBm and 6.9 dBm. As indicated, the transition

from latch-up to bit errors seems to occur between 10.9 dBm and 11.9 dBm. Figure 3-20 steps the frequency range up to 20 MHz at the inverter input. Figure 3-21 shows detail of the first cull, susceptibility build-up for cw input levels between 17.8 dBm and - 6.6 dBm. The transition from latch-up to bit errors seems to occur between 14.1 dBm and 15.7 dBm, slightly higher than power required for 10 MHz in figure 3-19. Figure 3-22 shows a more detail cull of the susceptibility build-up for cw input levels between 13.76 dBm and 15.39 dBm. The culled measure of the transition now seems to be around 14.45 dBm; again, higher than that at 10 MHz. Figure 3-23 steps the frequency up to 30 MHz at the inverter input. Figure 3-24 shows threshold data for input cw levels sweeping from 5 mW to 50 mW. Figure 3-25 show detailed culls of power levels between 15.41 dBm and 16.88 dBm. Upset seems to threshold around 16 dBm, again higher than that noted for the previous two lower frequencies.



54ALS03 NAND BASELINE

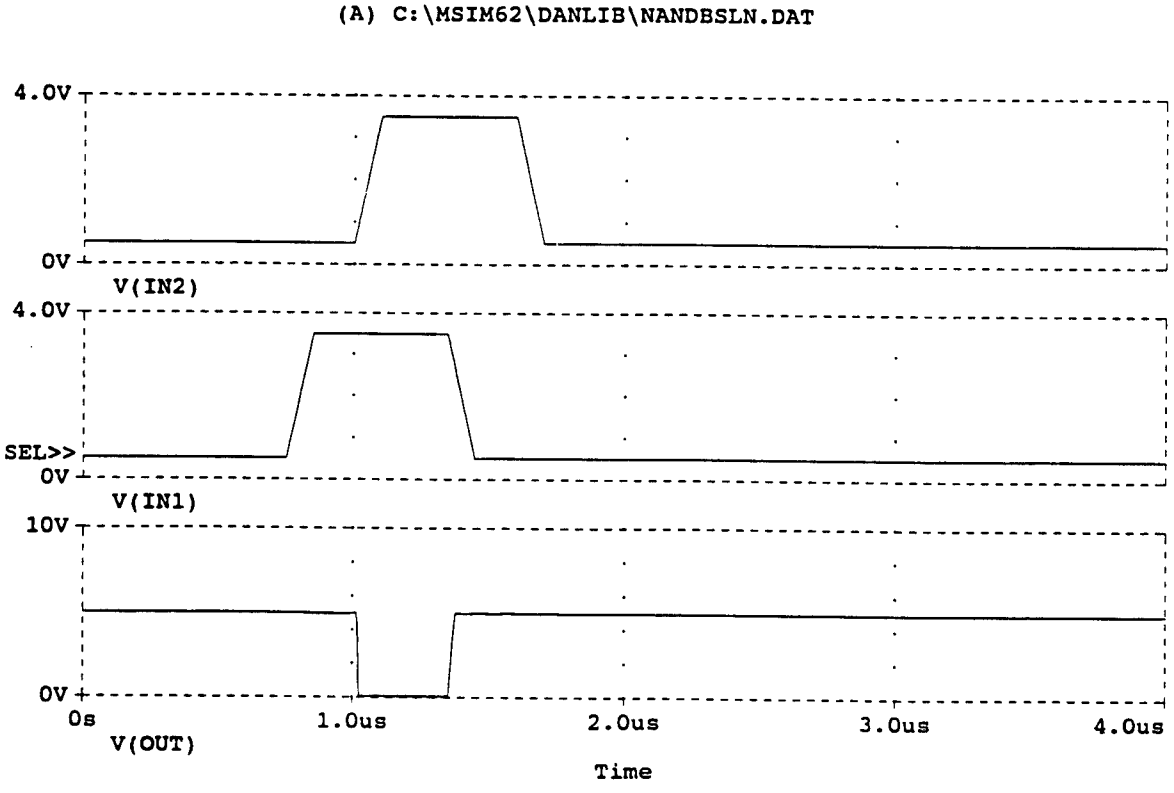
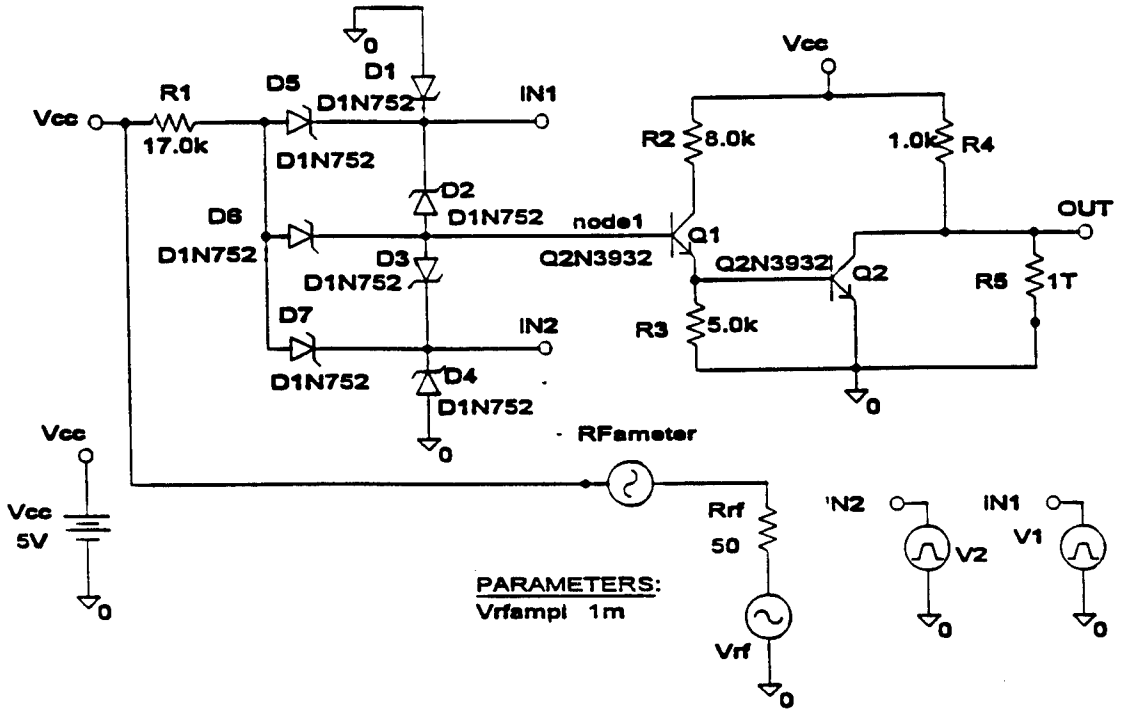


Figure 3-1 54ALS03 NAND Gate Baseline and Logic Responses



54ALS03 NAND GATE: 10MHZ @ Vcc BIAS RAIL

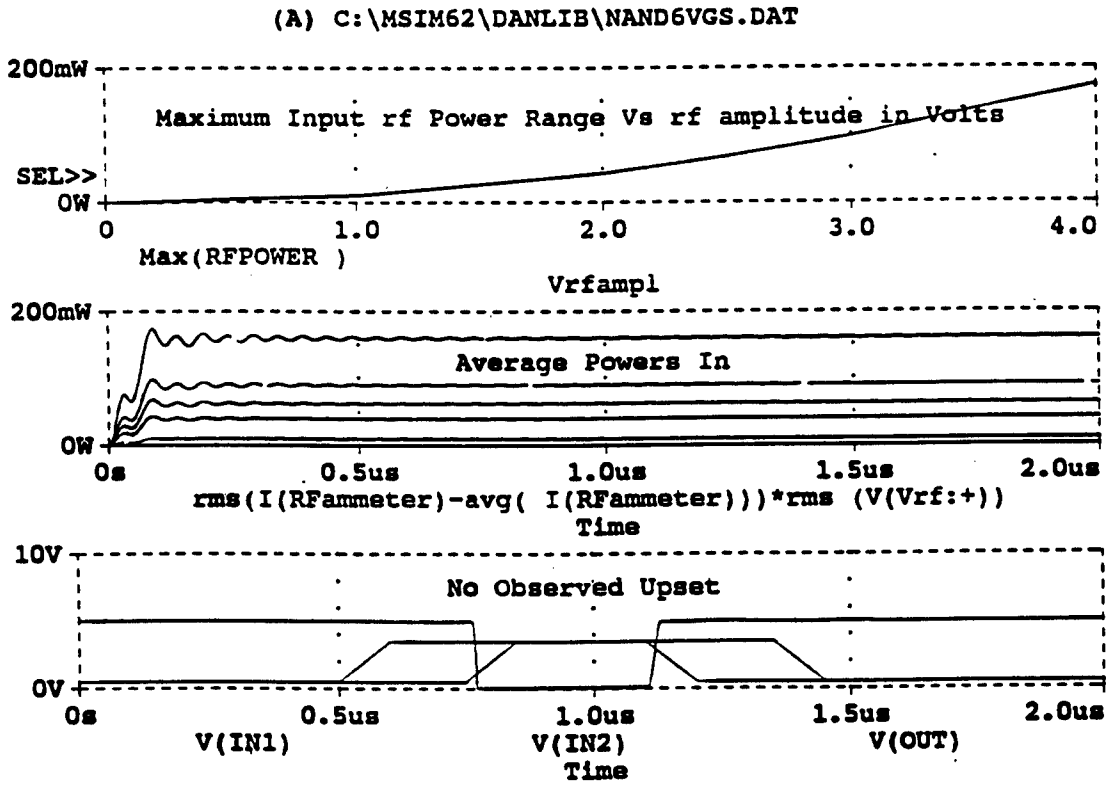
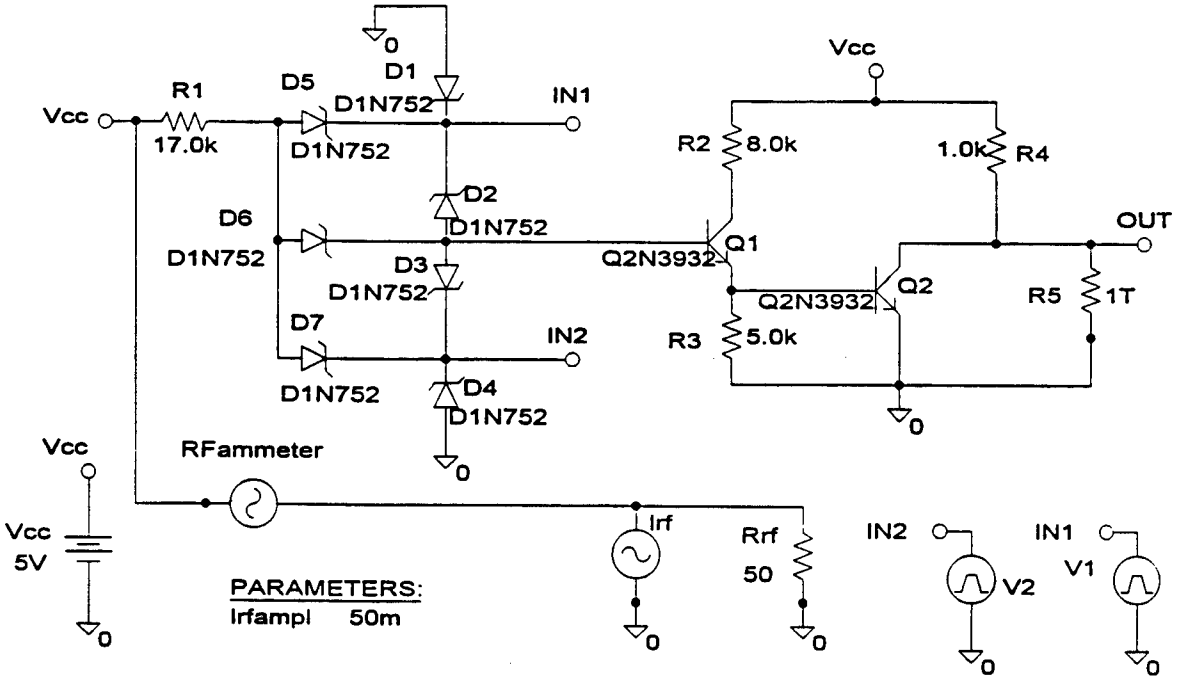


Figure 3-2 10 MHz Voltage Source in Parallel with Vcc Bias Rail



54ALS03 NAND GATE: 10MHZ ISOURCE INTO Vcc RAIL

(A) C:\MSIM62\DANLIB\NAND7VGS.DAT

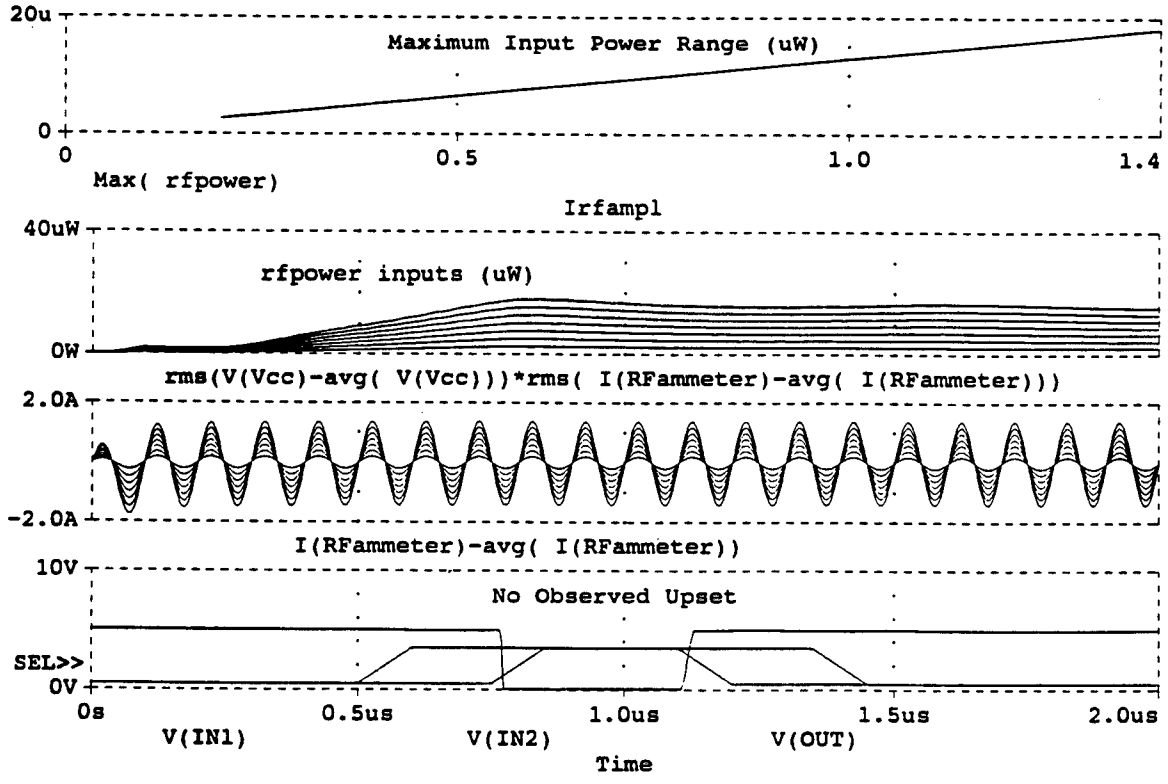
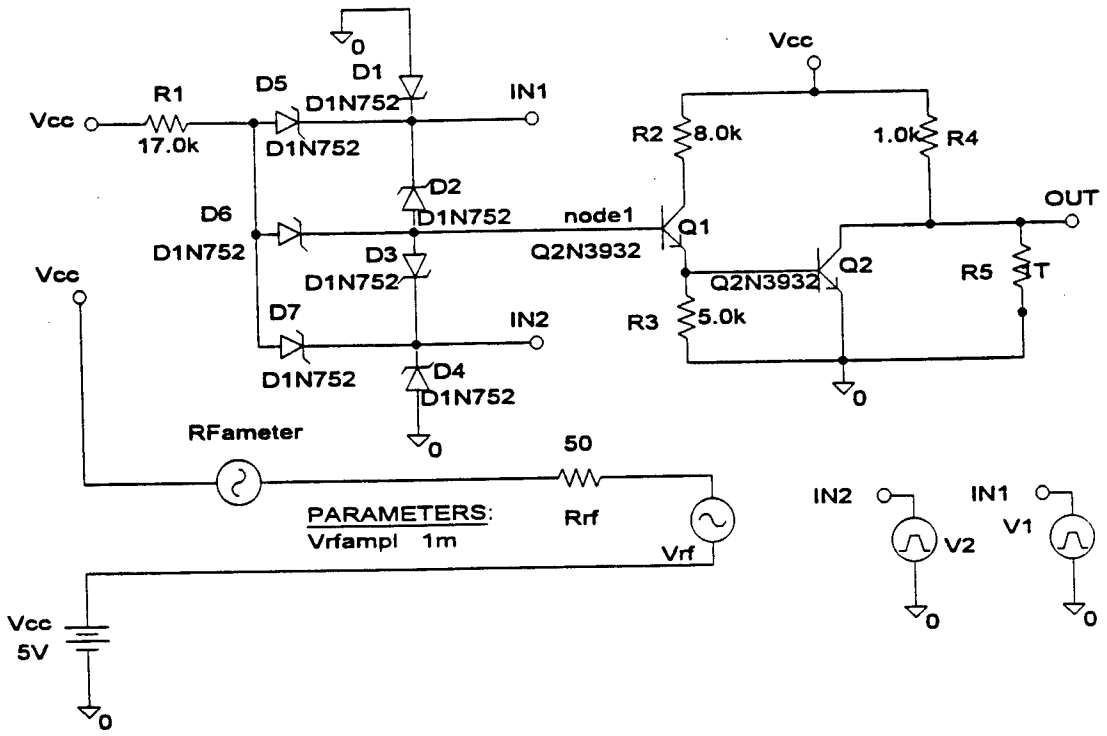


Figure 3-3 10 MHz Current Source in Parallel with Vcc Bias Rail



54ALS03 NAND GATE: (SERIES) 10MHZ @ Vcc BIAS RAIL

(A) C:\MSIM62\DANLIB\NAND6VG5.DAT

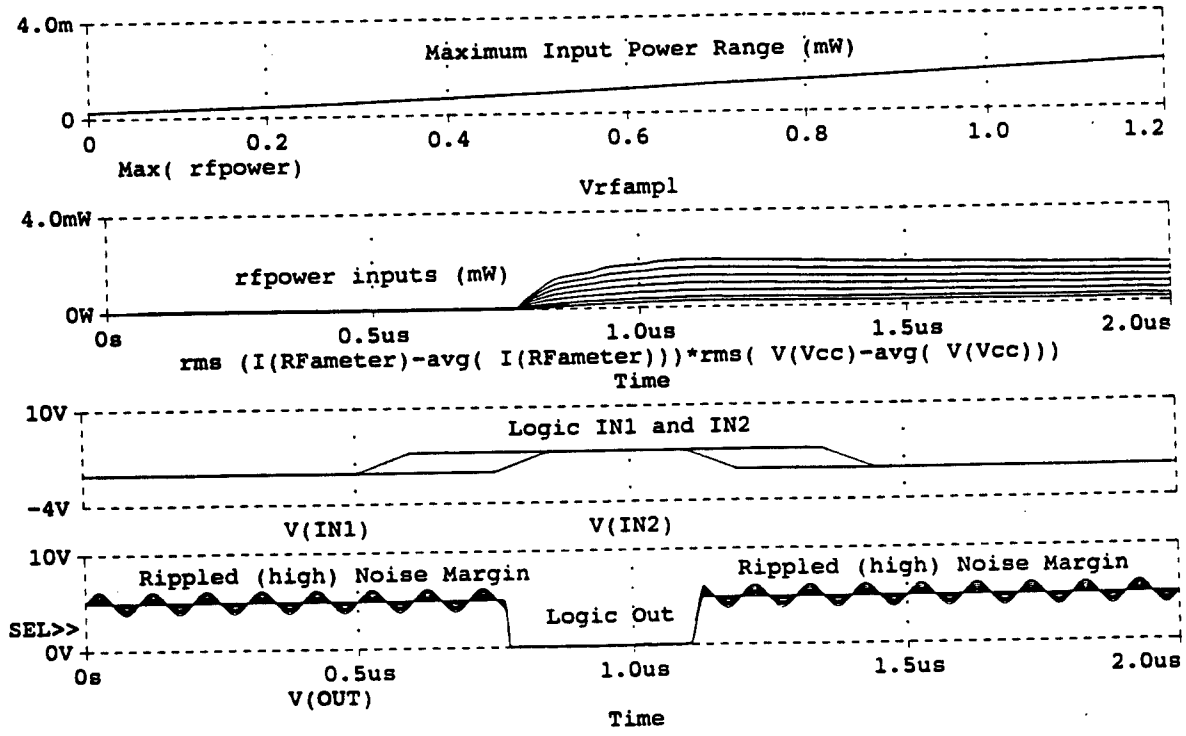


Figure 3-4 10 MHz Voltage Source in Series with Vcc Bias Rail

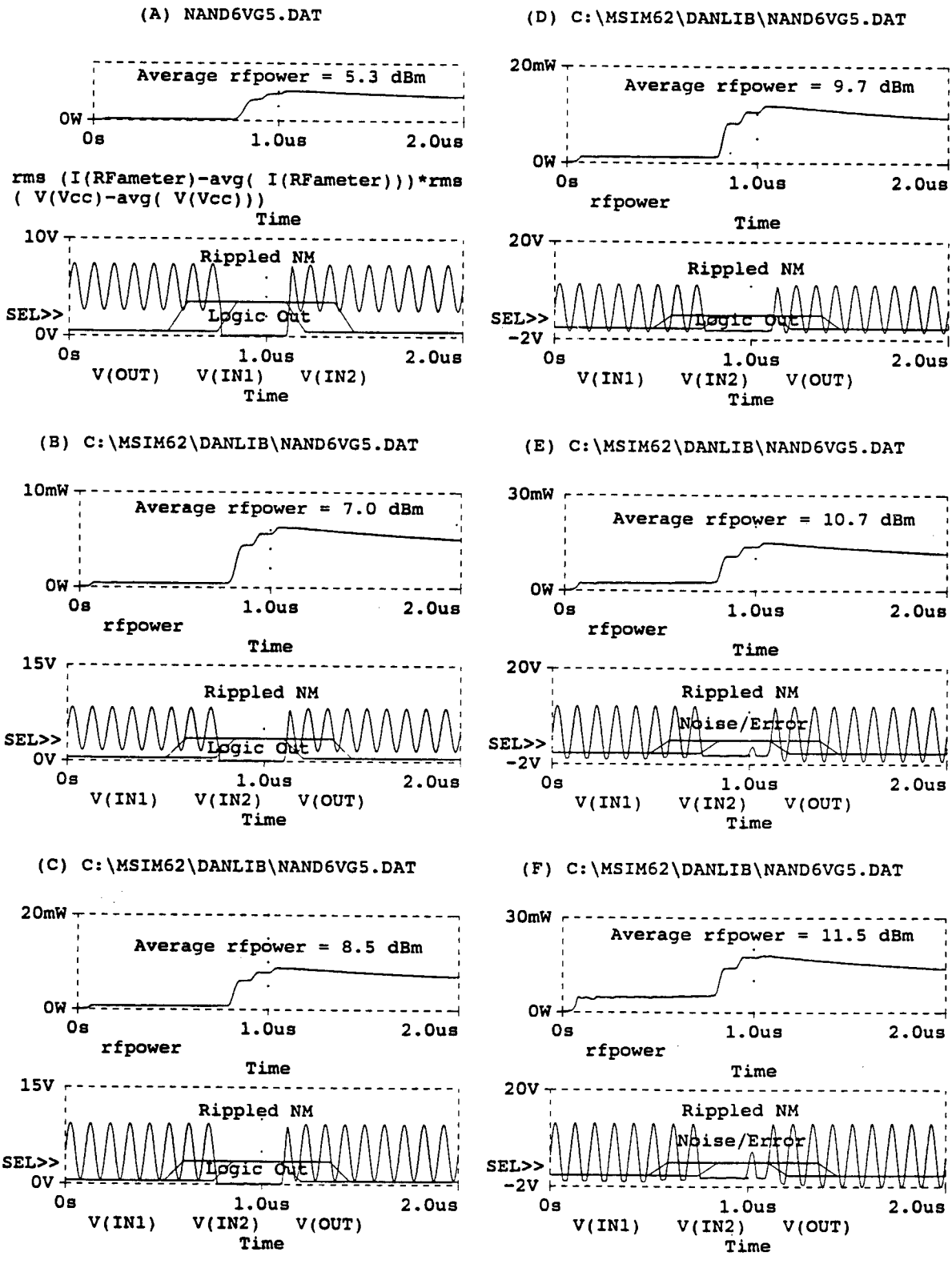
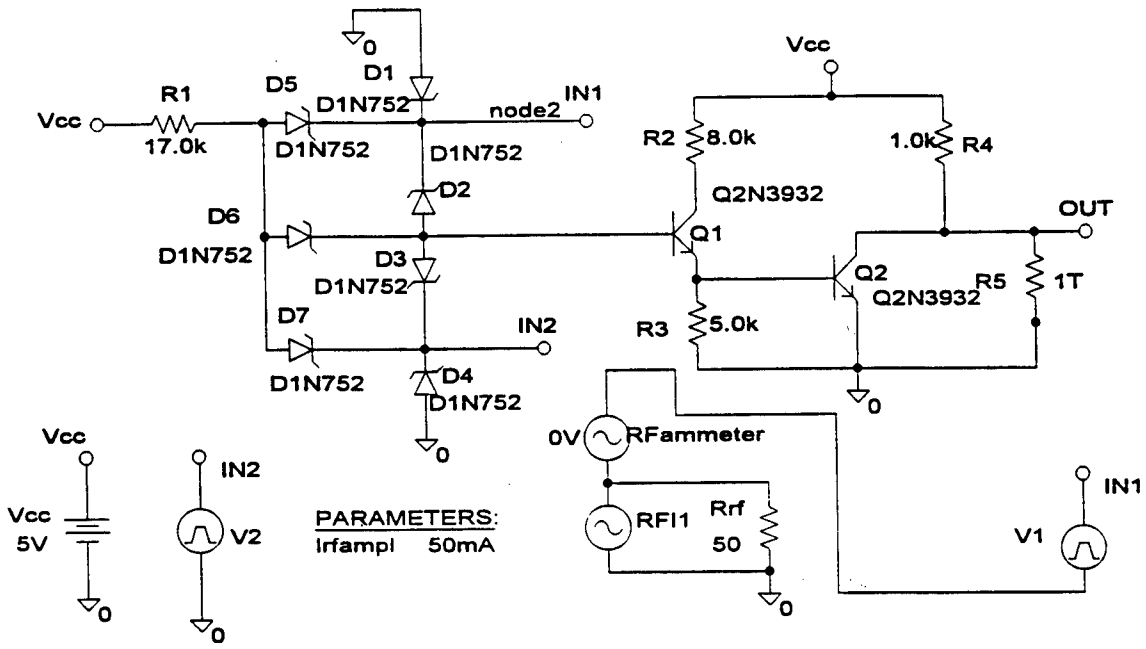


Figure 3-5 Ripple Noise Build-Up



54ALS03 NAND GATE: (SERIES) 30MHZ ISOURCE @ LOGIC IN1

(A) C:\MSIM62\DANLIB\NAND9VGS.DAT

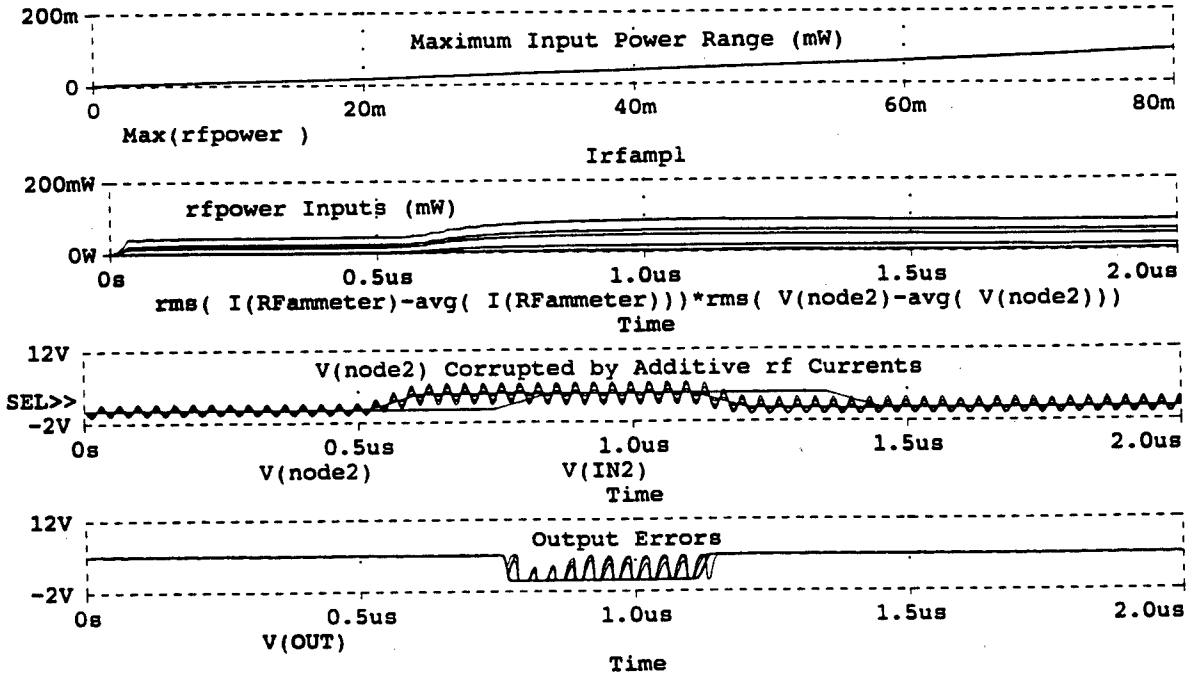


Figure 3-6 30 MHz Current Source in Series with LOGIC IN1

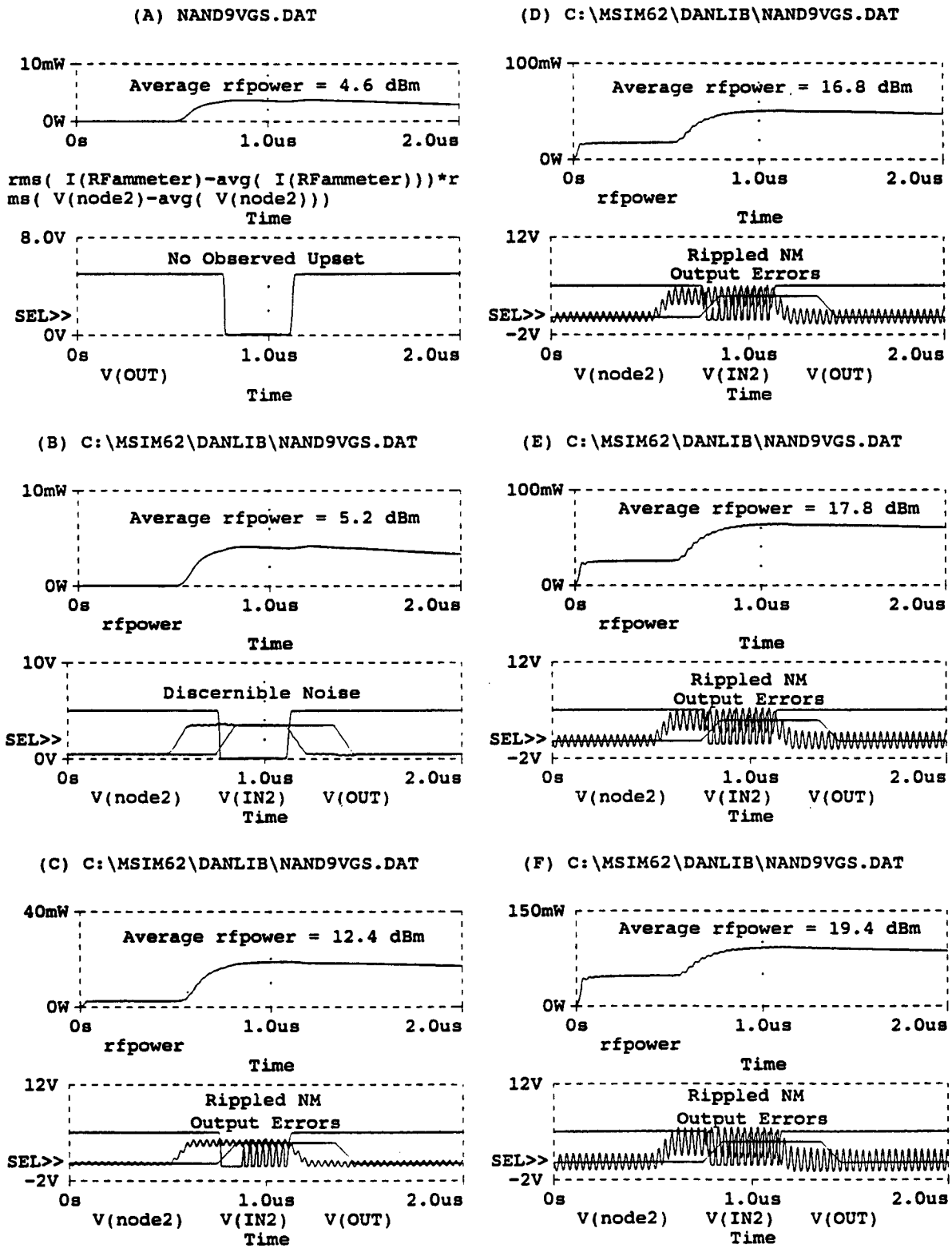
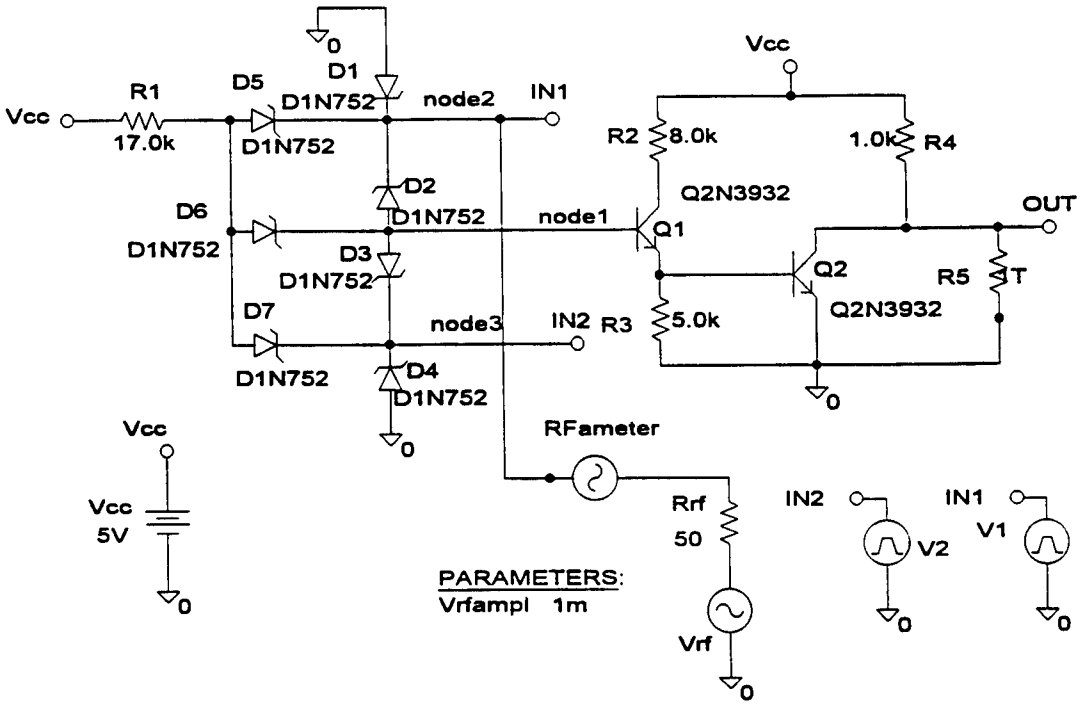


Figure 3-7 Build-Up of Threshold Susceptibility



54ALS03 NAND GATE: 10MHZ @ LOGIC IN1

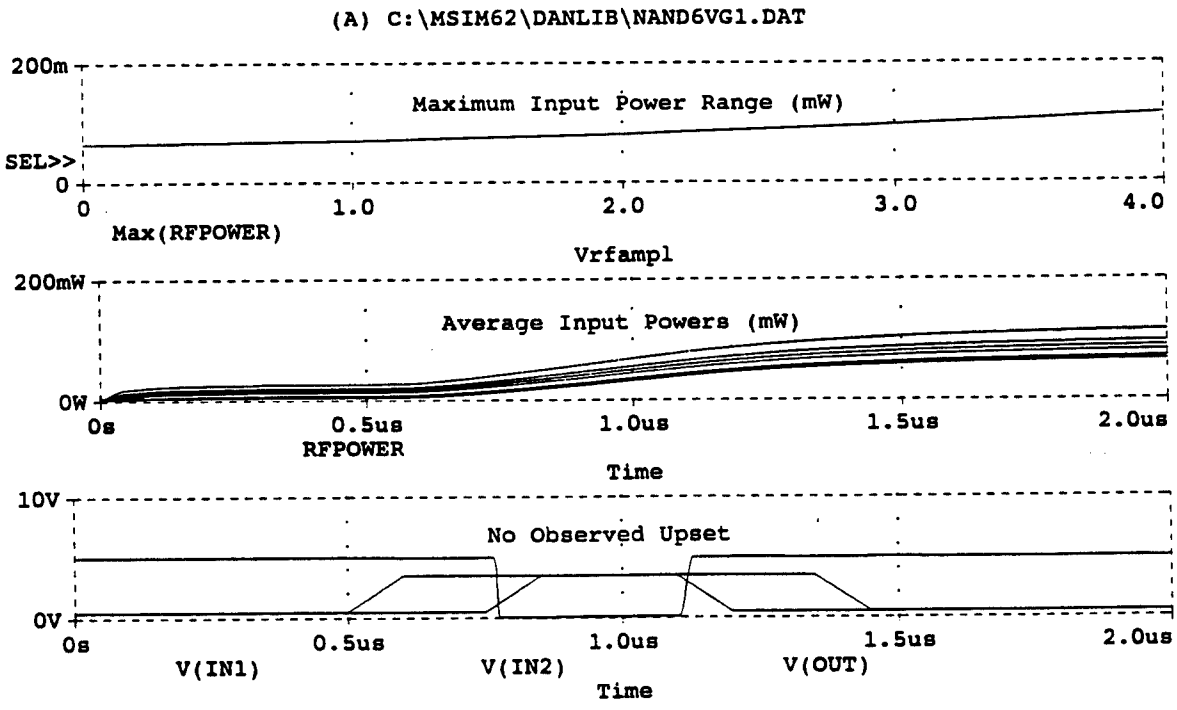
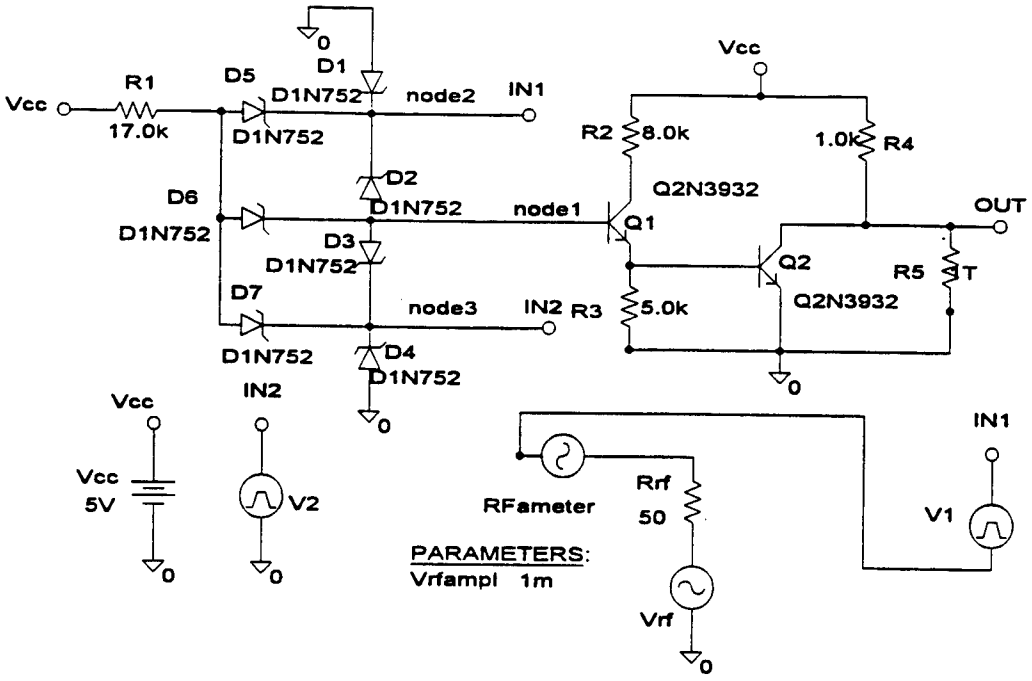


Figure 3-8 10 MHz Voltage Source in Parallel with LOGIC IN1



54ALS03 NAND GATE: (SERIES) 10MHZ @ LOGIC IN1

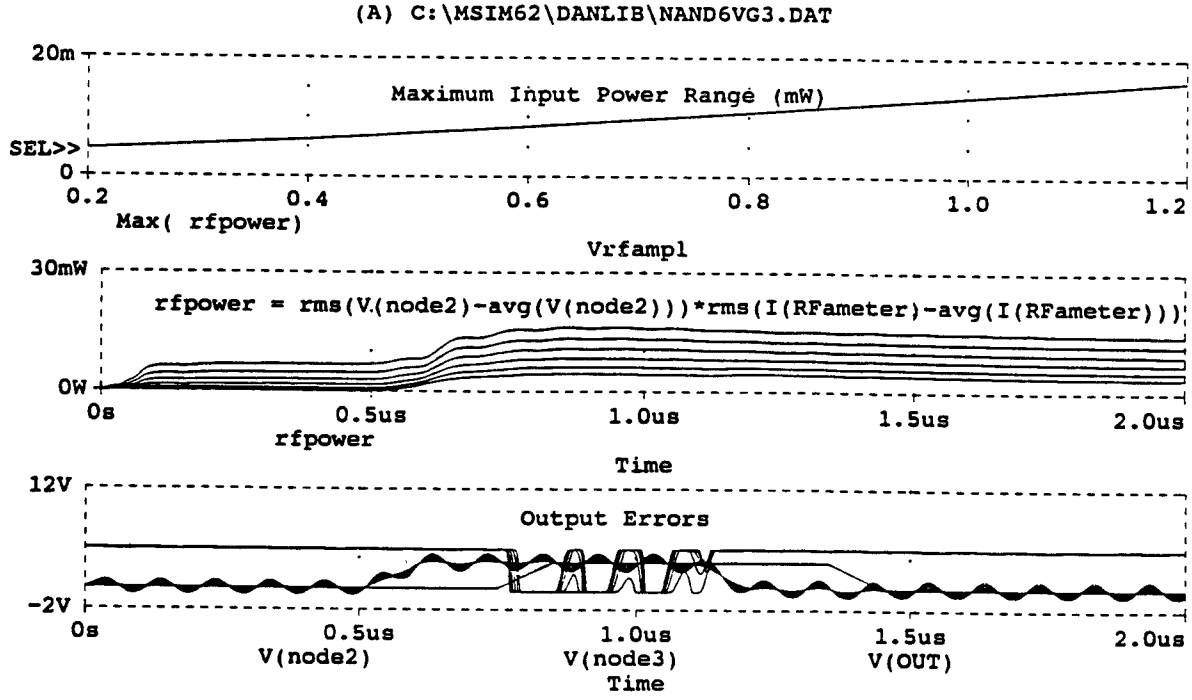


Figure 3-9 10 MHz Voltage Source in Series with LOGIC IN1

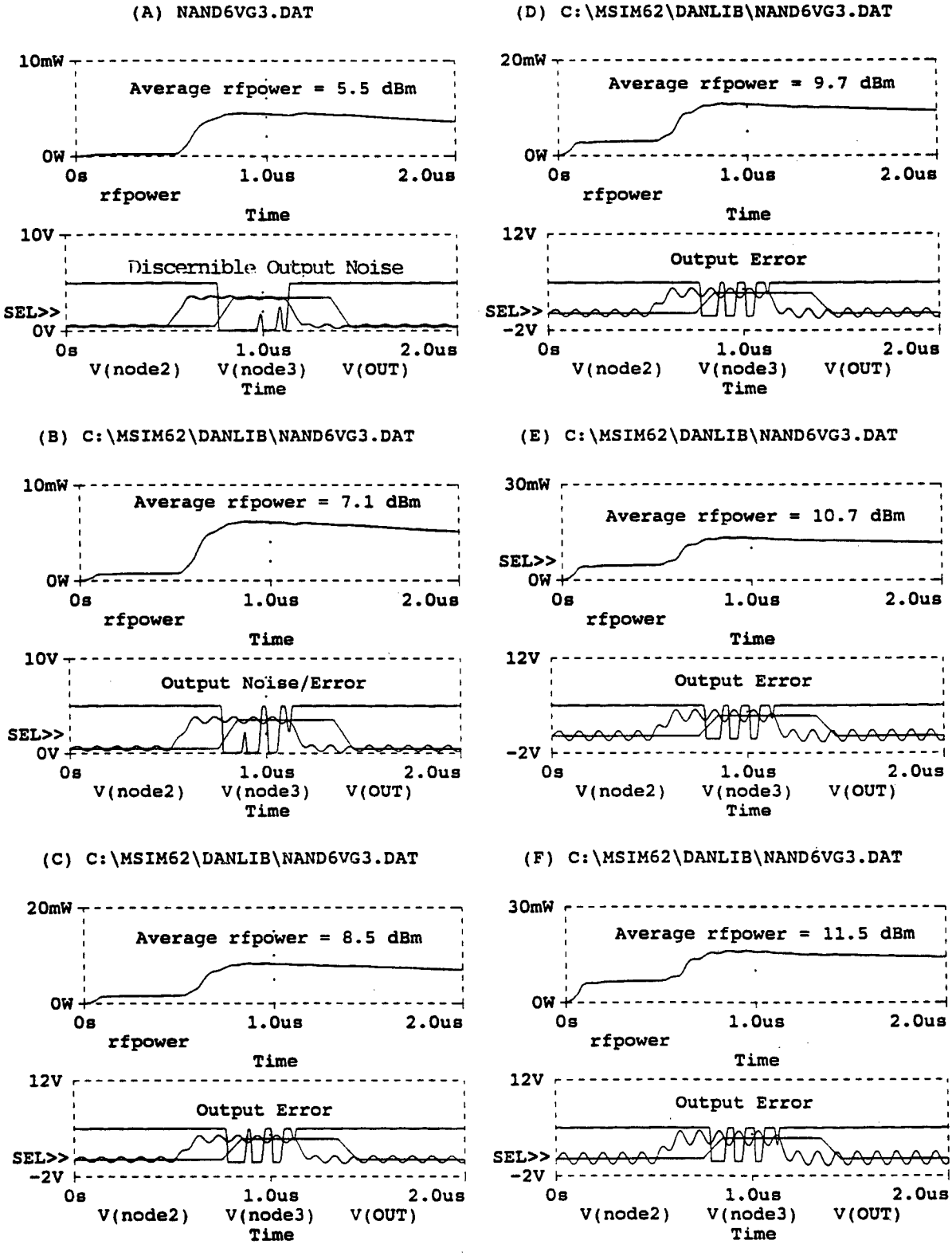
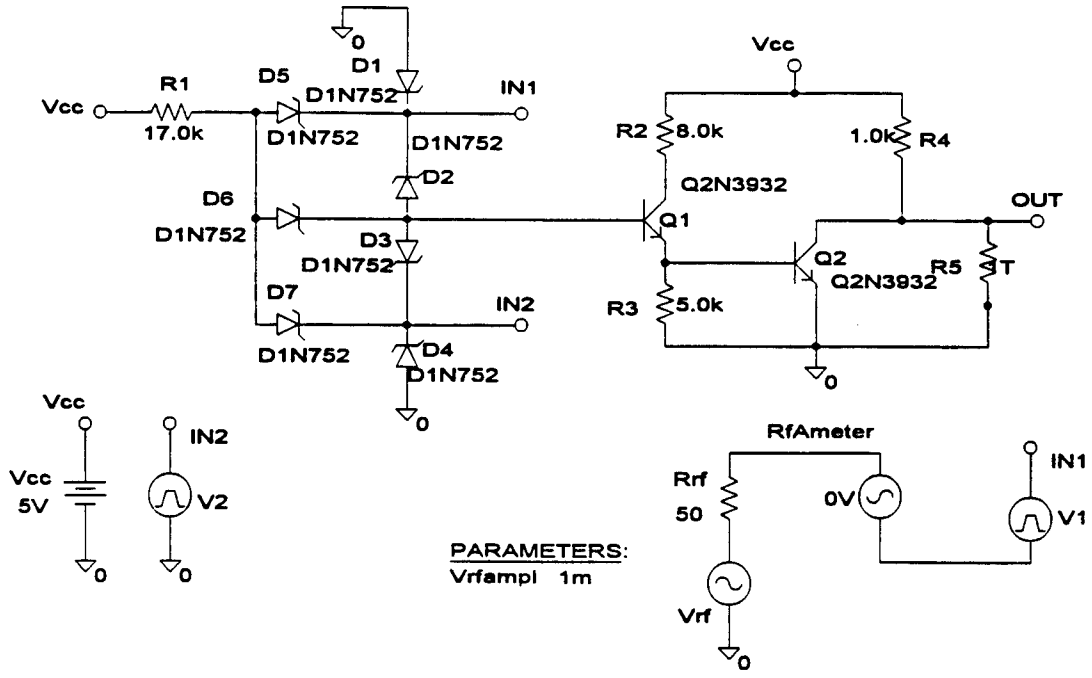


Figure 3-10 Susceptibility Threshold Build-Up



54ALS03 NAND GATE:(SERIES) 20MHZ @ LOGIC IN1

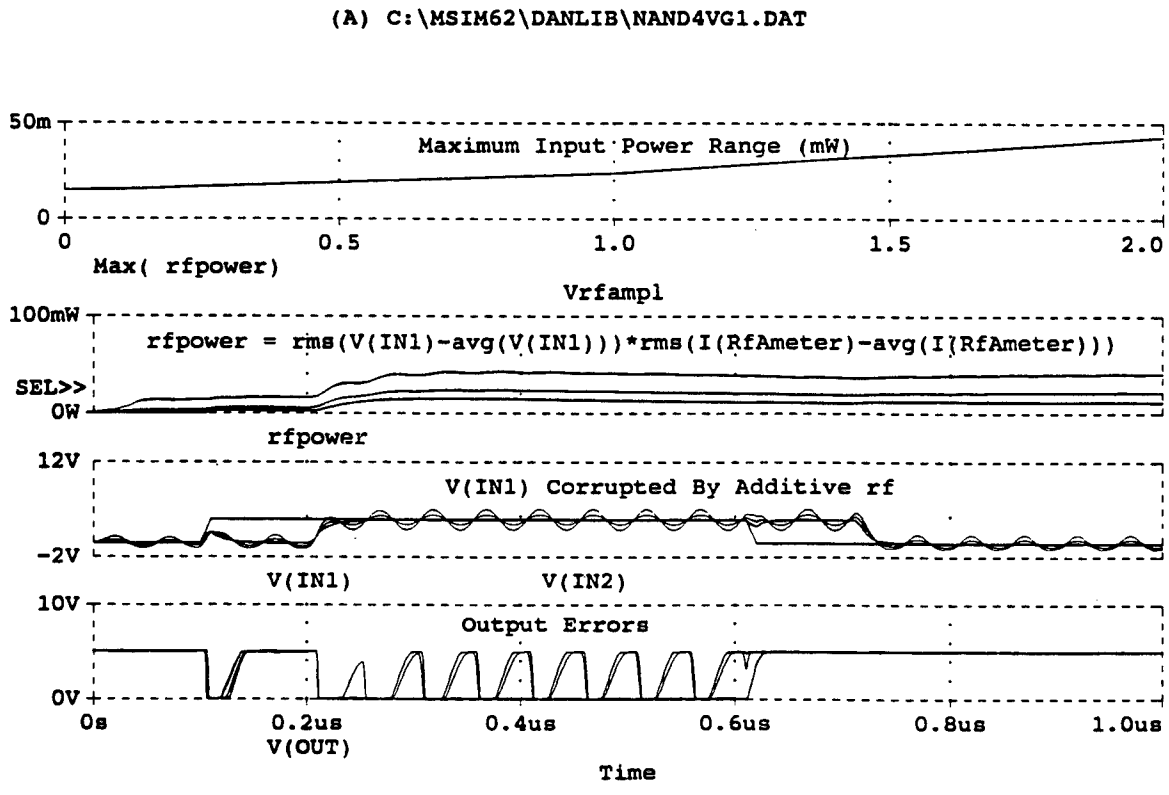


Figure 3-11 20 MHz Voltage Source in Series with LOGIC IN1

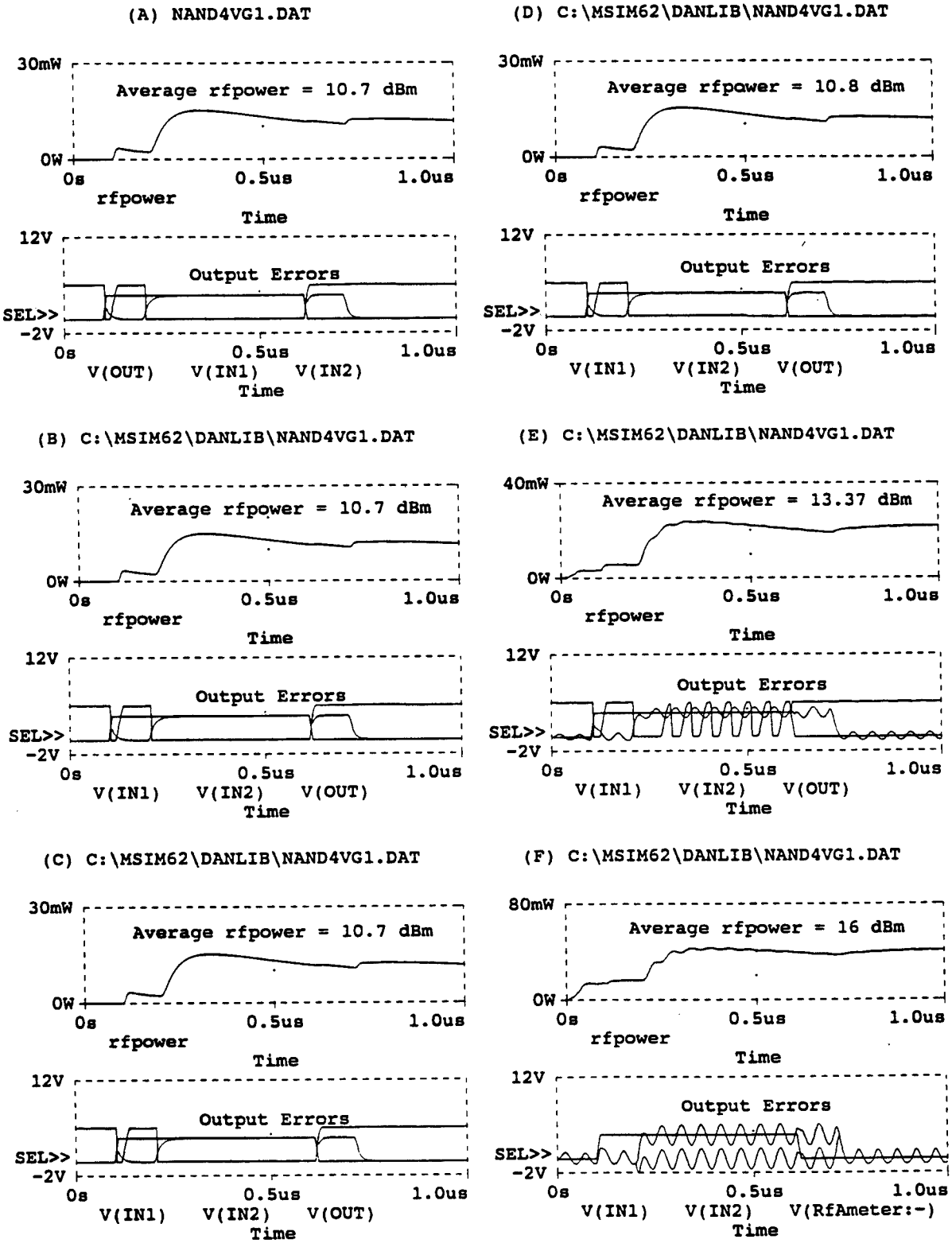
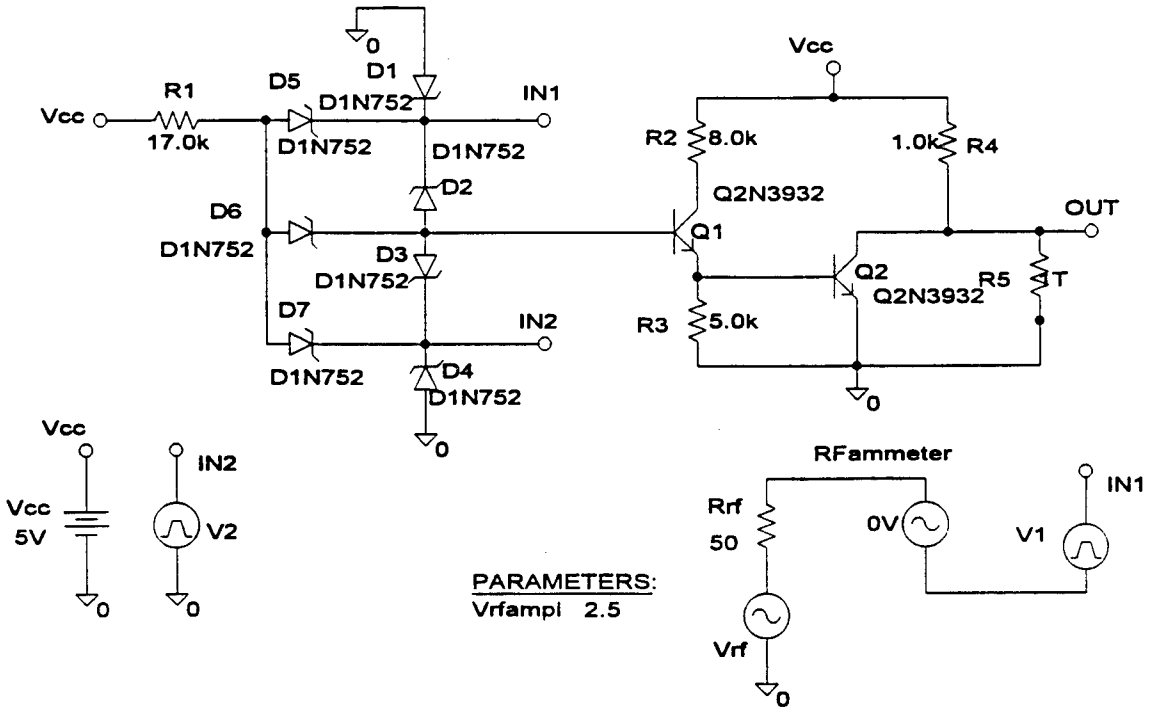


Figure 3-12 Susceptibility Threshold Build-Up



54ALS03 NAND GATE: (SERIES) 30MHZ @ LOGIC IN1

(A) C:\MSIM62\DANLIB\NAND3VG1.DAT

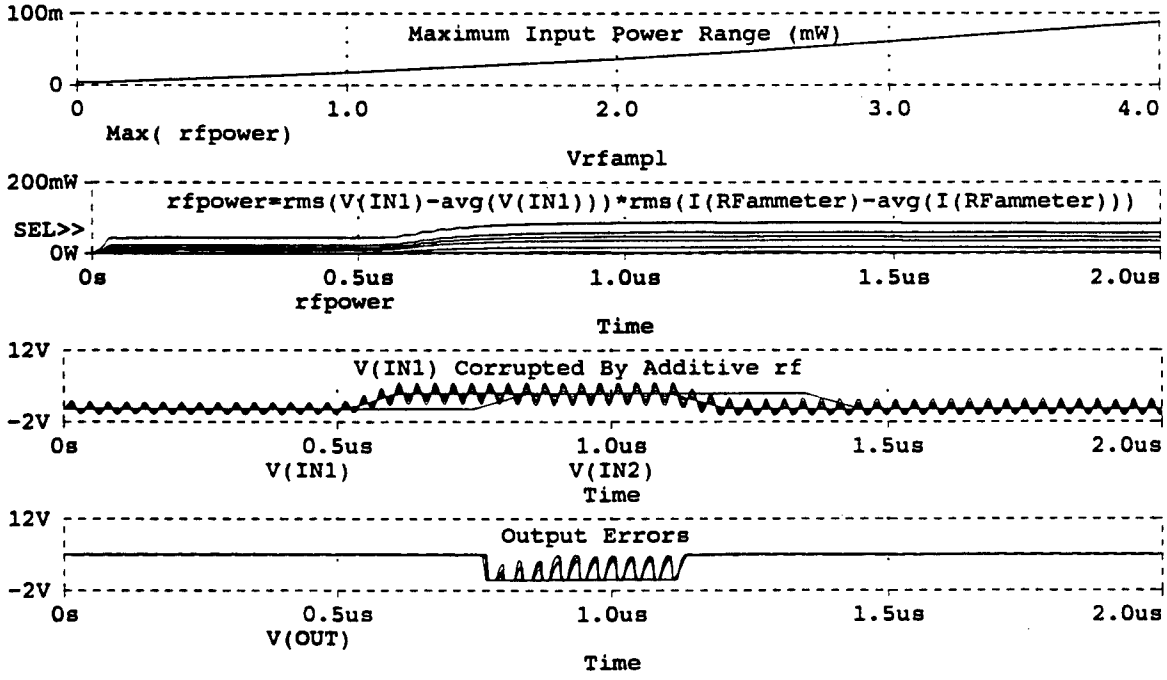


Figure 3-13 30 MHz Voltage Source in Series with LOGIC IN1

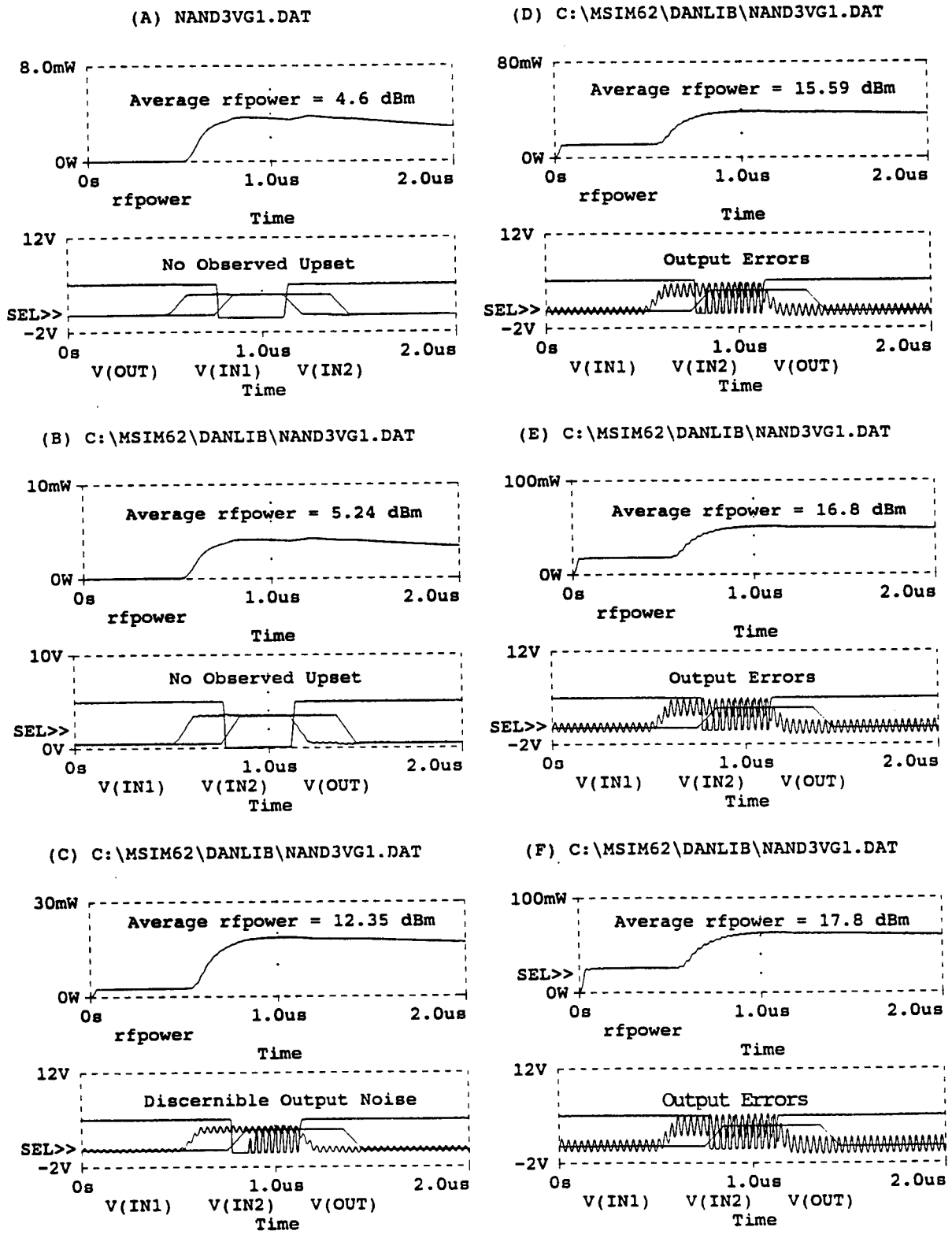
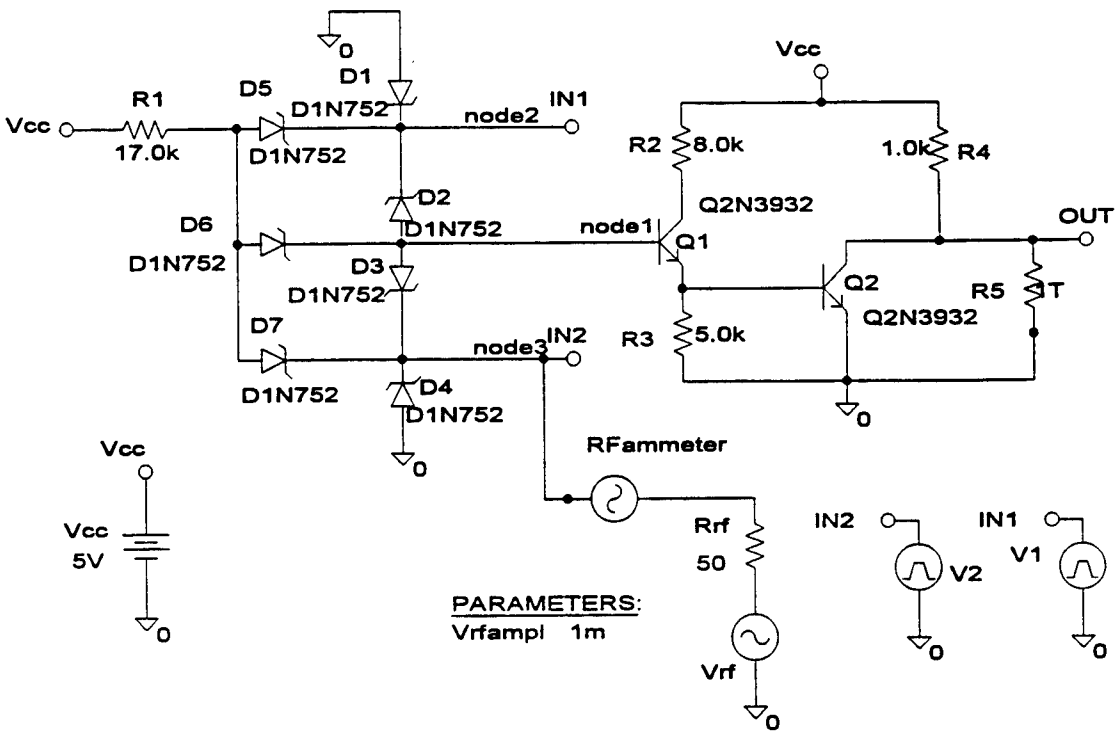


Figure 3-14 Susceptibility Threshold Build-Up



54ALS03 NAND GATE: 10MHZ @ LOGIC IN2

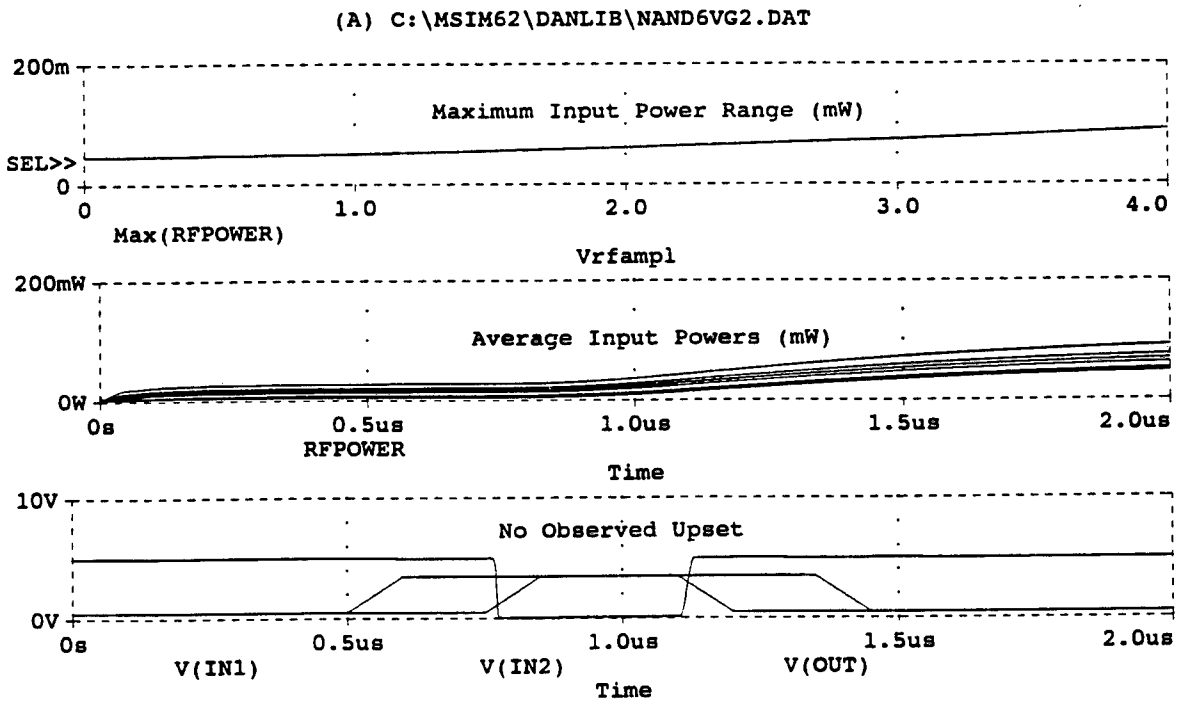


Figure 3-15 10 MHz Voltage Source in Parallel with LOGIC IN2

```
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     CIRCUIT DESCRIPTION

**********************************************************************
************



* Schematics Version 6.2 - April 1995
* Mon Jul 22 11:22:36 1996

.PARAM         Vrfampl=1m

** Analysis setup **
.tran .1us 2us 0 1n
.four 10MEG 3 v([out])
.OPTIONS NODE
.STEP  PARAM Vrfampl LIST
+ 1m 100m 1 2 2.5 3 4


* From [SCHEMATICS NETLIST] section of msim.ini:
.lib C:\MSIM62\LIB\MAGNETIC.LIB
.lib nom.lib

.INC "NAND1VGS.net"

**** INCLUDING NAND1VGS.net ****
* Schematics Netlist *



D_D8          0 IN1 D1N752
D_D9          $N_0001 IN1 D1N752
D_D10          $N_0001 IN2 D1N752
D_D11          0 IN2 D1N752
D_D12          $N_0002 IN1 D1N752
D_D13          $N_0002 $N_0001 D1N752
D_D14          $N_0002 IN2 D1N752
R_R6          Vcc $N_0002  17.0k
R_R7          $N_0003 Vcc  8.0k
R_R8          0 $N_0004  5.0k
R_R9          Vcc OUT  1.0k
```

Figure 3-16 (a) Simulation Output File

```
Q_Q3          $N_0003 $N_0001 $N_0004 Q2N3932
Q_Q4          OUT $N_0004 0 Q2N3932
V_Vcc          Vcc 0 5V
V_V2          IN2 0
+PULSE .5 3.5 .75u 0 0 .5u 1s
R_Rrf          $N_0006 $N_0005  50
V_Vrf          $N_0005 0
+SIN 0 {Vrfampl} 10MEG 0 0 0
V_V1          IN1 0
+PULSE .5 3.5 .5u 0 0 .5u 1s
R_R10          0 OUT  1T
V_RFameter          $N_0001 $N_0006
+SIN 0 0 10MEG 0 0 0

**** RESUMING NAND1VGS.CIR ****
.INC "NAND1VGS.als"

**** INCLUDING NAND1VGS.als ****
* Schematics Aliases *

.ALIASES
D_D8              D8(1=0 2=IN1 )
D_D9              D9(1=$N_0001 2=IN1 )
D_D10             D10(1=$N_0001 2=IN2 )
D_D11             D11(1=0 2=IN2 )
D_D12             D12(1=$N_0002 2=IN1 )
D_D13             D13(1=$N_0002 2=$N_0001 )
D_D14             D14(1=$N_0002 2=IN2 )
R_R6              R6(1=Vcc 2=$N_0002 )
R_R7              R7(1=$N_0003 2=Vcc )
R_R8              R8(1=0 2=$N_0004 )
R_R9              R9(1=Vcc 2=OUT )
Q_Q3              Q3(c=$N_0003 b=$N_0001 e=$N_0004 )
Q_Q4              Q4(c=OUT b=$N_0004 e=0 )
V_Vcc             Vcc(+=Vcc -=0 )
V_V2              V2(+=IN2 -=0 )
R_Rrf             Rrf(1=$N_0006 2=$N_0005 )
V_Vrf             Vrf(+=$N_0005 -=0 )
V_V1              V1(+=IN1 -=0 )
R_R10             R10(1=0 2=OUT )
V_RFameter            RFameter(+=$N_0001 -=$N_0006 )
_     _(OUT=OUT)
_     _(Vcc=Vcc)
_     _(IN2=IN2)
_     _(IN1=IN1)
.ENDALIASES


**** RESUMING NAND1VGS.CIR ****
```

Figure 3-16 (b) Simulation Output File, cont'd.

```
.probe

.END
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     ELEMENT NODE TABLE

********************************************************************************
************

0               D_D8            Q_Q4            R_R8            V_V1            V_V2
                D_D11           R_R10           V_Vcc           V_Vrf

IN1             D_D8            D_D9            V_V1            D_D12

IN2             V_V2            D_D10           D_D11           D_D14

out             Q_Q4            R_R9            R_R10

Vcc             R_R6            R_R7            R_R9            V_Vcc

$N_0001         D_D9            Q_Q3            D_D10           D_D13           V_RFame
ter

$N_0002         R_R6            D_D12           D_D13           D_D14

$N_0003         Q_Q3            R_R7

$N_0004         Q_Q3            Q_Q4            R_R8

$N_0005         R_Rrf           V_Vrf

$N_0006         R_Rrf           V_RFameter
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     Diode MODEL PARAMETERS
```

Figure 3-16 (c) Simulation Output File, cont'd.

```
**********************************************************************
************



              D1N752
          IS    1.154000E-15
         ISR    1.625000E-09
          BV    5.6
         IBV     .062583
         NBV     .62382
        IBVL  631.960000E-06
        NBVL   50
          RS     .9471
         CJO  150.000000E-12
          VJ     .75
           M     .5788
        TBV1  267.860000E-06

▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH


 ****     BJT MODEL PARAMETERS


**********************************************************************
************



              Q2N3932
              NPN
          IS   69.280000E-18
          BF   285
          NF    1
         VAF   100
         IKF     .02192
         ISE   69.280000E-18
          NE    1.176
          BR    1.179
          NR    1
          RB   10
         RBM   10
```

Figure 3-16 (d) Simulation Output File, cont'd.

```
 RC    4
CJE  939.800000E-15
MJE     .3453
CJC  893.100000E-15
MJC     .3017
 TF  141.100000E-12
XTF   30
VTF   10
ITF     .27
 TR    1.588000E-09
XTB    1.5

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                     PARAM VRFAMPL =    1.00
00E-03

**********************************************************************
************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)     .5000  (  IN2)     .5000  (  out)    5.0000  (  Vcc)
  5.0000

($N_0001)     .0140                  ($N_0002)     .6649

($N_0003)    5.0000                  ($N_0004) 47.45E-09

($N_0005)    0.0000                  ($N_0006)     .0140


    VOLTAGE SOURCE CURRENTS
```

Figure 3-16 (e) Simulation Output File, cont'd.

```
    NAME          CURRENT

    V_Vcc        -2.550E-04
    V_V2         -2.433E-05
    V_Vrf         2.792E-04
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH


 ****     FOURIER ANALYSIS                    TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                        PARAM VRFAMPL =    1.00
00E-03

*******************************************************************
************


FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)


 DC COMPONENT =    5.000000E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE         NOR
MALIZED
    NO          (HZ)      COMPONENT     COMPONENT     (DEG)         PHAS
E (DEG)

     1      1.000E+07     4.928E-06     1.000E+00     9.643E+01     0.0
00E+00
     2      2.000E+07     9.646E-09     1.957E-03     2.374E+01    -7.2
69E+01
     3      3.000E+07     4.258E-08     8.642E-03    -4.476E+01    -1.4
12E+02


     TOTAL HARMONIC DISTORTION =    8.860569E-01 PERCENT

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
```

Figure 3-16 (f) Simulation Output File, cont'd.

```
# 77047 ****
 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000
DEG C
 ****     CURRENT STEP                     PARAM VRFAMPL =     .1


********************************************************************************
************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)     .5000  (  IN2)     .5000  (  out)    5.0000  (  Vcc)
  5.0000
($N_0001)     .0140                  ($N_0002)     .6649

($N_0003)    5.0000                  ($N_0004) 47.45E-09

($N_0005)    0.0000                  ($N_0006)     .0140



    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V_Vcc        -2.550E-04
    V_V2         -2.433E-05
    V_Vrf         2.792E-04
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****
```

Figure 3-16 (g) Simulation Output File, cont'd.

```
 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     FOURIER ANALYSIS                    TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                        PARAM VRFAMPL =     .1


*******************************************************************
************


FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)


 DC COMPONENT =   4.999999E+00

 HARMONIC   FREQUENCY    FOURIER    NORMALIZED    PHASE         NOR
MALIZED
    NO          (HZ)     COMPONENT    COMPONENT    (DEG)        PHAS
E (DEG)

     1     1.000E+07    4.979E-04    1.000E+00    9.639E+01     0.0
00E+00
     2     2.000E+07    6.242E-06    1.254E-02   -1.174E+02    -2.1
38E+02
     3     3.000E+07    7.922E-07    1.591E-03    3.264E+01    -6.3
76E+01

     TOTAL HARMONIC DISTORTION =   1.263628E+00 PERCENT
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     INITIAL TRANSIENT SOLUTION          TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                        PARAM VRFAMPL =    1


*******************************************************************
************
```

Figure 3-16 (h) Simulation Output File, cont'd.

```
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)     .5000  (  IN2)     .5000  (  out)    5.0000  (  Vcc)
  5.0000

($N_0001)     .0140                  ($N_0002)     .6649

($N_0003)    5.0000                  ($N_0004) 47.45E-09

($N_0005)    0.0000                  ($N_0006)     .0140


    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V_Vcc        -2.550E-04
    V_V2         -2.433E-05
    V_Vrf         2.792E-04
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     FOURIER ANALYSIS                 TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                     PARAM VRFAMPL =    1


**********************************************************************
************
```

Figure 3-16 (i) Simulation Output File, cont'd.

```
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)


 DC COMPONENT =    4.999991E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE         NOR
MALIZED
    NO          (HZ)      COMPONENT     COMPONENT     (DEG)         PHAS
E (DEG)

     1      1.000E+07     5.111E-03     1.000E+00     9.573E+01     0.0
00E+00
     2      2.000E+07     7.985E-04     1.562E-01    -1.283E+02    -2.2
40E+02
     3      3.000E+07     2.219E-04     4.342E-02     2.628E+01    -6.9
45E+01


     TOTAL HARMONIC DISTORTION =    1.621584E+01 PERCENT
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****      INITIAL TRANSIENT SOLUTION       TEMPERATURE =    27.000
DEG C

 ****      CURRENT STEP                     PARAM VRFAMPL =     2


**********************************************************************
************


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)      .5000  (  IN2)      .5000  (  out)     5.0000  (  Vcc)
  5.0000

($N_0001)      .0140                   ($N_0002)      .6649

($N_0003)     5.0000                   ($N_0004)  47.45E-09
```

Figure 3-16 (j) Simulation Output File, cont'd.

```
($N_0005)     0.0000                    ($N_0006)      .0140


    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V_Vcc        -2.550E-04
    V_V2         -2.433E-05
    V_Vrf         2.792E-04
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     FOURIER ANALYSIS                    TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                        PARAM VRFAMPL =    2


*******************************************************************
************


FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)


 DC COMPONENT =   4.999982E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE          NOR
MALIZED
    NO          (HZ)      COMPONENT     COMPONENT     (DEG)          PHAS
E (DEG)

     1     1.000E+07     1.048E-02     1.000E+00     7.024E+01      0.0
00E+00
```

Figure 3-16 (k) Simulation Output File, cont'd.

```
     2      2.000E+07     6.447E-03     6.153E-01    -1.593E+02    -2.2
96E+02
     3      3.000E+07     2.776E-03     2.650E-01     2.972E+01    -4.0
53E+01

     TOTAL HARMONIC DISTORTION =   6.699384E+01 PERCENT
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                     PARAM VRFAMPL =    2.5


**********************************************************************
************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)      .5000  (  IN2)      .5000  (  out)    5.0000  (  Vcc)
  5.0000

($N_0001)     .0140                    ($N_0002)     .6649

($N_0003)    5.0000                    ($N_0004) 47.45E-09

($N_0005)    0.0000                    ($N_0006)     .0140



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_Vcc       -2.550E-04
    V_V2        -2.433E-05
    V_Vrf        2.792E-04
```

Figure 3-16 (l) Simulation Output File, cont'd.

```
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     FOURIER ANALYSIS                    TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                        PARAM VRFAMPL =    2.5


**********************************************************************
************


FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)


 DC COMPONENT =   4.999976E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE          NOR
MALIZED
    NO          (HZ)      COMPONENT     COMPONENT     (DEG)          PHAS
E (DEG)

     1      1.000E+07     1.268E-02     1.000E+00     7.113E+01      0.0
00E+00
     2      2.000E+07     7.089E-03     5.591E-01    -1.561E+02     -2.2
73E+02
     3      3.000E+07     1.771E-03     1.397E-01     1.702E+01     -5.4
11E+01

     TOTAL HARMONIC DISTORTION =   5.762982E+01 PERCENT
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

  * C:\MSIM62\DANLIB\NAND1VGS.SCH
```

Figure 3-16 (m) Simulation Output File, cont'd.

```
 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000
DEG C

 ****     CURRENT STEP                     PARAM VRFAMPL =     3


**************************************************************************
************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE

(  IN1)     .5000  (  IN2)     .5000  (  out)    5.0000  (  Vcc)
  5.0000

($N_0001)     .0140                   ($N_0002)     .6649

($N_0003)    5.0000                   ($N_0004) 47.45E-09

($N_0005)    0.0000                   ($N_0006)     .0140



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_Vcc       -2.550E-04
    V_V2        -2.433E-05
    V_Vrf        2.792E-04
    V_V1        -2.433E-05
    V_RFameter   2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH


 ****     FOURIER ANALYSIS                 TEMPERATURE =   27.000
DEG C
```

Figure 3-16 (n) Simulation Output File, cont'd.

```
****     CURRENT STEP                                PARAM VRFAMPL =     3

**********************************************************************
************

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)

 DC COMPONENT =    4.999973E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE          NOR
MALIZED
    NO          (HZ)      COMPONENT     COMPONENT     (DEG)          PHAS
E (DEG)
     1      1.000E+07     1.416E-02     1.000E+00     7.462E+01      0.0
00E+00
     2      2.000E+07     7.222E-03     5.101E-01    -1.590E+02     -2.3
37E+02
     3      3.000E+07     2.314E-03     1.634E-01    -1.897E+01     -9.3
59E+01

     TOTAL HARMONIC DISTORTION =    5.356340E+01 PERCENT
▒
**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =    27.000
DEG C

 ****     CURRENT STEP                                PARAM VRFAMPL =     4

**********************************************************************
************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   V
OLTAGE
```

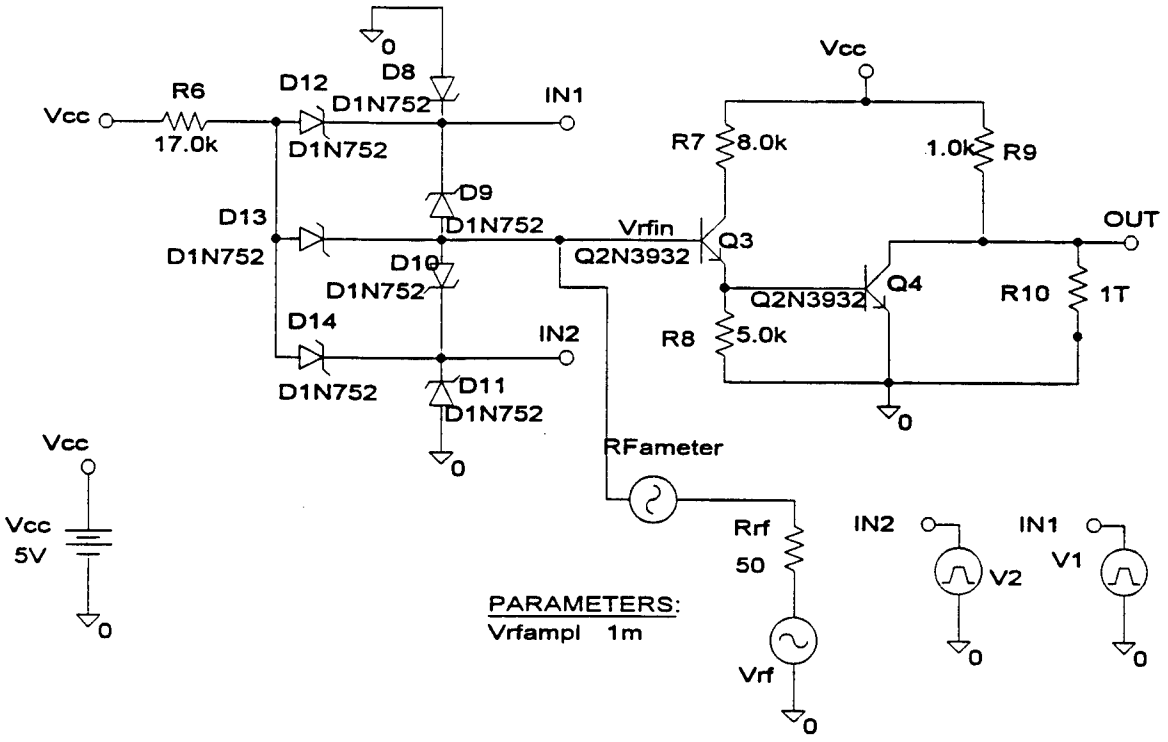
Figure 3-16 (o) Simulation Output File, cont'd.

```
(  IN1)      .5000   (  IN2)      .5000   (  out)     5.0000   (  Vcc)
  5.0000

($N_0001)      .0140                     ($N_0002)      .6649

($N_0003)     5.0000                     ($N_0004) 47.45E-09

($N_0005)     0.0000                     ($N_0006)      .0140



    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V_Vcc        -2.550E-04
    V_V2         -2.433E-05
    V_Vrf         2.792E-04
    V_V1         -2.433E-05
    V_RFameter    2.792E-04

    TOTAL POWER DISSIPATION   1.30E-03  WATTS

**** 07/22/96 15:22:39 **** Win32s PSpice 6.2 (April 1995) **** ID
# 77047 ****

 * C:\MSIM62\DANLIB\NAND1VGS.SCH


 ****      FOURIER ANALYSIS                    TEMPERATURE =   27.000
DEG C

 ****      CURRENT STEP                        PARAM VRFAMPL =     4


*****************************************************************
************


FOURIER COMPONENTS OF TRANSIENT RESPONSE V(out)
```

Figure 3-16 (p) Simulation Output File, cont'd.

```
 DC COMPONENT =    4.999911E+00

 HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE          NOR
MALIZED
    NO          (HZ)       COMPONENT     COMPONENT     (DEG)         PHAS
E (DEG)

     1      1.000E+07     1.647E-02     1.000E+00     8.125E+01      0.0
00E+00
     2      2.000E+07     8.485E-03     5.152E-01    -1.686E+02     -2.4
99E+02
     3      3.000E+07     4.548E-03     2.761E-01    -2.312E+01     -1.0
44E+02

      TOTAL HARMONIC DISTORTION =    5.844951E+01 PERCENT

           JOB CONCLUDED

           TOTAL JOB TIME            104.19
```

Figure 3-16 (q) Simulation Output File, cont'd.



54ALS03 NAND GATE: 10MHZ @ INVERTER INPUT

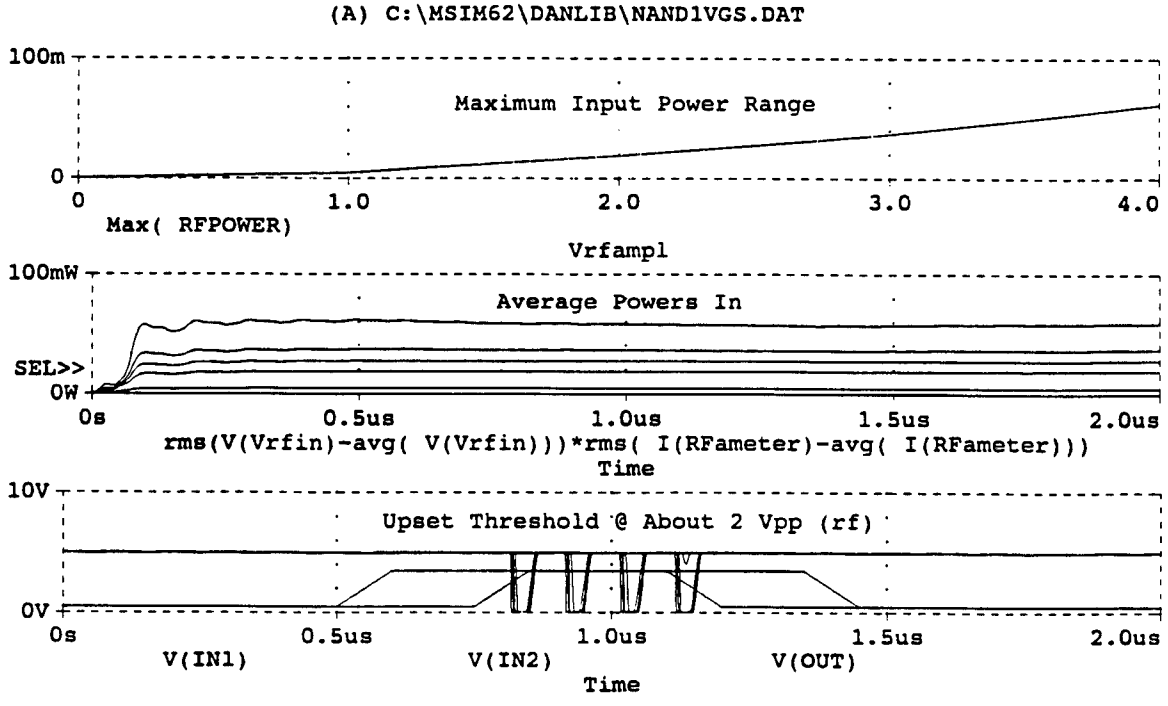


Figure 3-17 10 MHz Voltage Source at Inverter Input

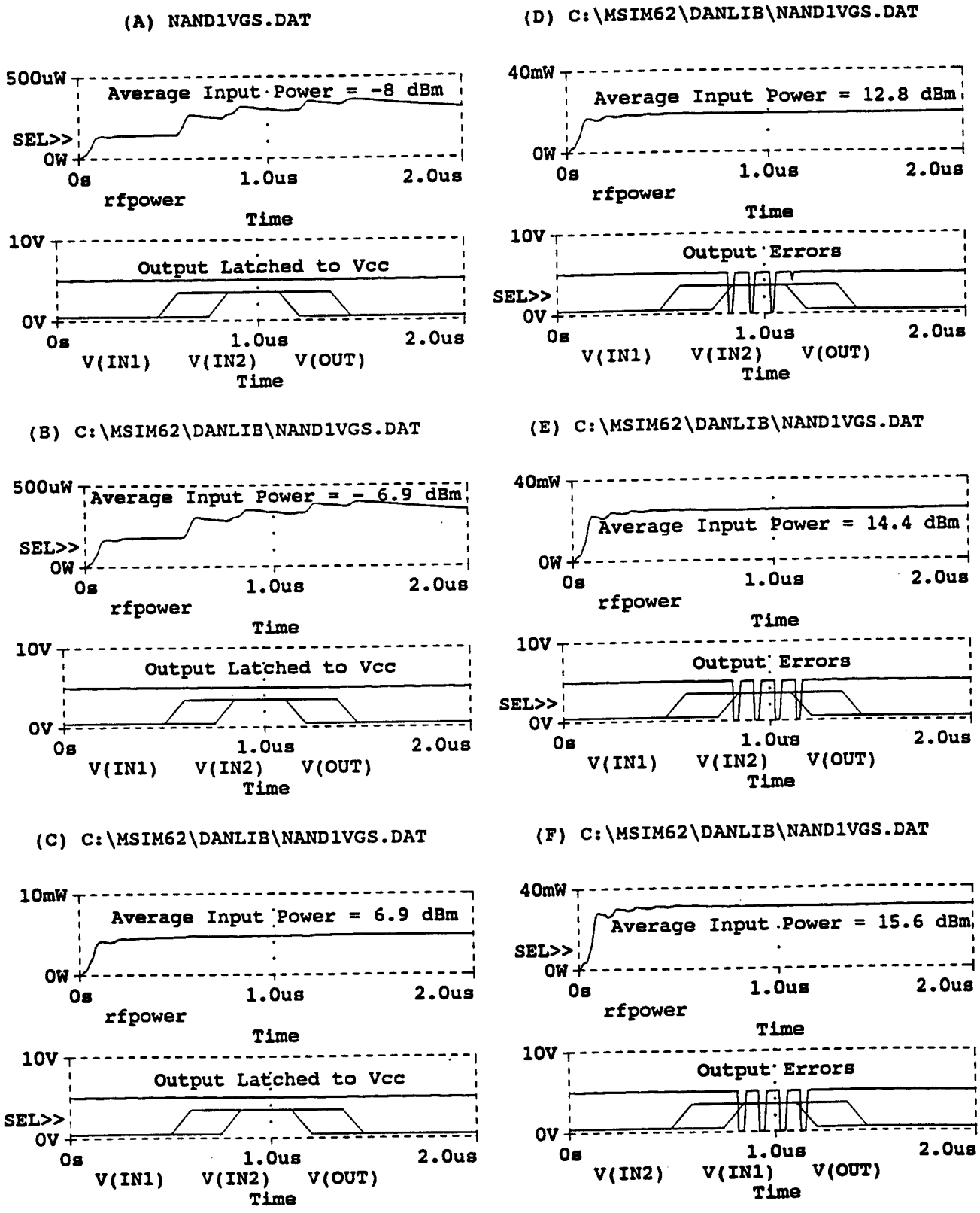


Figure 3-18 First Cull Susceptibility Thresholds

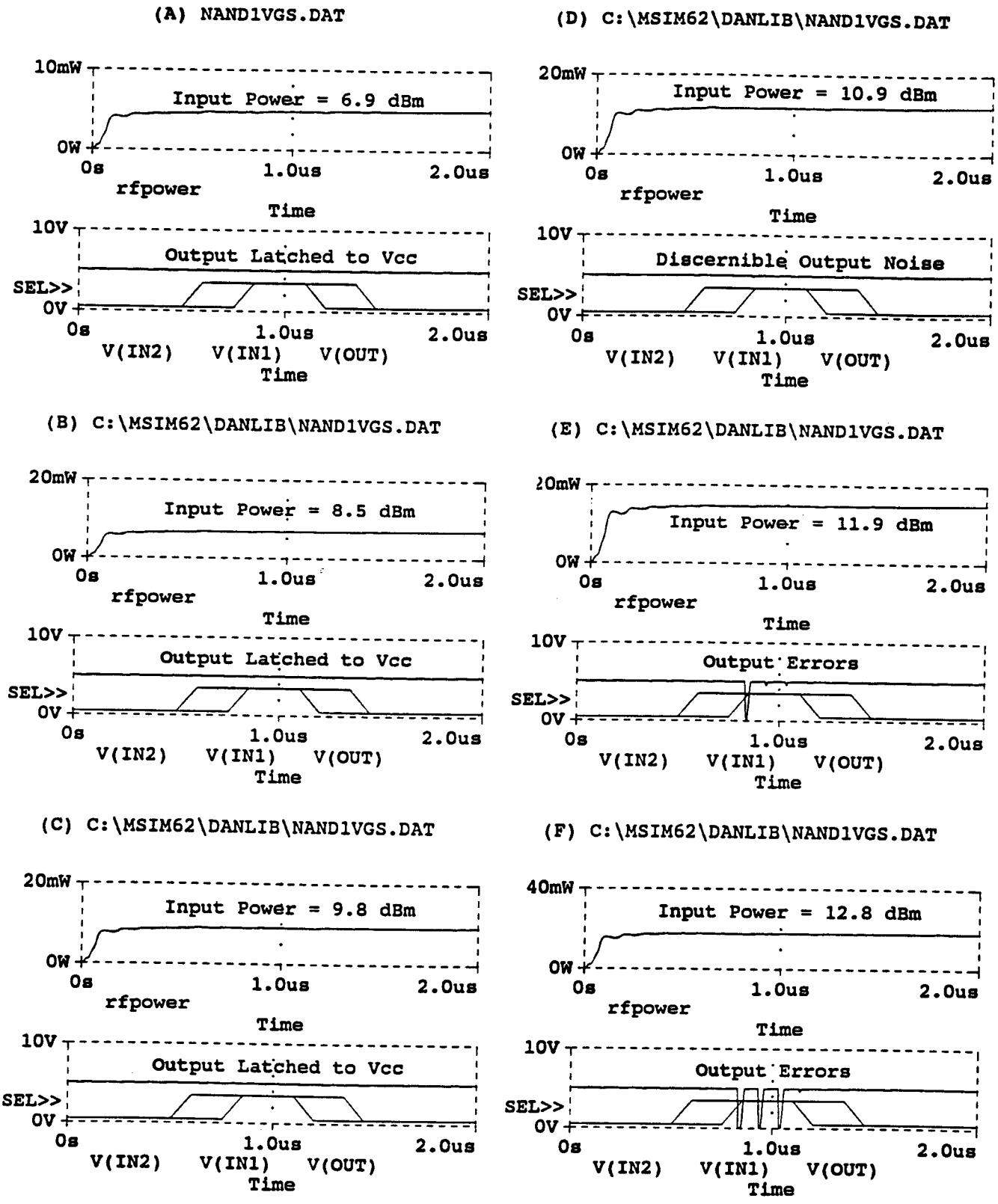
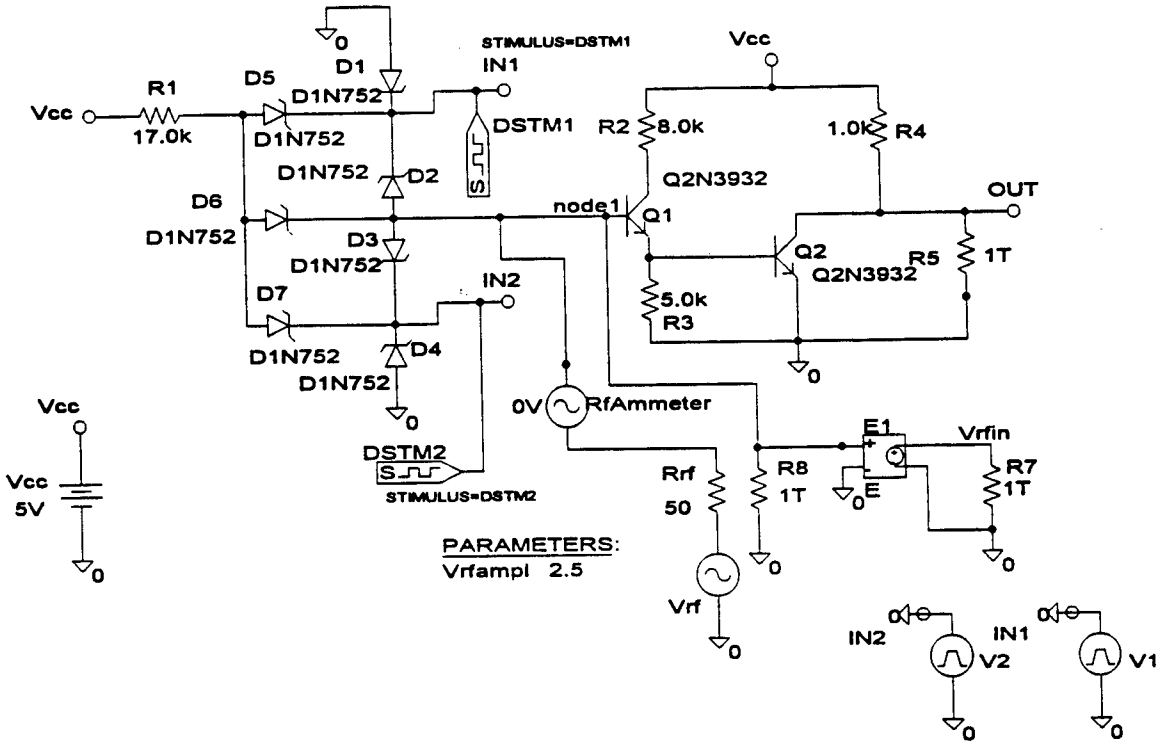


Figure 3-19 Detail Susceptibility Threshold Build-Up



54ALS03 NAND GATE: 20MHZ @ INVERTER INPUT

(A) C:\MSIM62\DANLIB\NAND2VGS.DAT

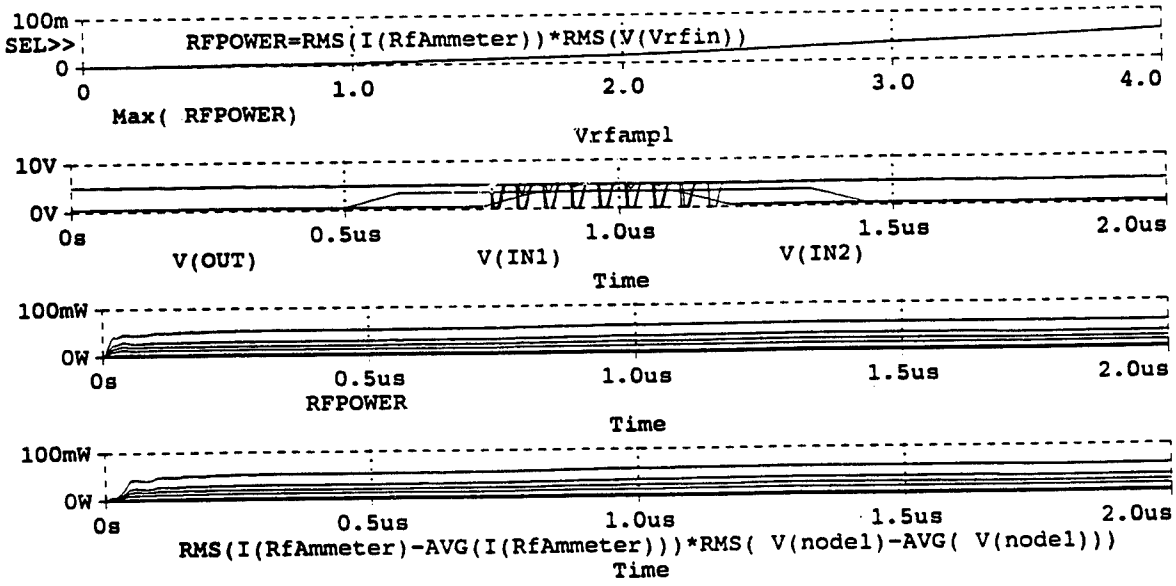


Figure 3-20 20 MHz Voltage Source at Inverter Input

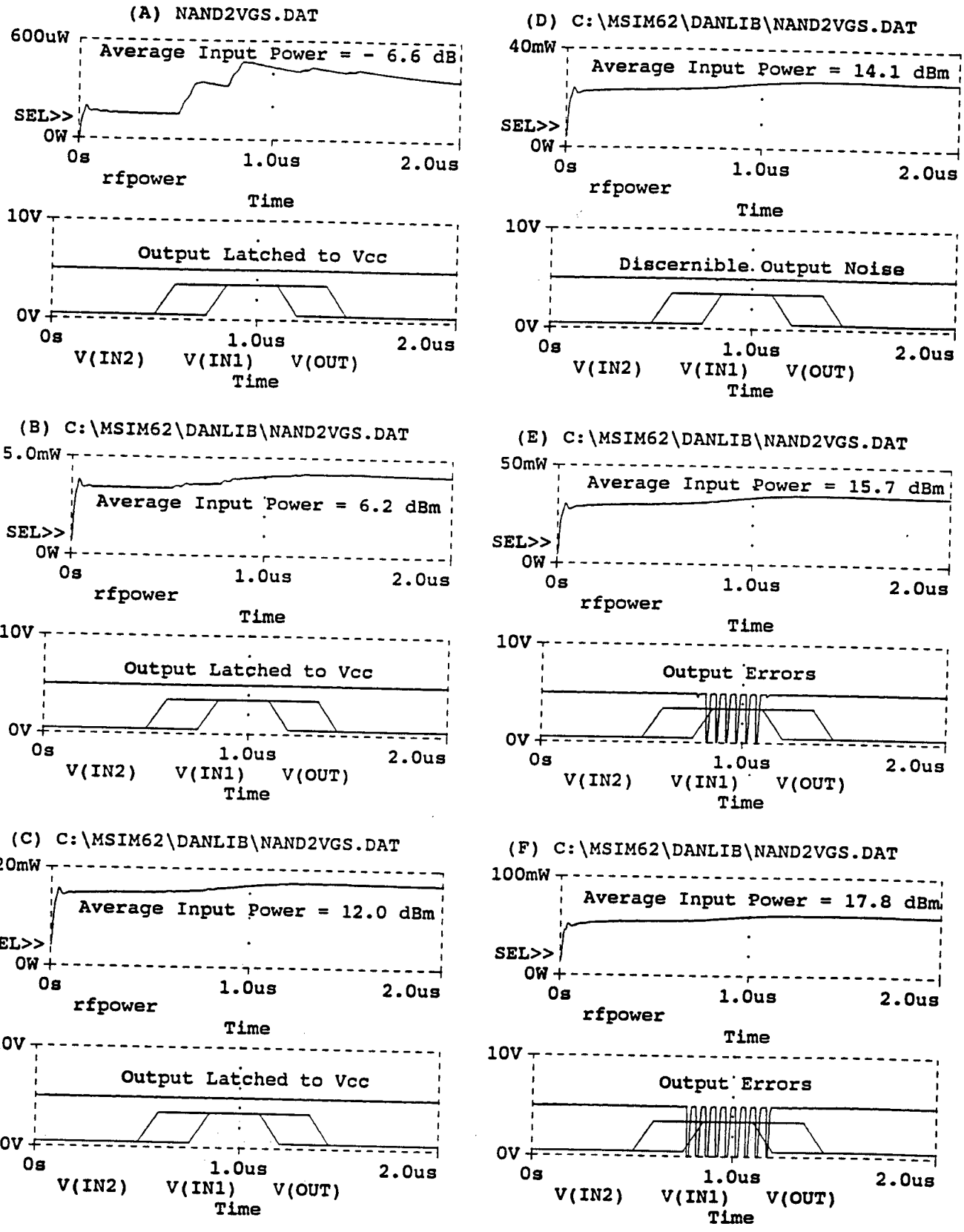


Figure 3-21 First Cull Susceptibility Thresholds

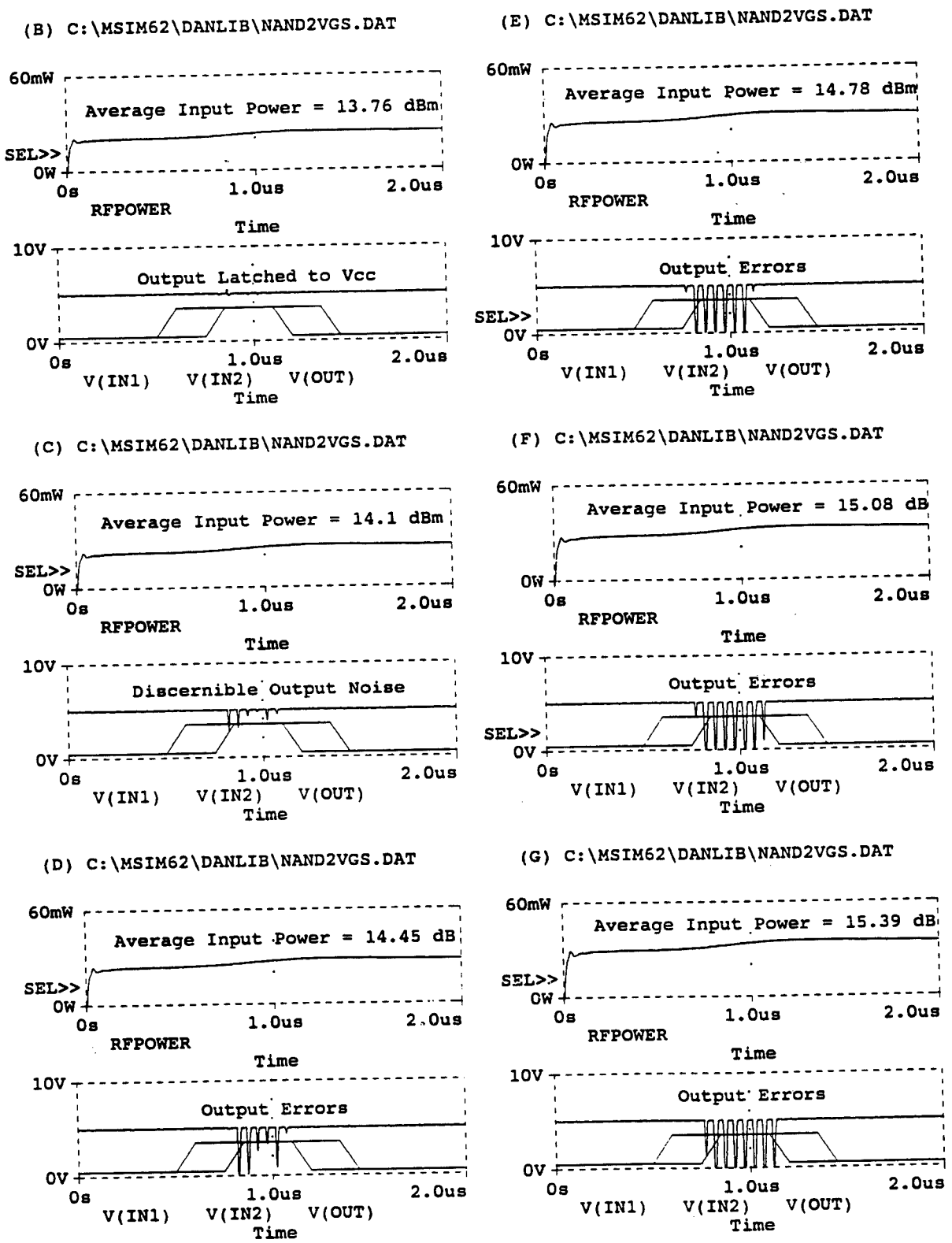


Figure 3-22 Detail Susceptibility Threshold Build-Up

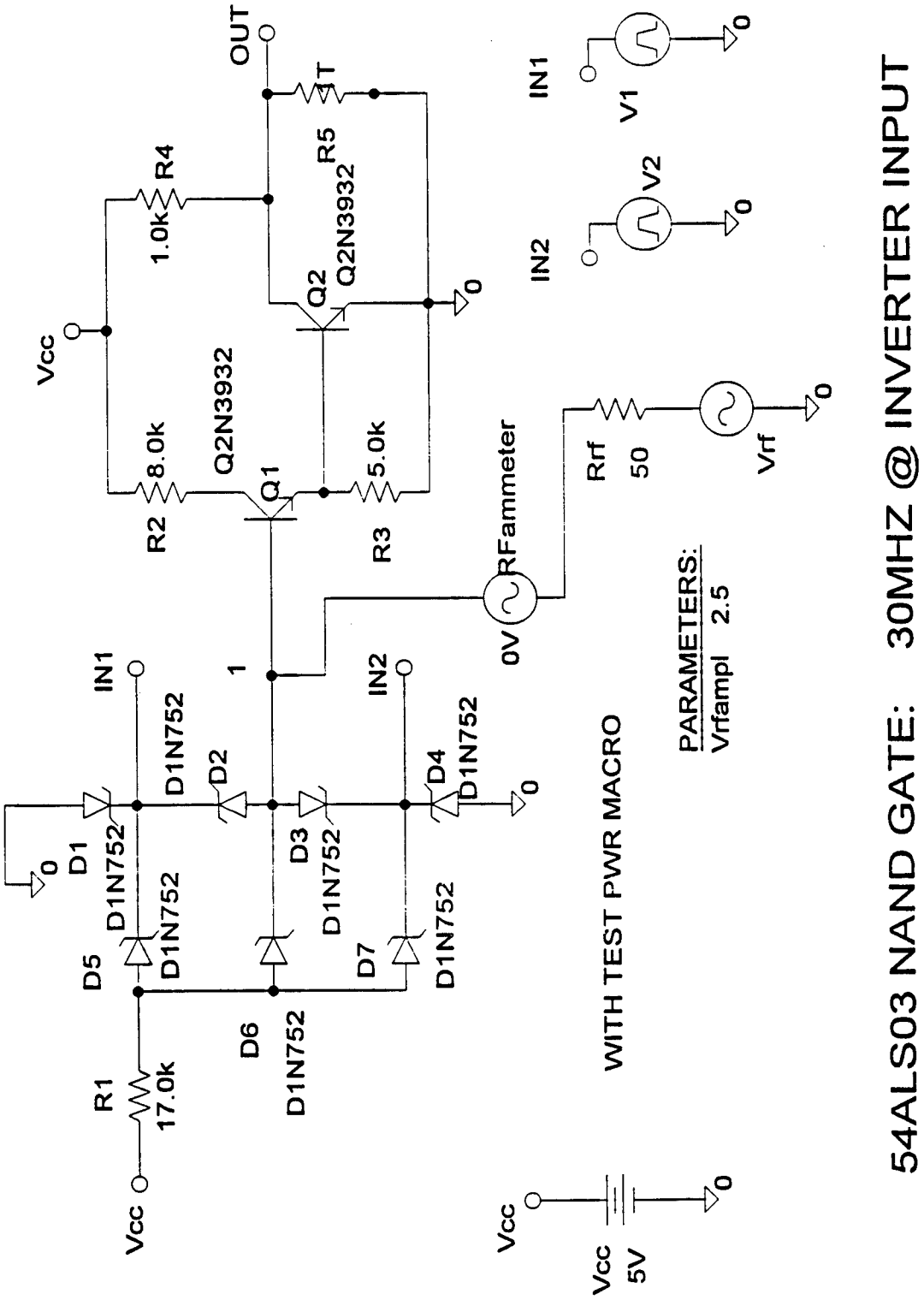


Figure 3-23 30 MHz Voltage Source at Inverter Input

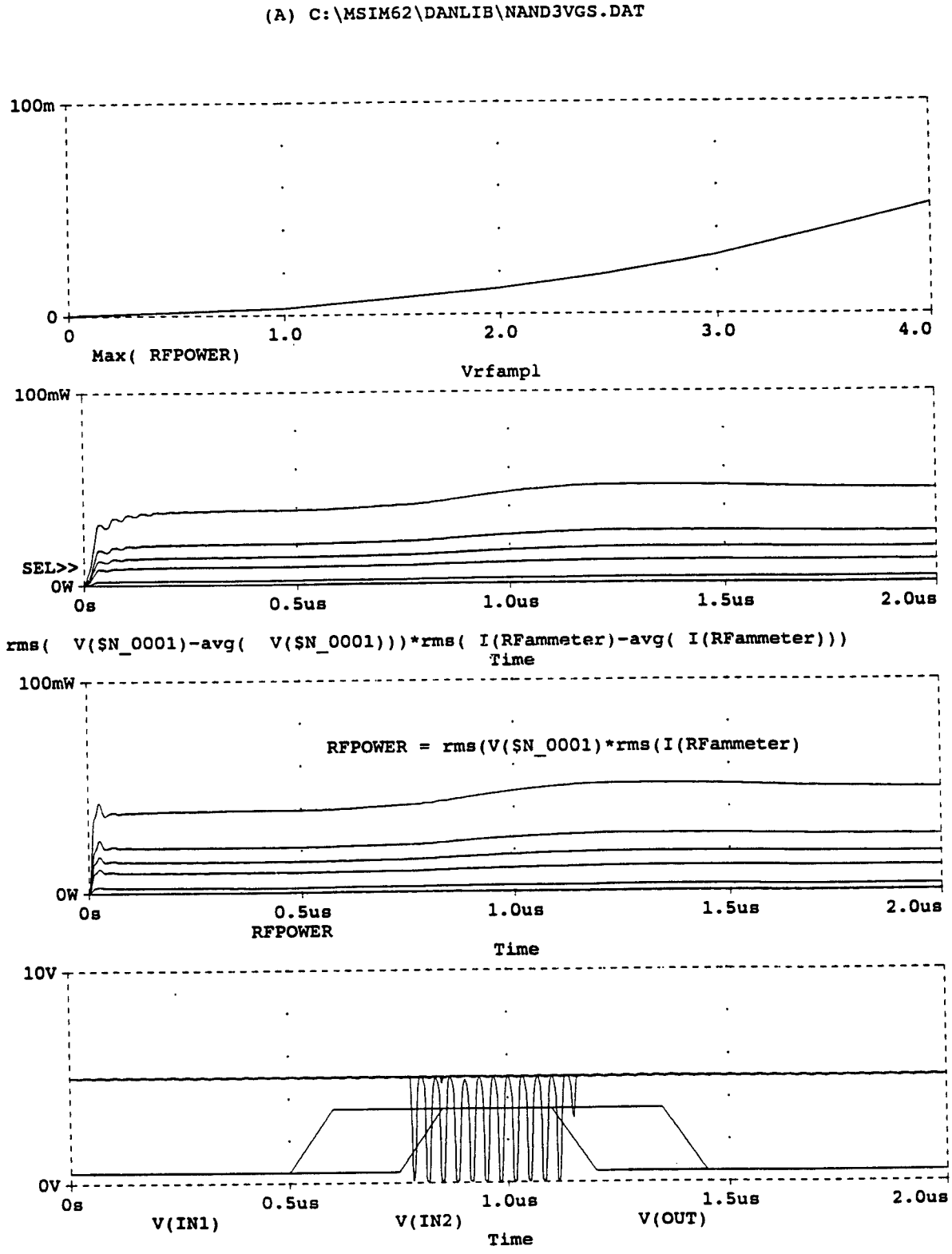


Figure 3-24 First Cull Susceptibility Thresholds

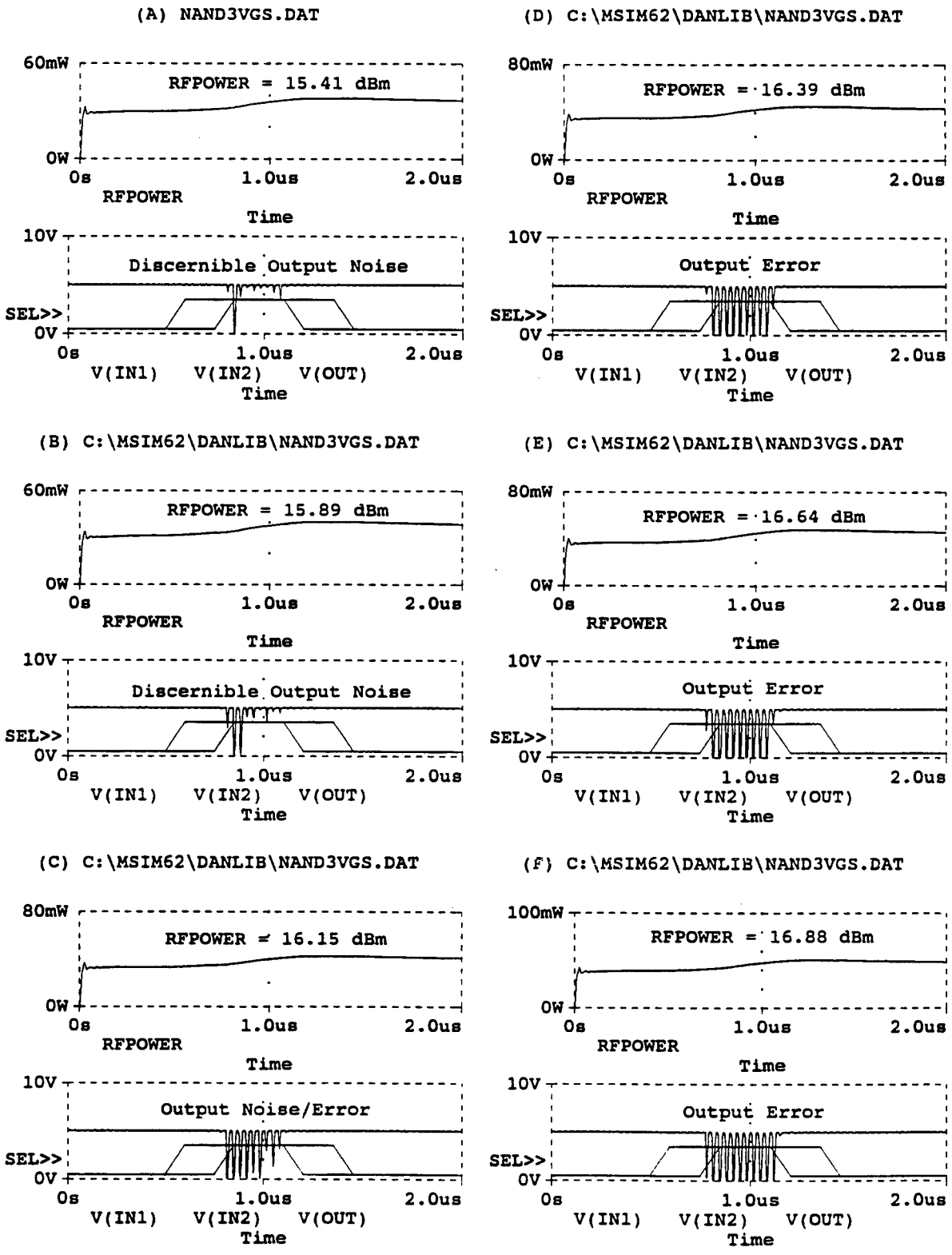


Figure 3-25 Detail Susceptibility Threshold Build-Up

4. DS7820 DIFFERENTIAL LINE RECEIVERS

The National Semiconductor, DS7820 dual differential line receivers are dual circuits on a single monolithic IC chip where the two halves use a common power supply and ground. They are designed to sense small differential signals in the presence of large common-mode noise signals. There are two input channels for both inverting and noninverting inputs. These devices are TTL-compatible and provide output signals as a function of polarity of the differential input voltage. The outputs go high when the inputs are open-circuited. A strobe port is also provided which when driven low disables the receiver and sets the output ports high. Response time control ports are also provided for each channel and can be used to dc isolate resistive terminations of twisted pair, wire transmission lines and to otherwise shape the overall frequency response. These circuits are made to be directly interchangeable with Texas Instruments differential line receiver devices, SN55182 and SN75182. The device logic is as follows: output H when strobe L and differential input X; output H when strobe H and differential input H; output L when strobe H and differential input L.

Figures 4-1 and 4-2 show the baseline circuits and their logic responses for pulse inputs at both noninverting and inverting ports, respectively. In these runs, the sampling strobe was set high and the response time control port open. Figure 4-3 shows the noninverting receiver being driven by a 10 MHz voltage source in parallel with its Vcc bias rail. As indicated, no output upset responses were observed for input power levels up to 3 uW. Since other sources [1] have suggested rf susceptibility levels of 20 dBm from 1 - 100 MHz are needed to cause upset, the rf power sweep in the above run was apparently not set high enough to drive the device into upset.

Figure 4-4 shows the noninverting receiver being driven by a 10 MHz voltage source in series with its Vcc bias rail. First cull data shows apparent noise ripple and upset errors. Figure 4-5 show detail data of the susceptibility threshold build-up; noise ripple begins at about 6.1 dBm and upset errors are added at about 8.7 dBm. Figure 4-6 shows the noninverting receiver being driven by a 20

MHz voltage source in series with its Vcc bias rail. Noise ripple and upset errors are evident in the culling power sweep from 4 mW to 25 mW. Figure 4-7 shows detail data of the susceptibility threshold build-up. While most of the noise ripple is outside the desired signal time width, this could present a problem of excessive noise margins to succeeding logic. Note that nearly 11.4 dBm is needed to drive the output pulse into "some" level of bit error. Figure 4-8 shows the noninverting receiver being driven by a 40 MHz voltage source in series with its Vcc bias rail. Again, noise ripple and upset errors are evident in the culling power sweep from 4 mW to 40 mW. Figure 4-9 shows detail data of the susceptibility threshold build-up. Again, most of the noise ripple is outside the desired signal time width and nearly 13.6 dBm is needed to drive the output pulse into "some" level of bit error. These data suggest that noise ripple and upset error require more EM power as the frequency increases; i.e., the susceptibility of the Vcc pin to a series driven, cw EM source decreases as the source frequency increases. These results are consistent with previously published data [2].

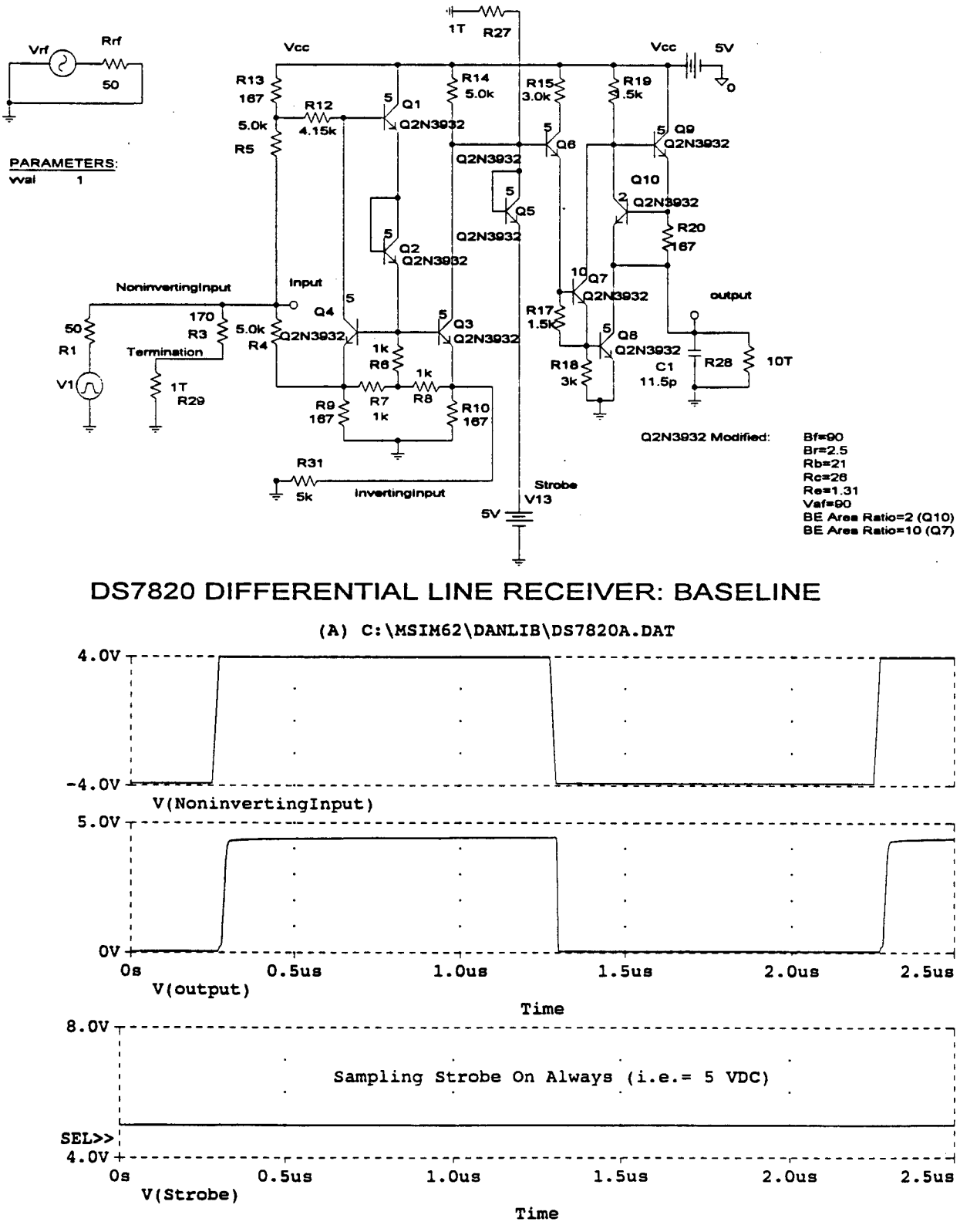
Figure 4-10 shows the noninverting receiver being driven by a 10 MHz voltage source in parallel with the noninverting input port. Resistor R42 at 1 uohm is used to define better the EM entry port and to provide node isolation for ERC. As is evident in the power range from 10 mW to 75 mW, there is considerable ripple noise and upset error. Figure 4-11 show detail data of the susceptibility threshold build-up; there is discernible noise ripple at about 11.23 dBm and upset errors are added at about 13.2 dBm. With the input rf power at 17 dBm, the ripple noise and upset errors are both considerable. Figure 4-12 shows the noninverting receiver being driven by a 20 MHz voltage source in parallel with the noninverting input port. In the power range from 10 mW to 75 mW, there are ripple noise and upset errors. Figure 4-13 show detail data of the susceptibility threshold build-up; there is discernible noise ripple at about 11.23 dBm and upset errors are added at about 15.23 dBm. Figure 4-14 shows shows the noninverting receiver being driven by a 40 MHz voltage source in parallel with the noninverting input port. In this power range, there seems to be

no upset errors, only ripple noise outside the time width of the output pulse. Figure 4-15 shows detail data in the power range from 13 mW to 50 mW. Noise ripple is evident throughout the sweep but no upset errors are observed.

This latter run at rf frequency at 40 MHz indicating no upset is of interest. If the conjecture that the device susceptibility is decreasing with increasing frequency is correct (i.e. more rf power is needed to cause upset), then no upset data were observed because perhaps the rf power range in this run was not set high enough to drive the device into upset. If the conjecture is incorrect, these data at 40 MHz are anomalous. Further, it may be of interest to note that runs were also made on this device with cw EM in series with the noninverting input port. No upsets were observed for rf power sweeps in source available powers from - 2 dBm to 31.5 dBm.

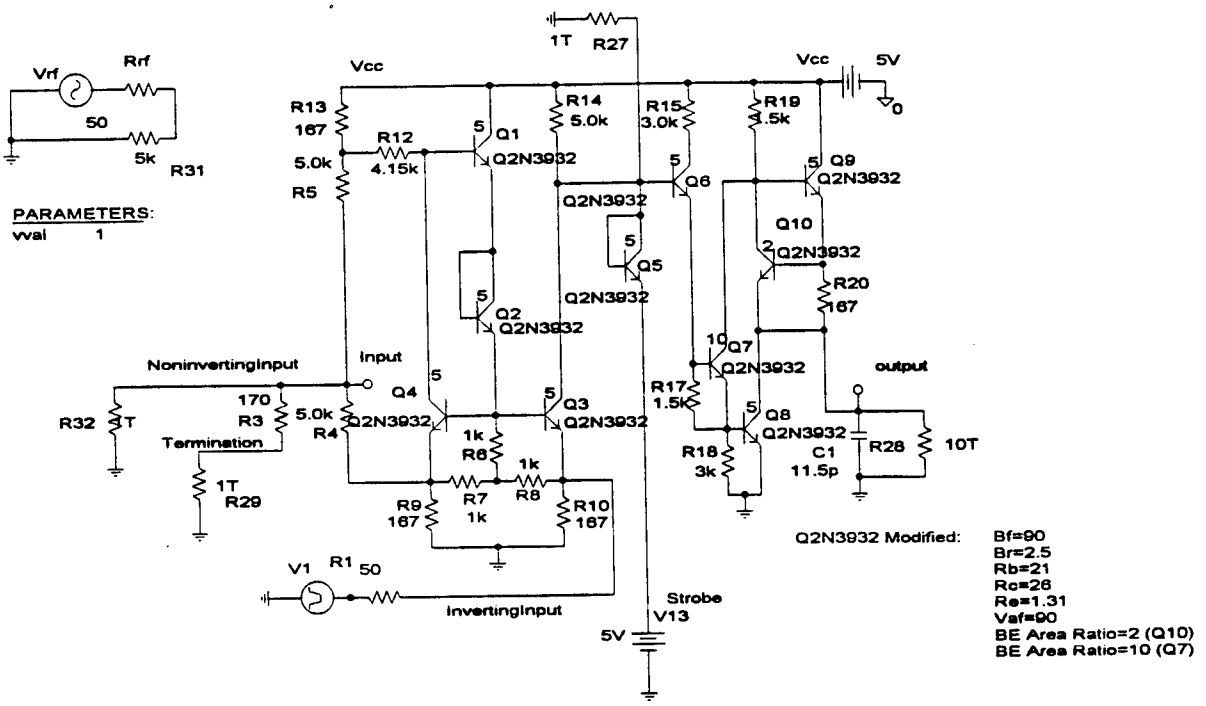
[1] Rohrbaugh, John P. and Pursley, Randall H., "X-Band T/R Module Conducted Interference Simulation and Measurements", Georgia Institute of Technology, Final Report, June 1992; Summer Research Program for Rome Laboratory, Air Force Office of Scientific Research, Bolling Air Force Base, Washington, DC.

[2] Ibid.



DS7820 DIFFERENTIAL LINE RECEIVER: BASELINE

Figure 4-1 DS7820 Differential Line Receiver; Noninverting Baseline



DS7820 DIFFERENTIAL LINE RECEIVER: BASELINE

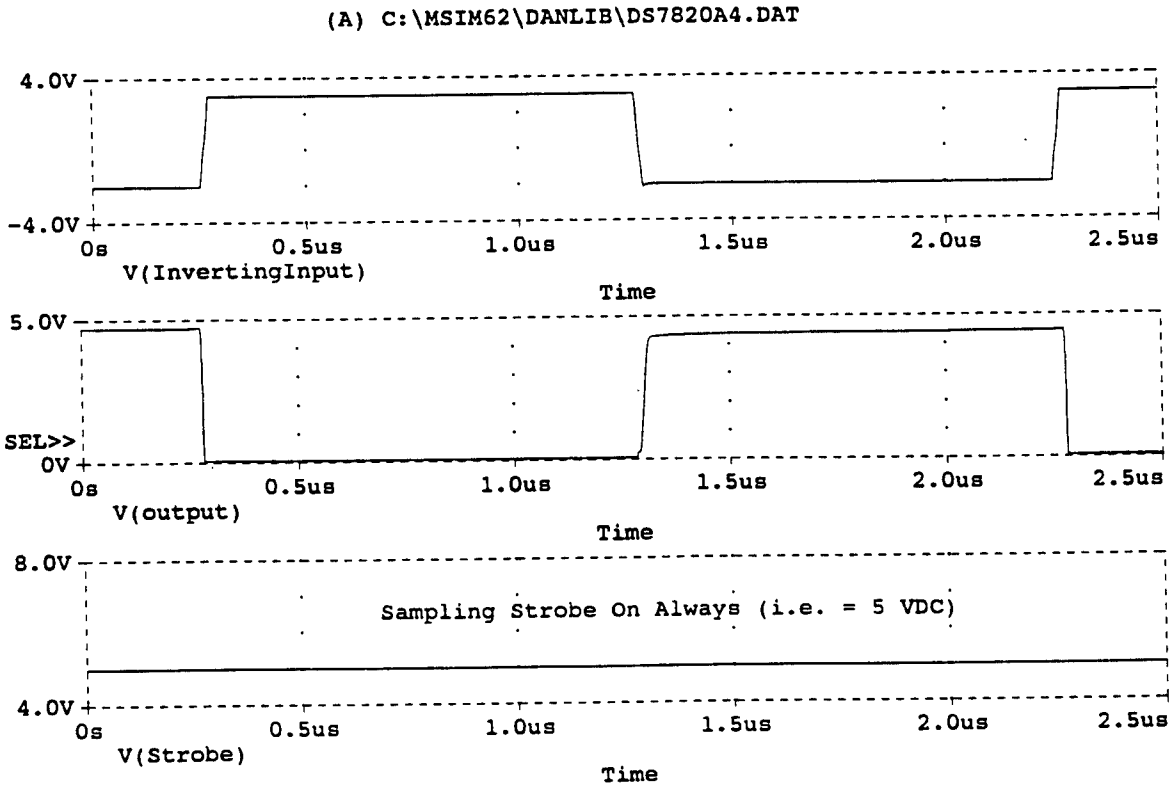
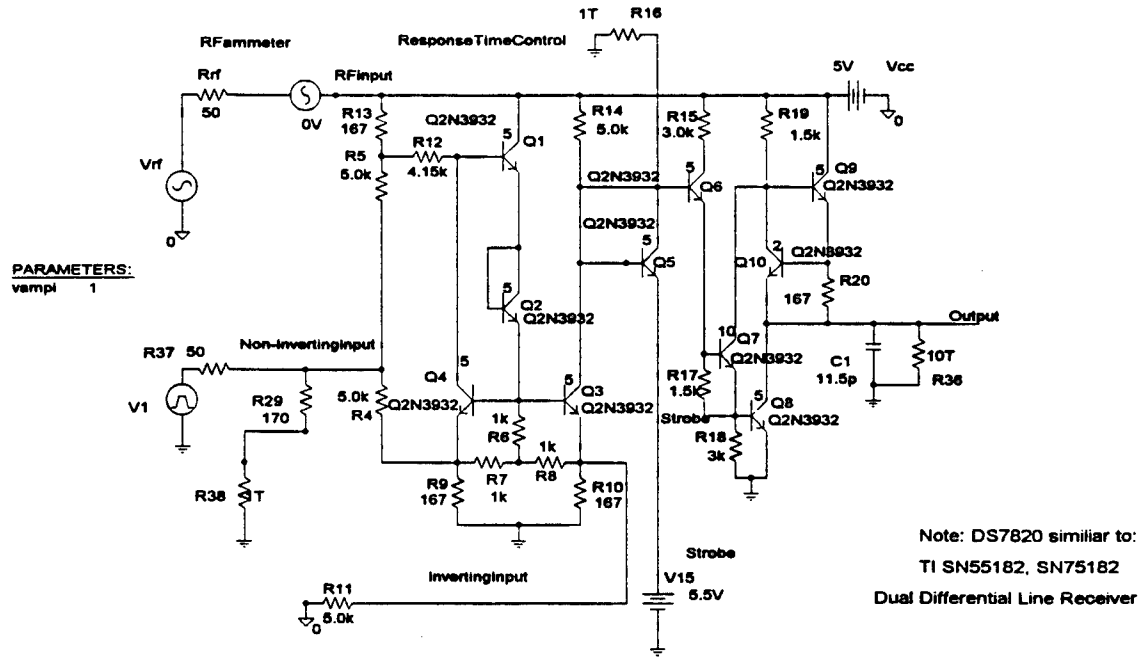


Figure 4-2 DS7820 Differential Line Receiver; Inverting Baseline



DS 7820 DIFFERENTIAL RECEIVER: (10 MHz) EM @ Parallel Driven Vcc Rail

(A) C:\MSIM62\DANLIB\DS7820A3.DAT

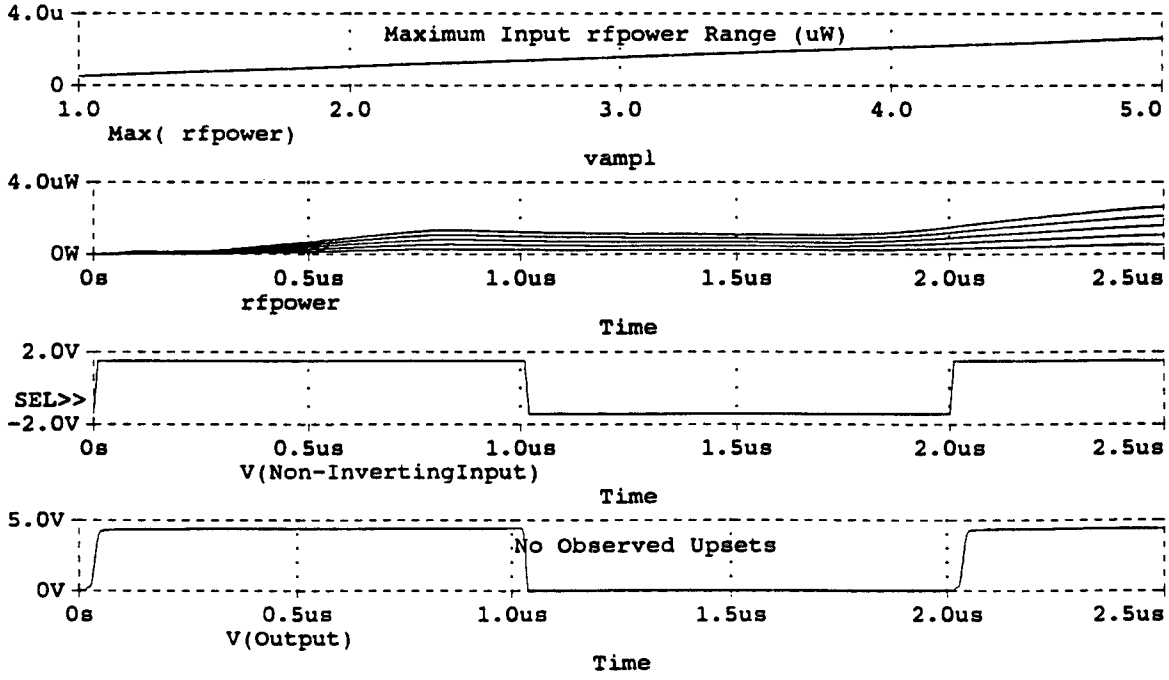
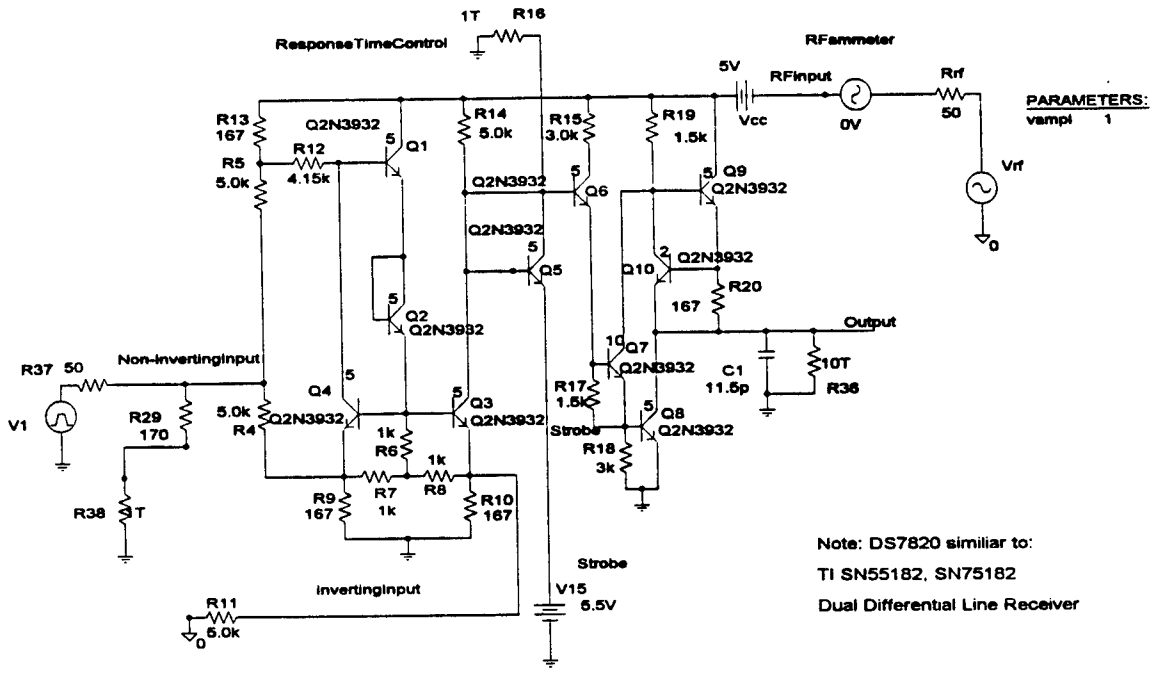


Figure 4-3 10 MHz Voltage Source in Parallel with Vcc Bias Rail



DS 7820 DIFFERENTIAL RECEIVER: (10 MHz) EM @ Series Driven Vcc Rail

(A) C:\MSIM62\DANLIB\DS7820A2.DAT

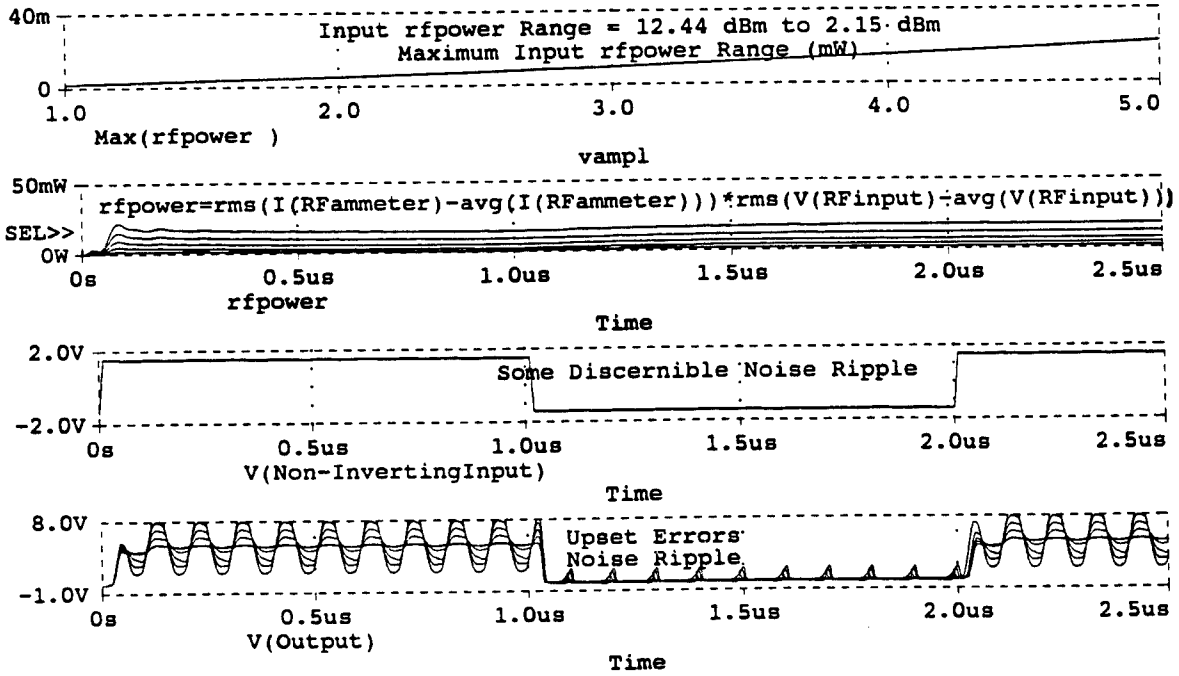


Figure 4-4 10 MHz Voltage Source in Series with Vcc Bias Rail

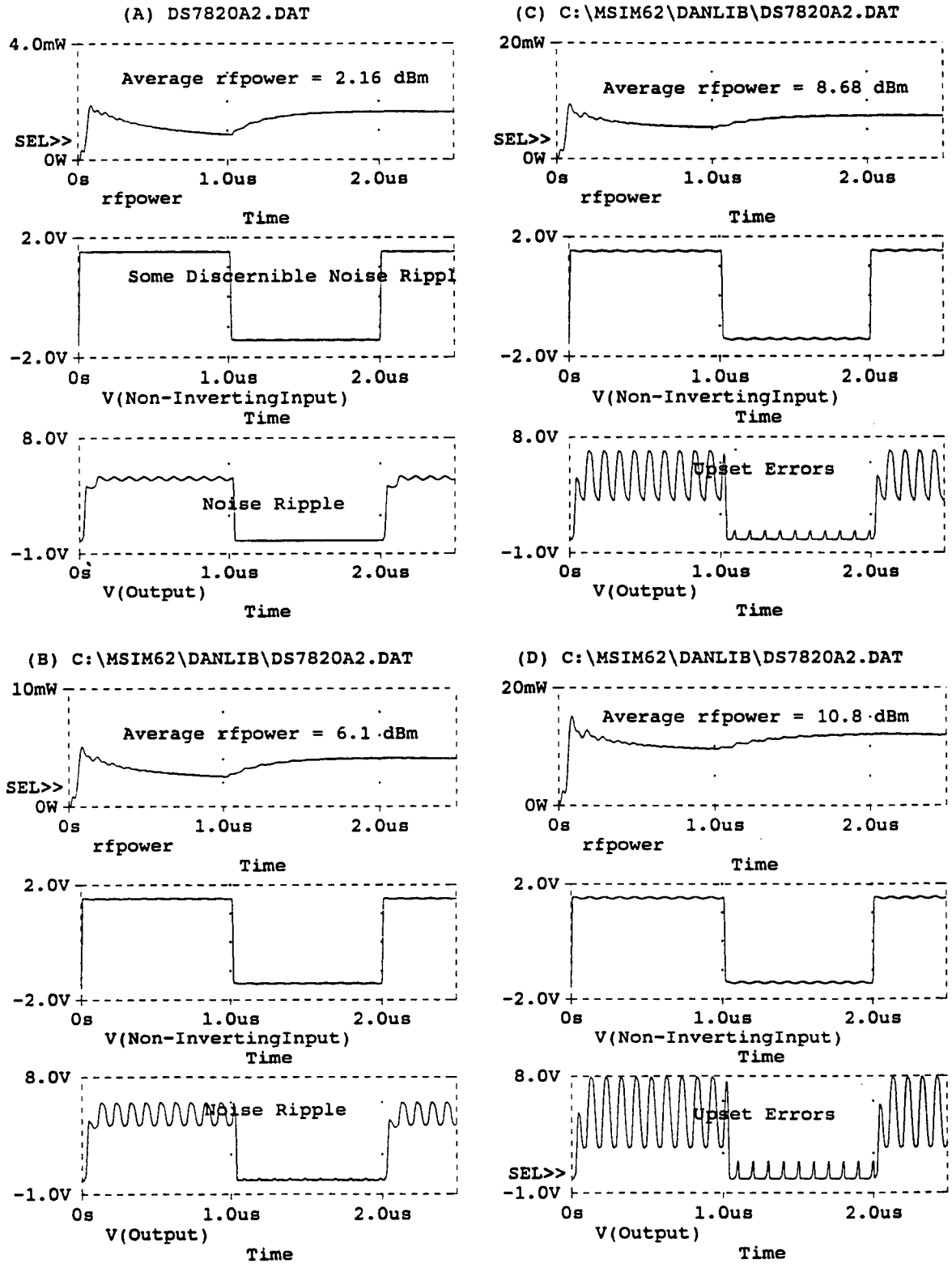
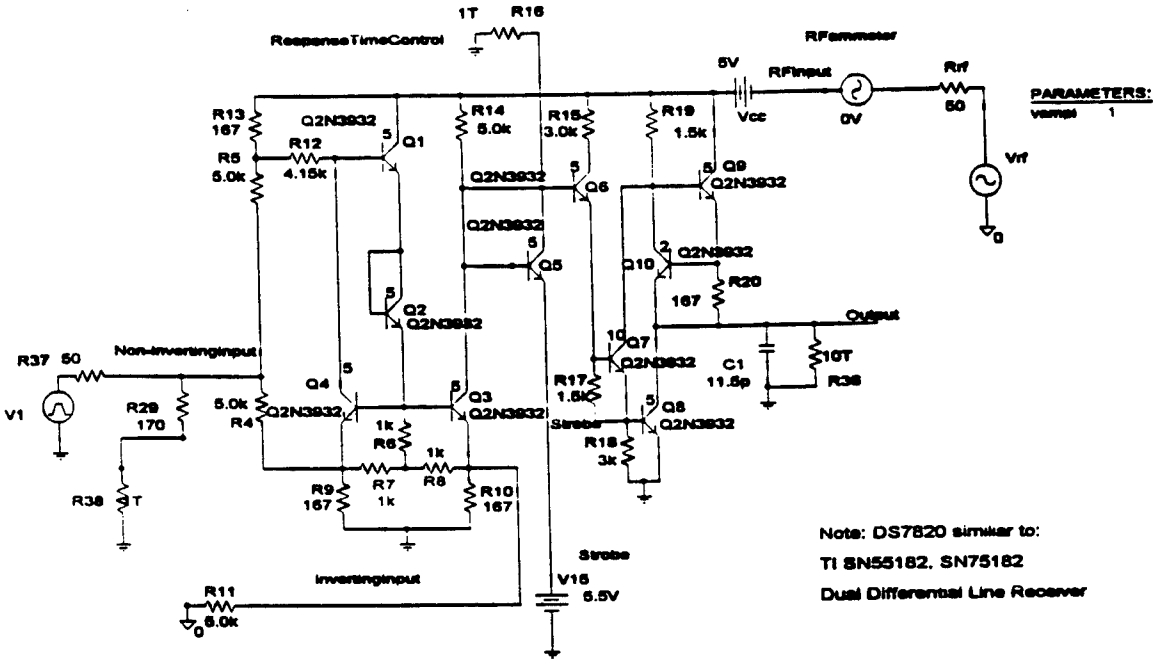


Figure 4-5 Detail Threshold Susceptibility Build-Up



DS 7820 DIFFERENTIAL RECEIVER: (20 MHz) EM @ Series Driven Vcc Rail

(A) C:\MSIM62\DANLIB\DS7820A2.DAT

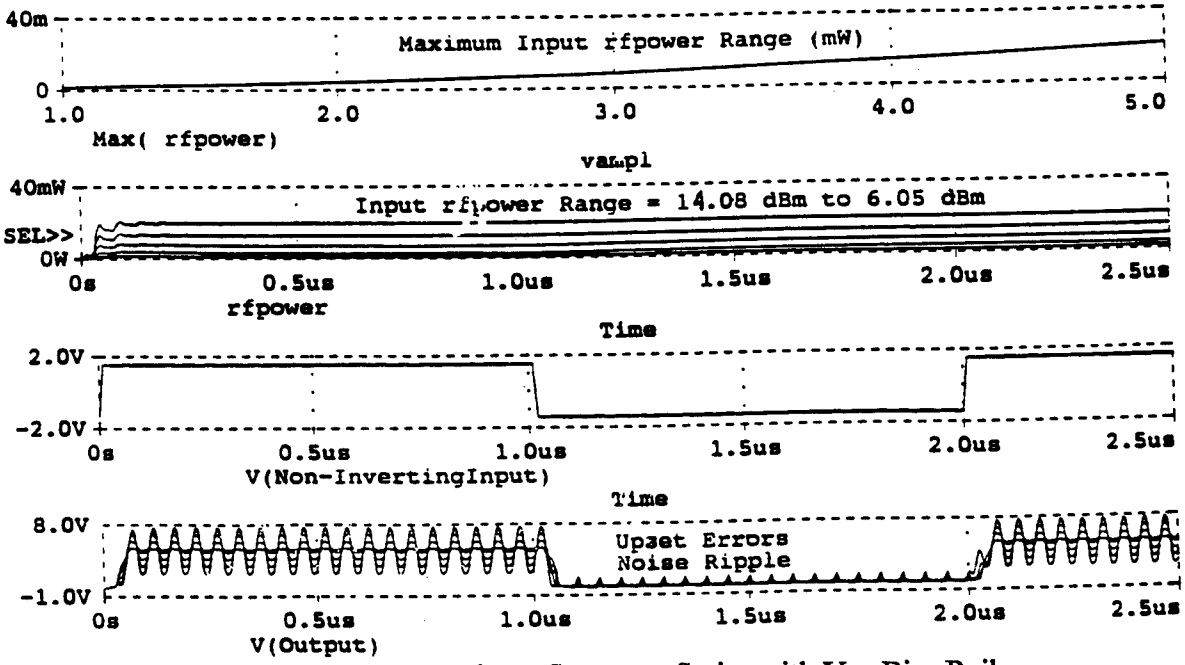


Figure 4-6 20 MHz Voltage Source in Series with Vcc Bias Rail

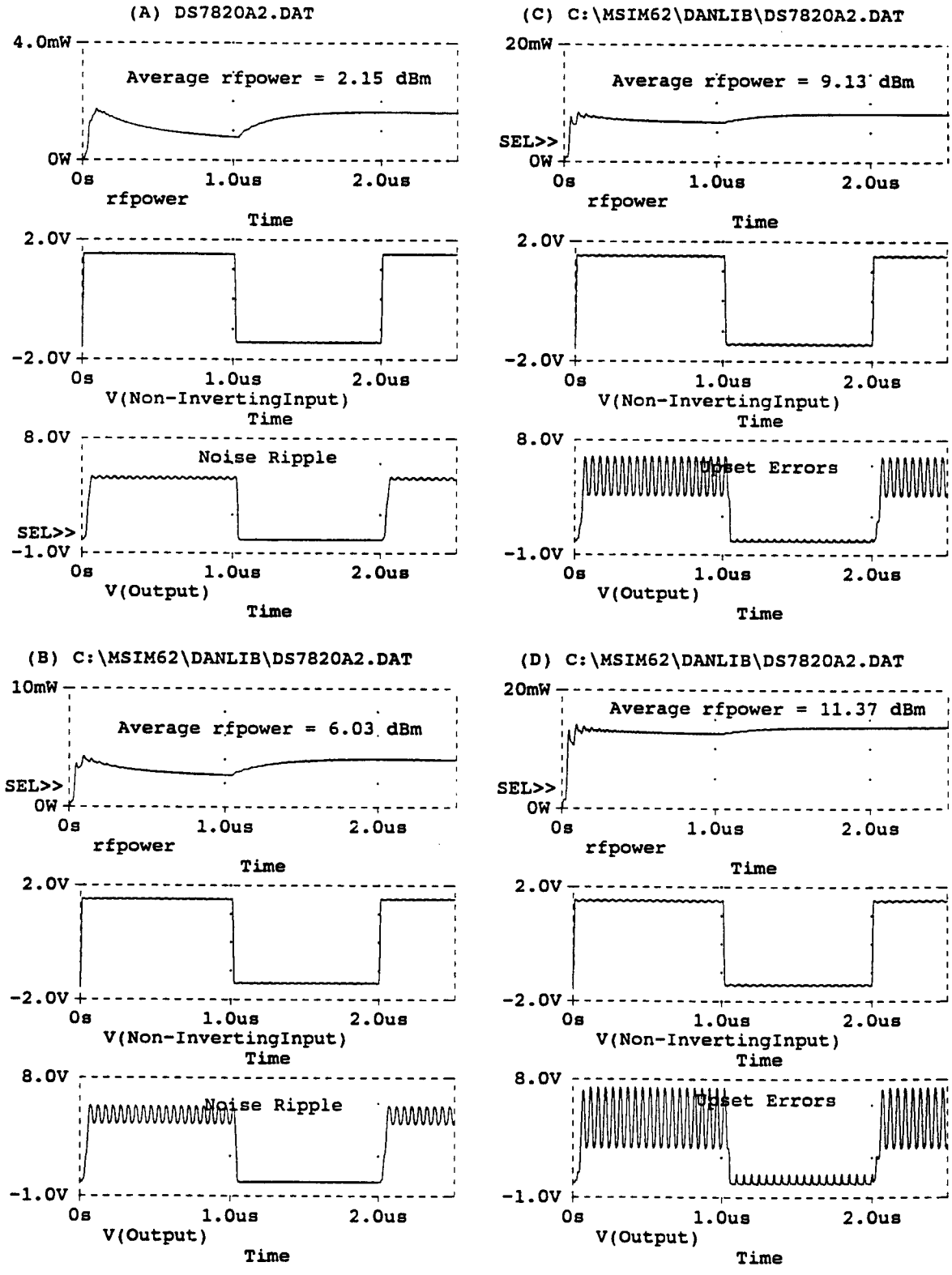
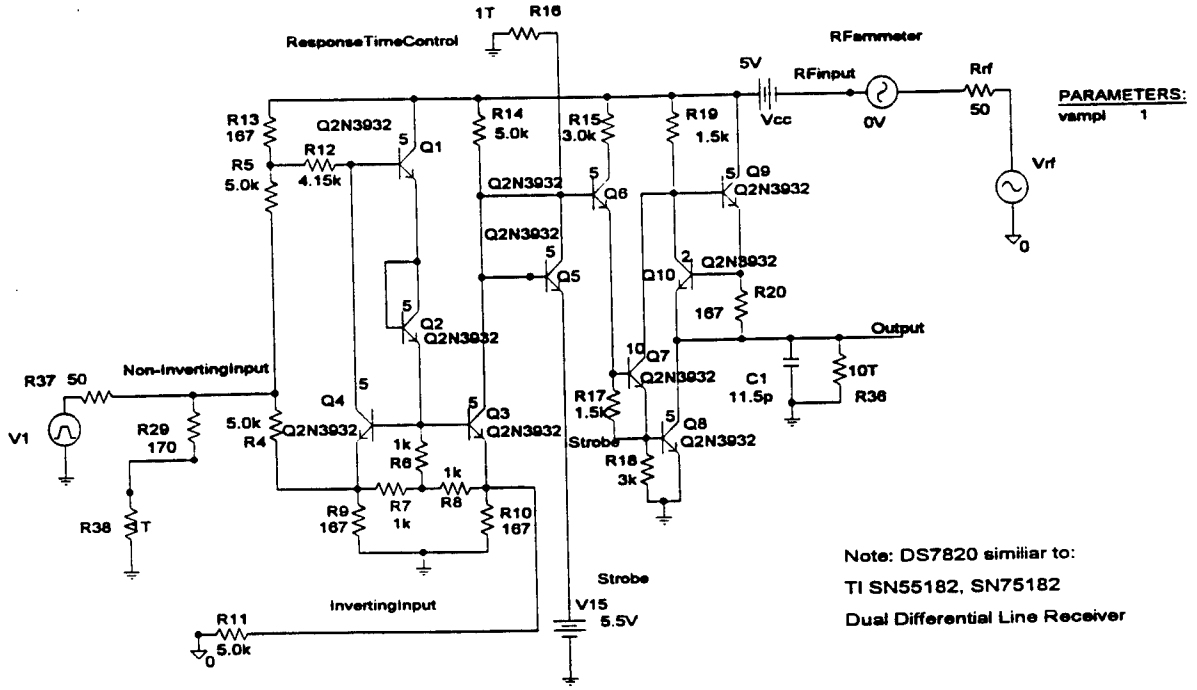


Figure 4-7 Detail Threshold Susceptibility Build-Up



DS 7820 DIFFERENTIAL RECEIVER: (40 MHz) EM @ Series Driven Vcc Rail

(A) C:\MSIM62\DANLIB\DS7820A2.DAT

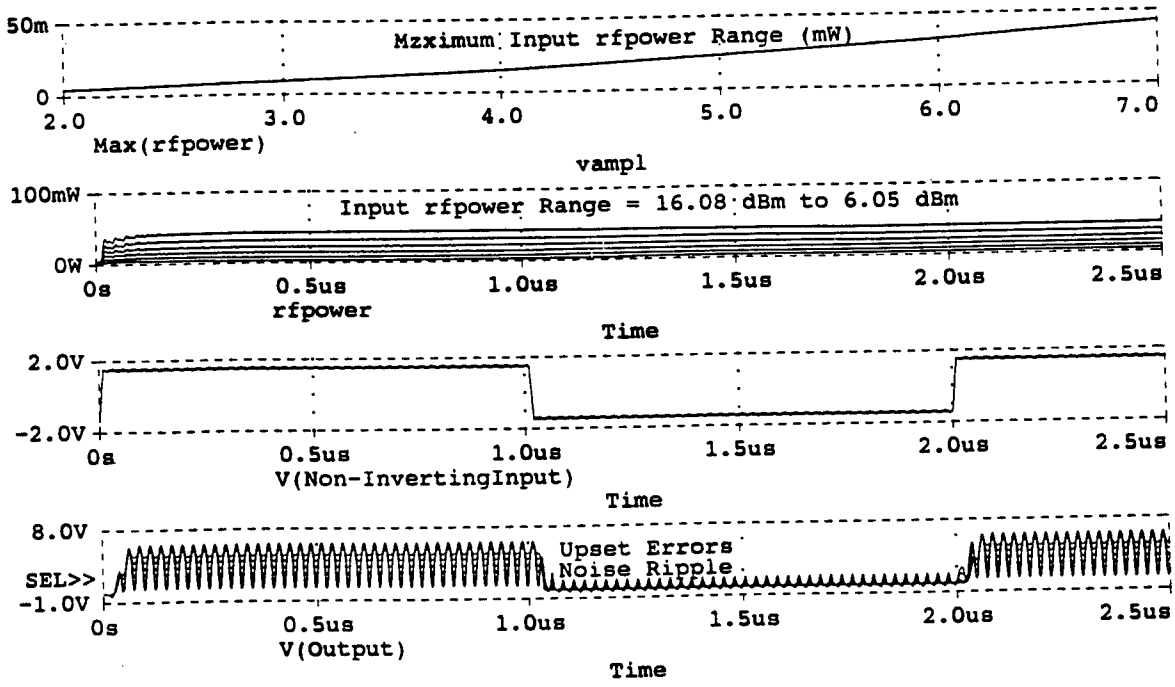


Figure 4-8 40 MHz Voltage Source in Series with Vcc Bias Rail

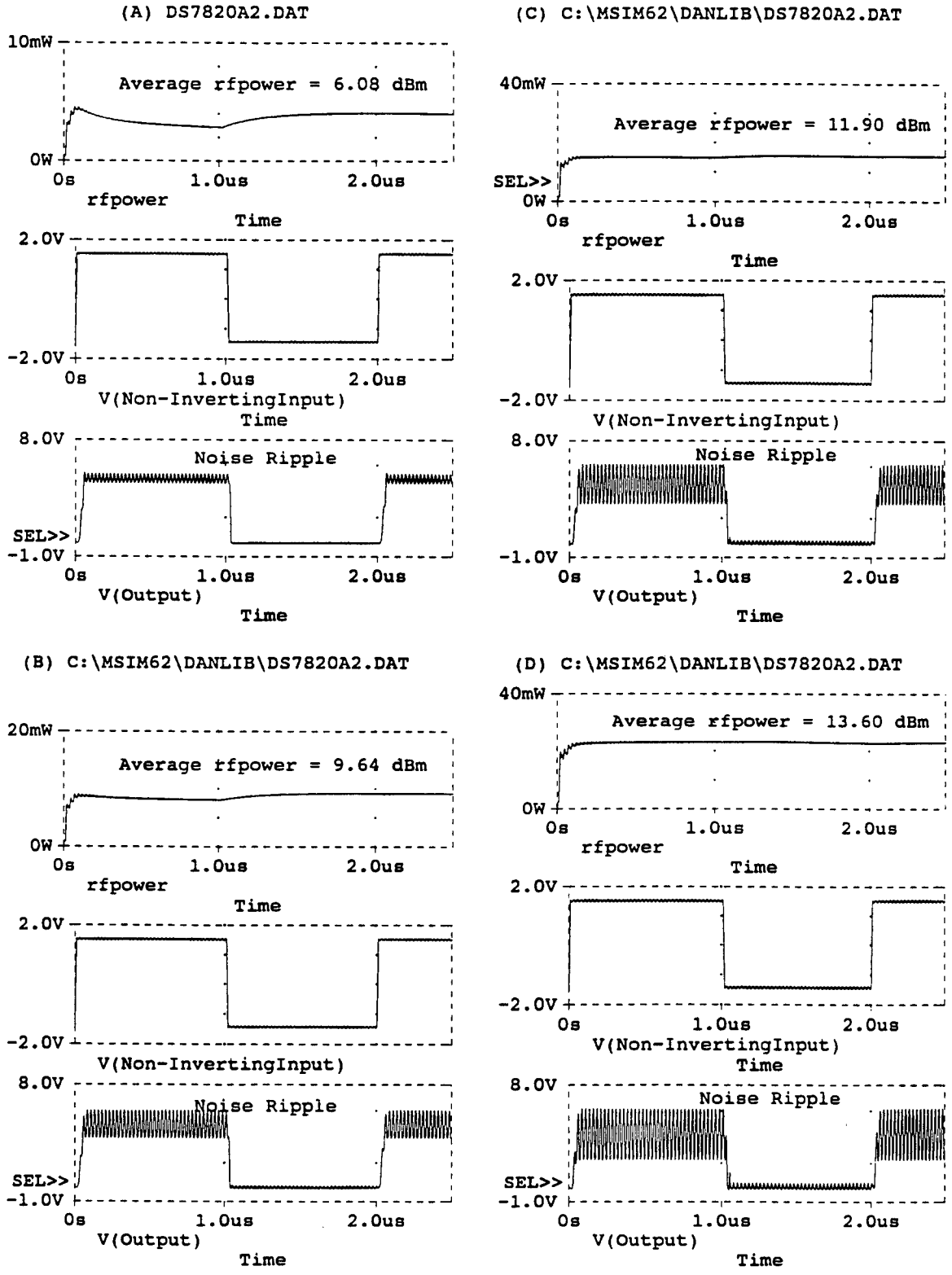
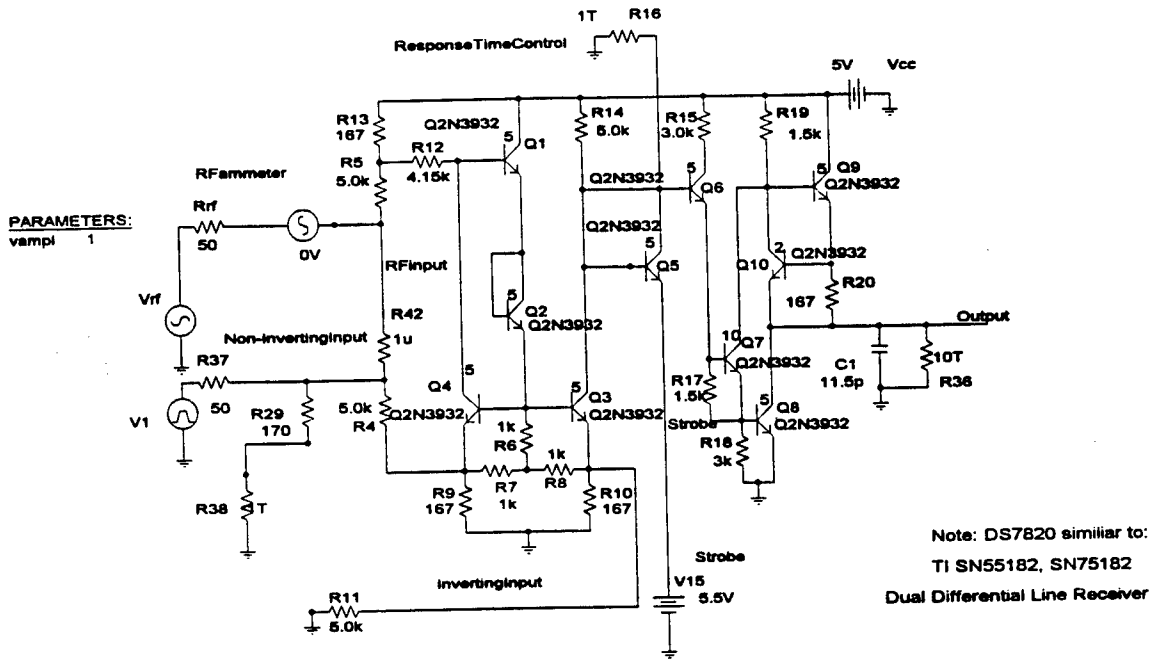


Figure 4-9 Detail Threshold Susceptibility Build-Up



DS 7820 DIFFERENTIAL RECEIVER: (10 MHz) EM @ Parallel Non-Inverting Input

(A) C:\MSIM62\DANLIB\DS7820A3.DAT

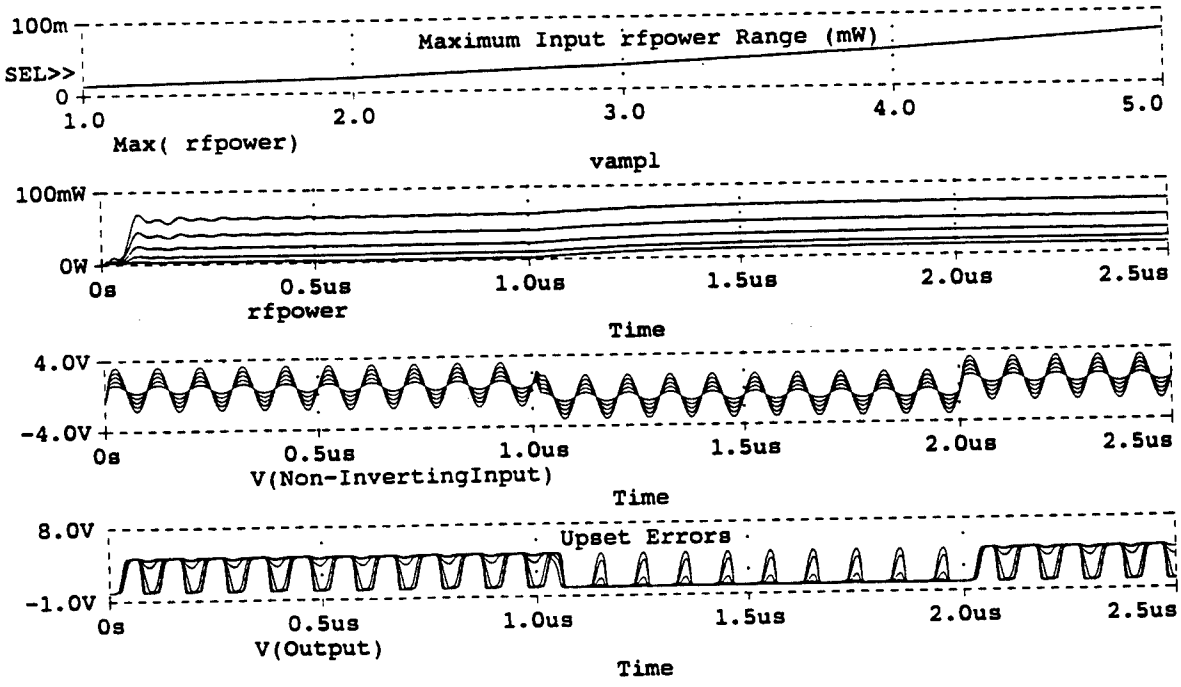


Figure 4-10 10 MHz Voltage Source in Parallel with Noninverting Input

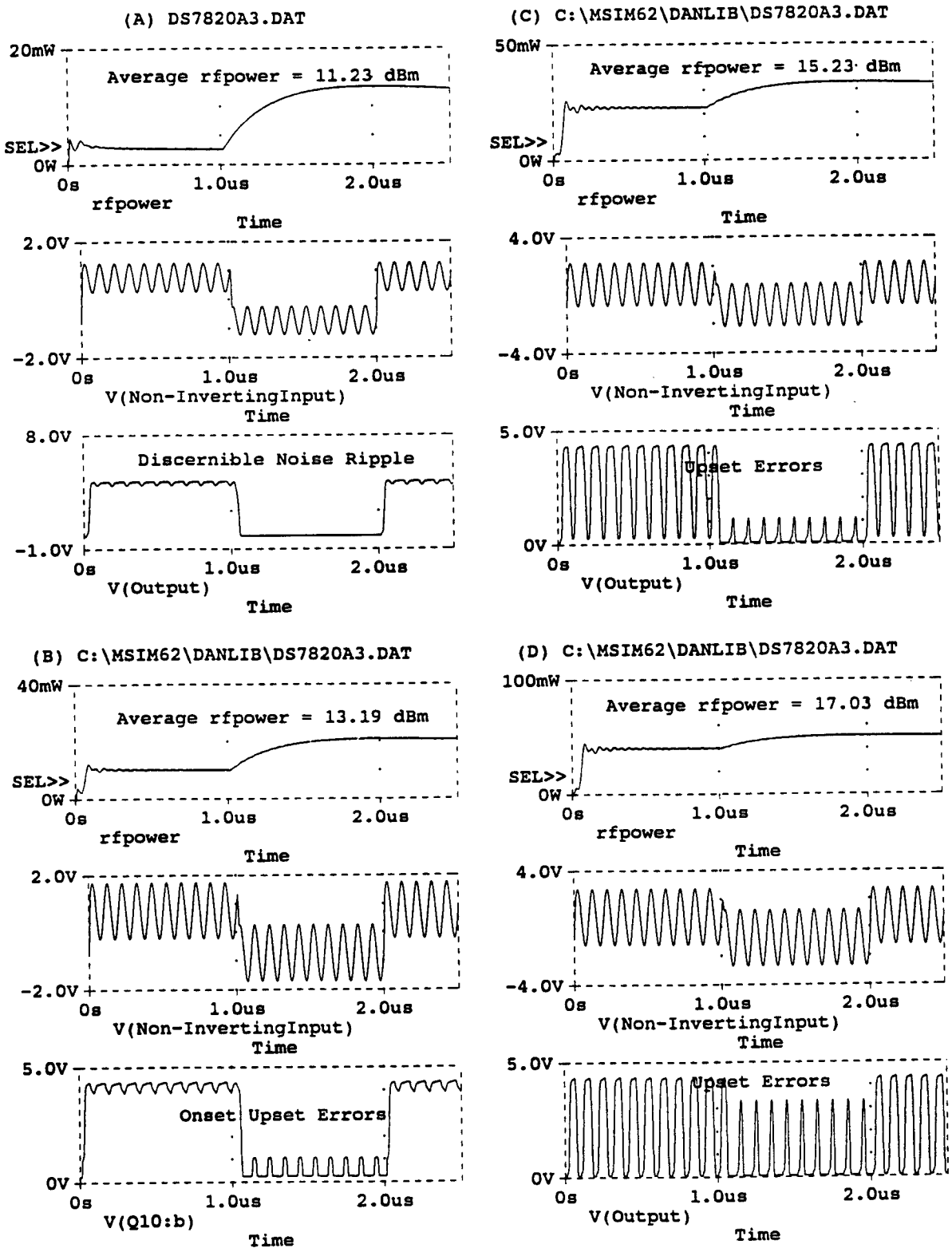
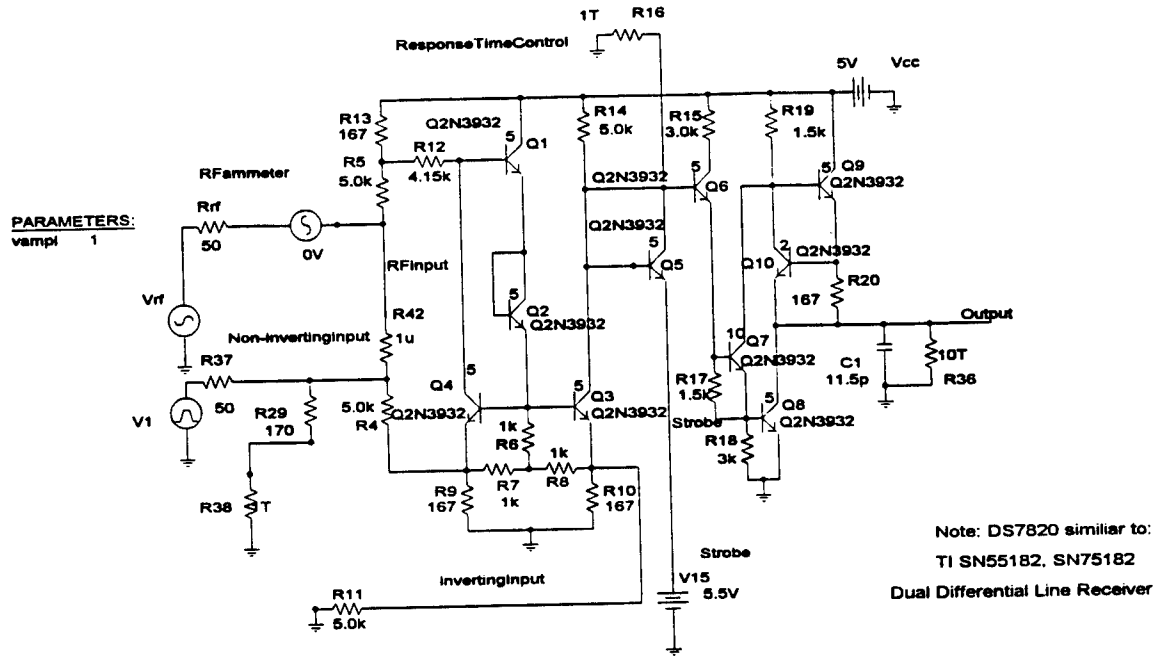


Figure 4-11 Detail Threshold Susceptibility Build-Up



DS 7820 DIFFERENTIAL RECEIVER: (20 MHz) EM @ Parallel Non-Inverting Input

(A) C:\MSIM62\DANLIB\DS7820A3.DAT

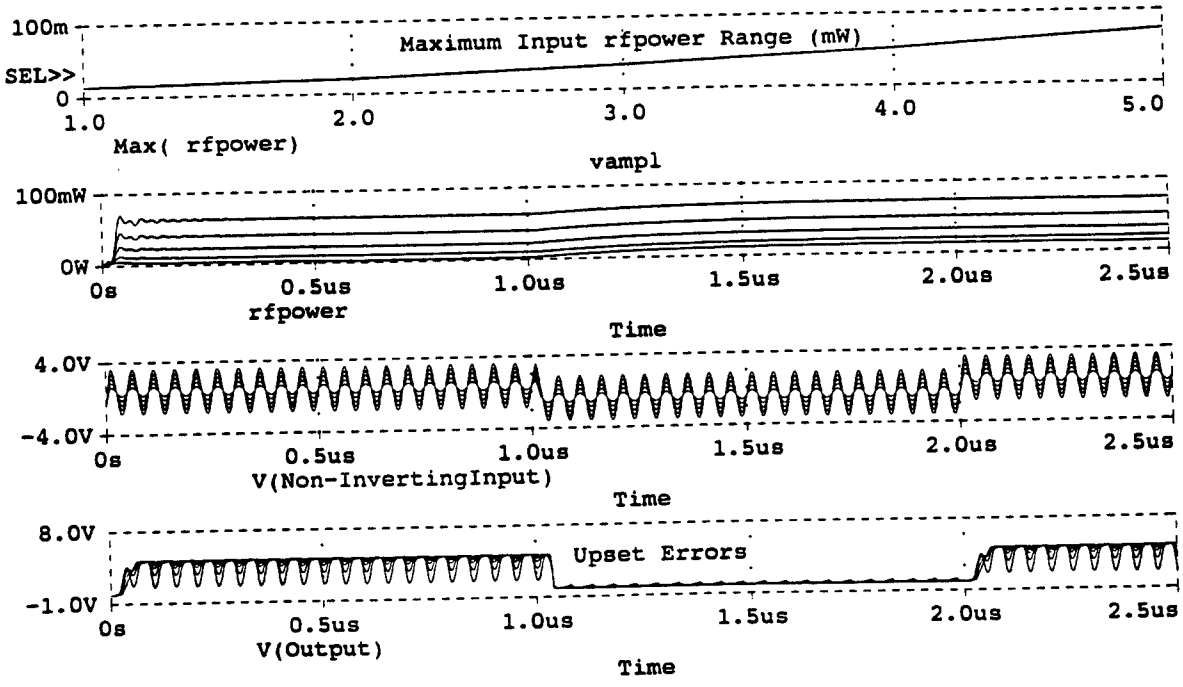


Figure 4-12 20 MHz Voltage Source in Parallel with Noninverting Input

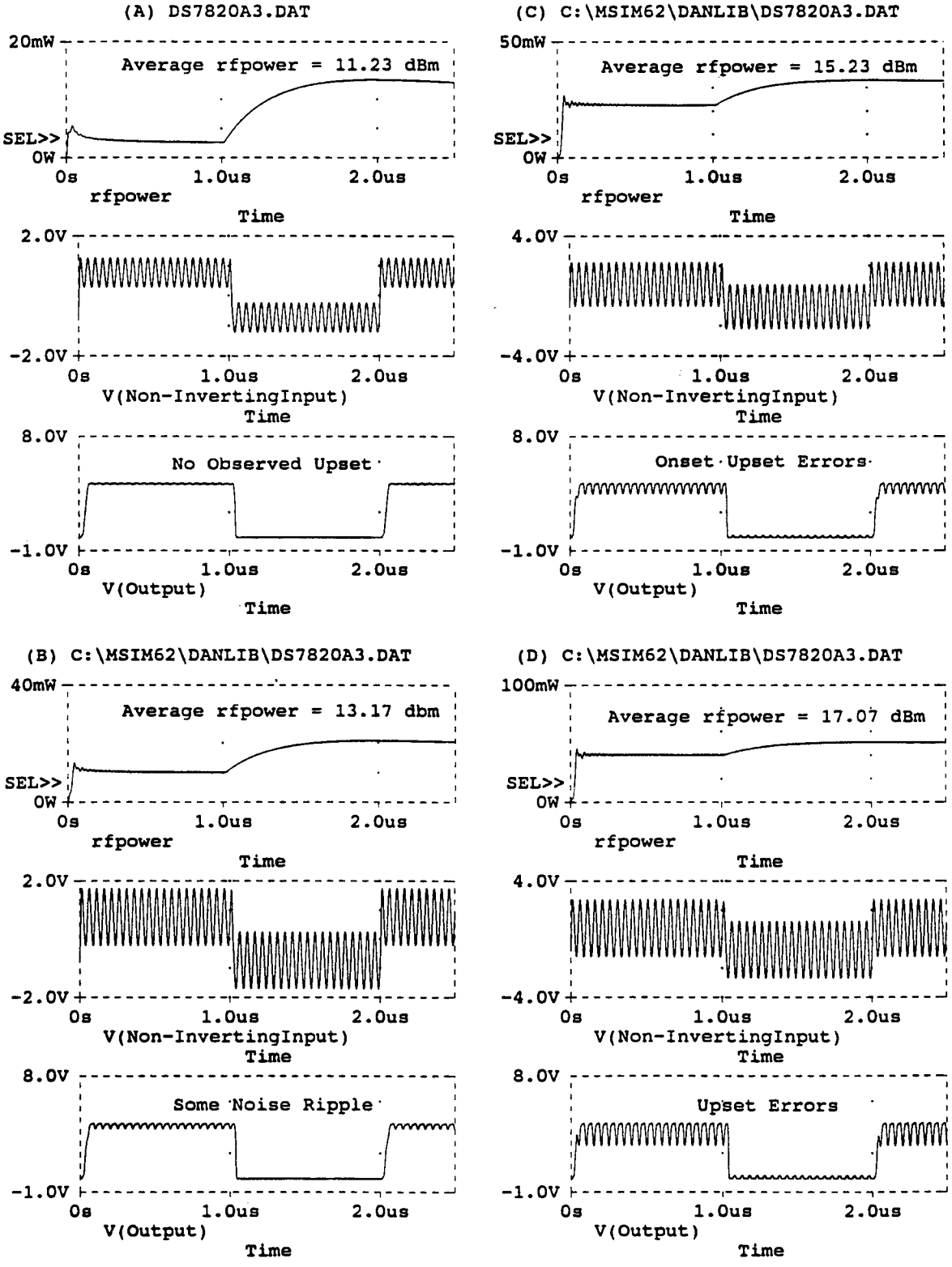
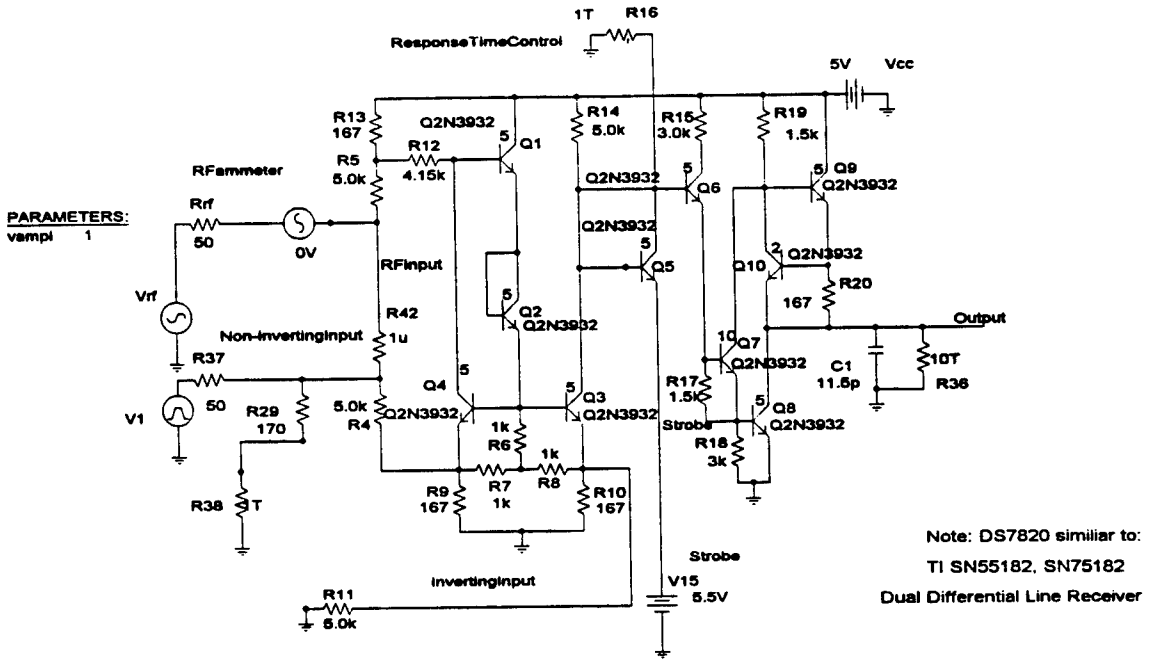


Figure 4-13 Detail Threshold Susceptibility Build-Up



DS 7820 DIFFERENTIAL RECEIVER: (40 MHz) EM @ Parallel Non-Inverting Input

(A) C:\MSIM62\DANLIB\DS7820A3.DAT

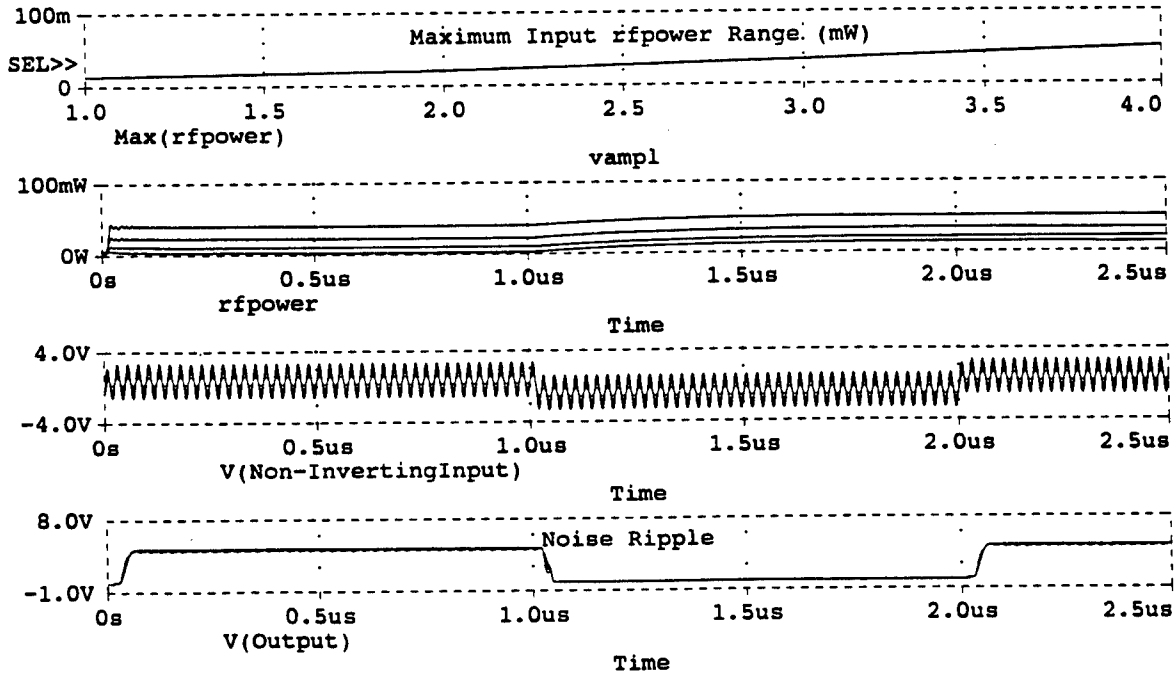


Figure 4-14 40 MHz Voltage Source in Parallel with Noninverting Input

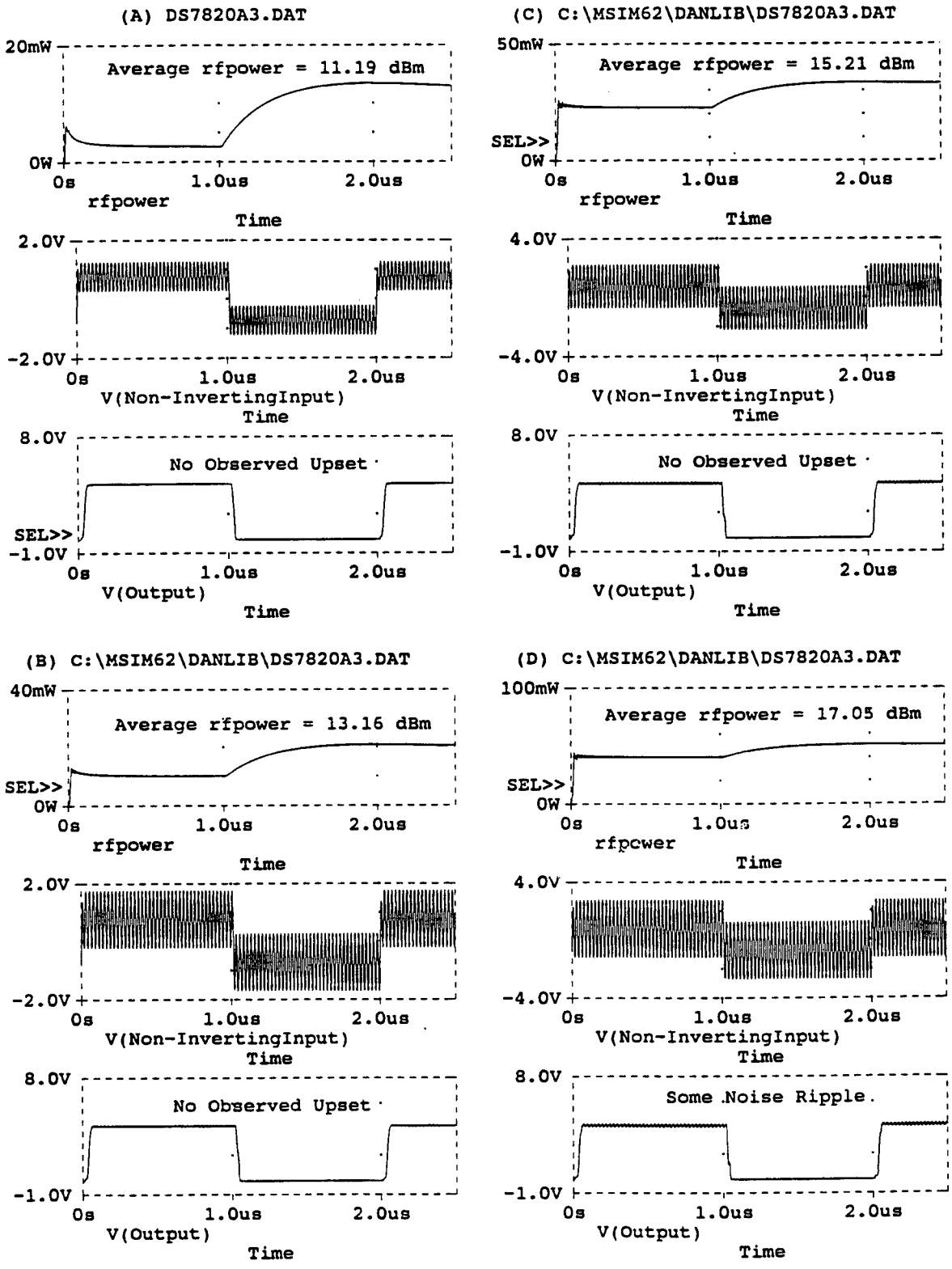


Figure 4-15 Detail Threshold Susceptibility Build-Up

5. 74S00 NAND GATES

Type 74S00 nand gates by Texas Instruments are packaged as four independent 2-input gates designed for the operating temperature range from 0°C to 70°C. Package configurations for these TTL-compatible devices include ceramic chip carriers, plastic DIPs, and ceramic DIPs. In this section, we start to use the peak level of the rf power waveform over the indicated sweeps in the analysis because in most cases the rf power waveform reaches a stable level well before the end of the sweep. Actually, the difference between its peak and steady state level in most sweeps was not significant in the simulation runs to follow.

Recall for most nand gates reported in section 3, the decision by the analyst to "call" an rf driven event (in an output waveform) as upset usually requires comparison with manufacturers' specs and design data on acceptable noise margins. In some cases, this may be tedious, ambiguous, or both. Instead, we decided here to insert an additional nand logic gate on the output of the gate being simulated to detect and track the occurrence of any resulting rf (EM) driven upsets. The reasoning is if the gate being simulated is to drive compatible logic, then it should be (impedance) loaded with the same compatible logic. One result of using this new upset "detection criterion" scheme is to introduce mixed mode signal analyses into the signal mix which PSPICE can easily accommodate.

For example, using compatible ABM logic devices selected from PSPICE model library, the EM analyst simply uses a pristine logic gate connected at the output port of the gate being simulated and allows it to decide that an upset event has occurred during subsequent analyses. This added gate is essentially a digital waveform comparator that provides comparable loading and functions as a bit error rate (BER) detector in PROBE. It is very sensitive to both rf input power levels and timing related thresholds, and computes the precise occurrence of level and timing related upsets in the gate being tested. This BER detector makes the upset decision in a more design realistic way than simply by eye-balling the output logic waveform and comparing it to what is specified.

In the following figures, both analog and digital data are presented on the same plots. Digital plots may contain symbols "R" and "F" that indicate rising and falling transitions, respectively. They are also used to define any ambiguity regions in the output waveform. This happens when the EM driven analysis cannot "decide" on or unambiguously computes a resultant output state. In PROBE, "R" and "F" transitions define an ambiguous region in a waveform as left- and right-handed sides, respectively, of a parallelogram symbol whose time width indicates the persistence of the state uncertainty. Also, a symbol "X" indicates an unknown or indeterminate state which may result from timing hazards or other kinds of upset. Its waveform symbol is a rectangle of some time width. Note that while digital waveforms in PROBE cannot be annotated with text labels, text annotations of analog waveforms are allowed but may cause graphical errors and stack overflows. Increasing the numbers of stacks sometimes helped; the best expedient was simply not annotate.

Figure 5-1 shows the 74S00 baseline gate with a BER detector gate connected to its digital output port. The waveforms shown are mixed mode - input A, input B, and "digout" waveforms are analog; BER waveform is digital. Figure 5-2 shows the test gate driven by a 10 MHz voltage source in series with its Vcc bias rail. BER output data for input rf power levels from 5 mW to 12 mW show timing and level ambiguities, and advent of upset errors. Figures 5-3 and 5-4 show more detailed data. At low rf power of - 0.21 dBm, there was no observed upset in the low state of the desired pulse but distinct ripple modulation of the high state. Upset errors in the pulse were observed at 2.81 dBm. At 5.13 dBm, there were state ambiguities in the pulse. At 8.51 dBm, there seems to be some clipping in the digout waveform. At 9.62 dBm, there were added upset transitions outside the desired pulse. At 10.65 dBm, there is considerable ripple in the high state, unknown states, and ambiguous states in the BER output. Figures 5-5 show the test gate driven by a 20 MHz voltage source in series with its Vcc bias rail. BER output data for input rf power levels from 1.4 mW to 2.9 mW timing and level ambiguities, and advent of upset errors. Figure 5-6 shows the detail of the

build-up of the ripple modulation outside the desired pulse width. Upset errors in BER output seem to commence around 2.55 dBm. Figure 5-7 shows the test gate driven by a 30 MHz voltage source in series with its Vcc bias rail. BER data for input rf power levels from 1 mW to 14 mW indicate considerable ripple modulation outside the pulse width. Figure 5-8 shows the detail; BER upsets occur at 5.7 dBm and ambiguities are evident at 11.66 dBm.

Figure 5-9 shows the test gate driven by a 10 MHz voltage source in series with its logic inputA. For rf input power levels around 1.26 dBm, upset errors are apparent. Figure 5-10 shows the build-up to the upset states. At 1.11 dBm, there is discernible noise ripple; at 1.24 dBm, the ripple is distinct; at 1.42 dBm, the BER detector announces upset in the waveform; at 1.64 dBm, the upset is sustained. Figure 5-11 the test gate driven by a 20 MHz voltage source in series with its logic inputA. Again, For rf input power levels around 2.11 dBm, upset errors are apparent. Figure 5-12 shows the detail of the build-up. The BER detector announces upset at about 2 dBm. Figure 5-13 shows the test gate driven by a 30 MHz voltage source in series with its logic inputA. For rf input power levels around 2.73 dBm, upset errors are apparent. Figure 5-14 shows the detail of the build-up. Upset threshold by the BER detector is now about 2.91 dBm.

Figure 5-15 shows the test gate driven by a 10 MHz voltage source in parallel with its logic inputA. In these and all other parallel runs, the EM source and logic input A source were both doubled to offset the voltage divider formed by internal source resistances. In rf power ranges of 18 dBm, upsets are evident. Figure 5-16 shows the detail of the build-up. Upset thresholds from the BER are at about 18.0 dBm which suggest victim is relatively EM hard. Figure 5-17 shows the test gate driven by a 20 MHz voltage source in parallel with its logic inputA. Figure 5-18 shows the BER detected thresholds to be around 18.16 dBm. Again, this device port is hard for the EM coupling indicated. Figure 5-19 shows the test gate driven by a 30 MHz voltage source in parallel with its logic inputA. Figure 5-20 shows the detail performance and that the BER detector again thresholds

at around 18 dBm, still indicating a hard device at this frequency. Figure 5-21 again shows the baseline gate. Figure 5-22 show the gate being driven by 30 MHz current source in series with its logic inputA. Because current sources and voltage sources in series are duals, these data are comparable to figures 5-13 and 5-14 where the upset susceptibility seems higher than in present cases of current driven sources. Figure 5-23 indicates the attendant build-up of ripple noise and upset errors which threshold at about 5 dBm (compare to 3 dBm for comparable voltage sources).

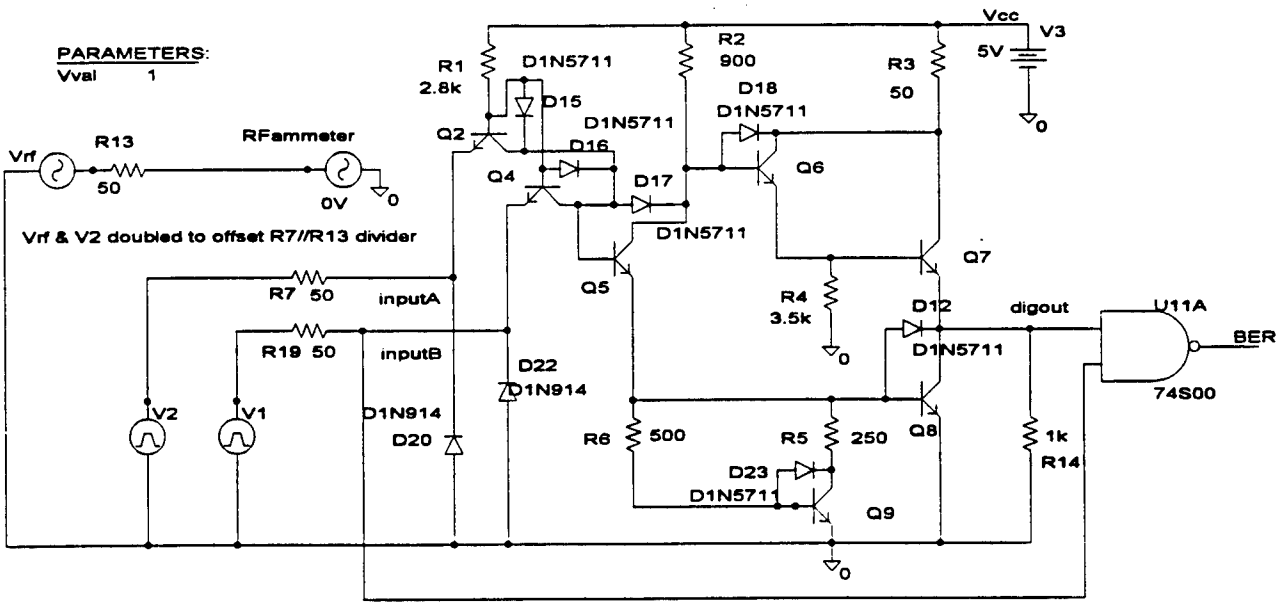
Figure 5-24 shows the gate being driven by 30 MHz current source in series with its intended ground. Error upsets are evident. Figure 5-25 shows the detailed onset of these errors at which BER2 corresponds to an rf input peak power at the ground port of - 2.0 dBm. For the BER response waveforms shown, BER1,2,3...7 waveforms correspond to rf input peak powers equal to - 10 dBm, - 2.0 dBm, 1.86 dBm, 4.7 dBm, 8.24 dBm, 10.8 dBm, and 12.7 dBm, respectively. It is of interest to note that simply setting a source amplitude to zero may not be a realistic simulation of "no" source. The source resistance that remains in the schematic may cause erroneous results. For example, in figure 5-25 BER1 is the logic response for Irfampl set to zero and no upset is indicated. However, some dc power is measured by the power meter at the intended ground node which is no longer at zero voltage due to the source resistance. With the current source amplitude Irfampl set to zero (during the parametric sweep), desired sources V1 and V2 have become dc biased and violate the baseline integrity. To avoid this problem and simulate a (current or voltage) source with zero amplitude, it's best to physically remove it and its resistance from the schematic.

Figure 5-26 shows the gate being driven by 10 MHz current source in parallel with its logic inputA. For input power levels between 18 and 19 dBm, the device exhibits a relatively hard susceptibility. Figure 5-27 shows the detail and indicates a threshold of 18.6 dBm. Next, figure 5-28 shows the gate being driven by 20 MHz current source in parallel with its logic inputA. The device still exhibits the same hard susceptibility. Figure 5-29 shows an upset threshold of 18.6 dBm, again.

Figure 5-30 shows the gate being driven by 30 MHz current source in parallel with its logic inputA. The device still exhibits the same hard susceptibility. Figure 5-31 shows the detail and indicates an upset threshold of 18.5 dBm. These last three runs suggest that device susceptibility is "hard" and constant over this frequency range.

Figure 5-32 shows the gate being driven by 10 MHz current source at the inverter input stage. For a peak level of rf input power equal to 12.24 dBm, there is no apparent upset in the BER waveforms. However, there are sustained ambiguous and unknown states evidenced in the duration of the desired pulse. Closer inspection of the test circuit reveals that connecting a current source RFI1 puts its source resistance Rrf in parallel with the bias resistance R4 of output inverter Q7. This effectively pulls the bias node to ground during the logic pulse and causes the BER output waveforms to be contaminated with X's and F's each bit cycle. Since this situation seemed to be independent of rf amplitude, two other frequency cuts were taken at 20 MHz and 30 MHz. Figures 5-33 and 5-34 at the same input rf power levels confirm this kind of latch-up in the BER responses. Note that figures 3-17 to 3-25 also show comparable responses for voltage sources at an inverter input.

Finally, for purposes of comparison to data elsewhere in this report, we present figures 5-35 and 5-36 which show the test gate driven by a 10 MHz voltage source and a 10 MHz current source each in parallel with its Vcc bias port, respectively. While available rf powers range from 4-12 dBm in figure 5-35 and 10-16 dBm in figure 5-36, there were no upsets observed. In these runs, very little rf power was absorbed by the bias ports. As in figures 3-2 to figures 3-5, Vcc ports seem to exhibit relatively low susceptibility levels (greater than 12 dBm) to parallel coupled, cw rf sources in these frequency ranges. In contrast, figures 5-2 through 5-8 for series coupled, cw rf sources exhibited relatively high susceptibility levels (around 2.5 dBm).



74S00 NAND GATE: BASELINE

(A) C:\MSIM62\DANLIB\74S00-3B.DAT

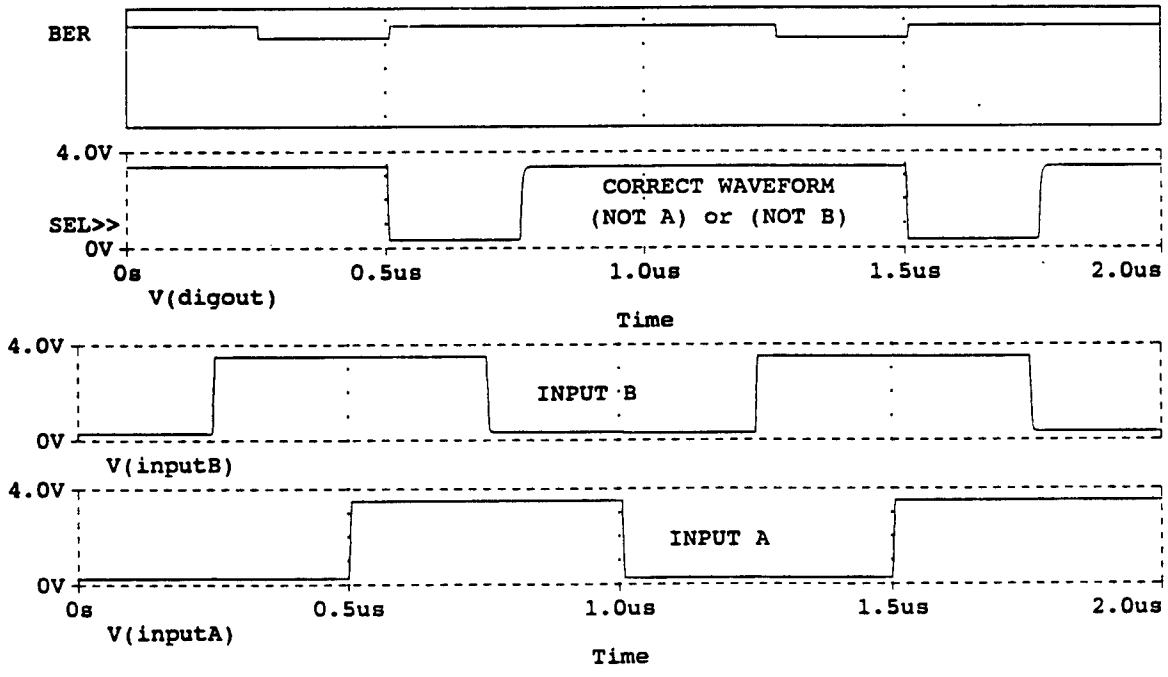
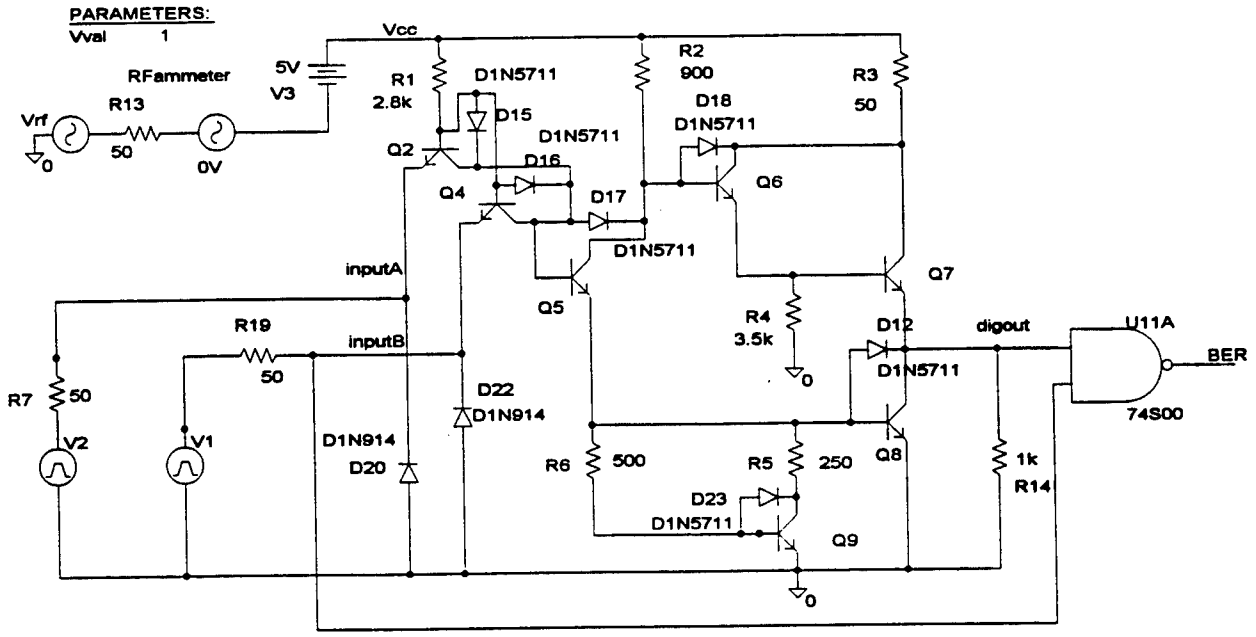


Figure 5-1 Baseline 74S00 Gate and Logic Responses



74S00 NAND GATE: (10MHz) EM @ Series Driven Vcc Rail

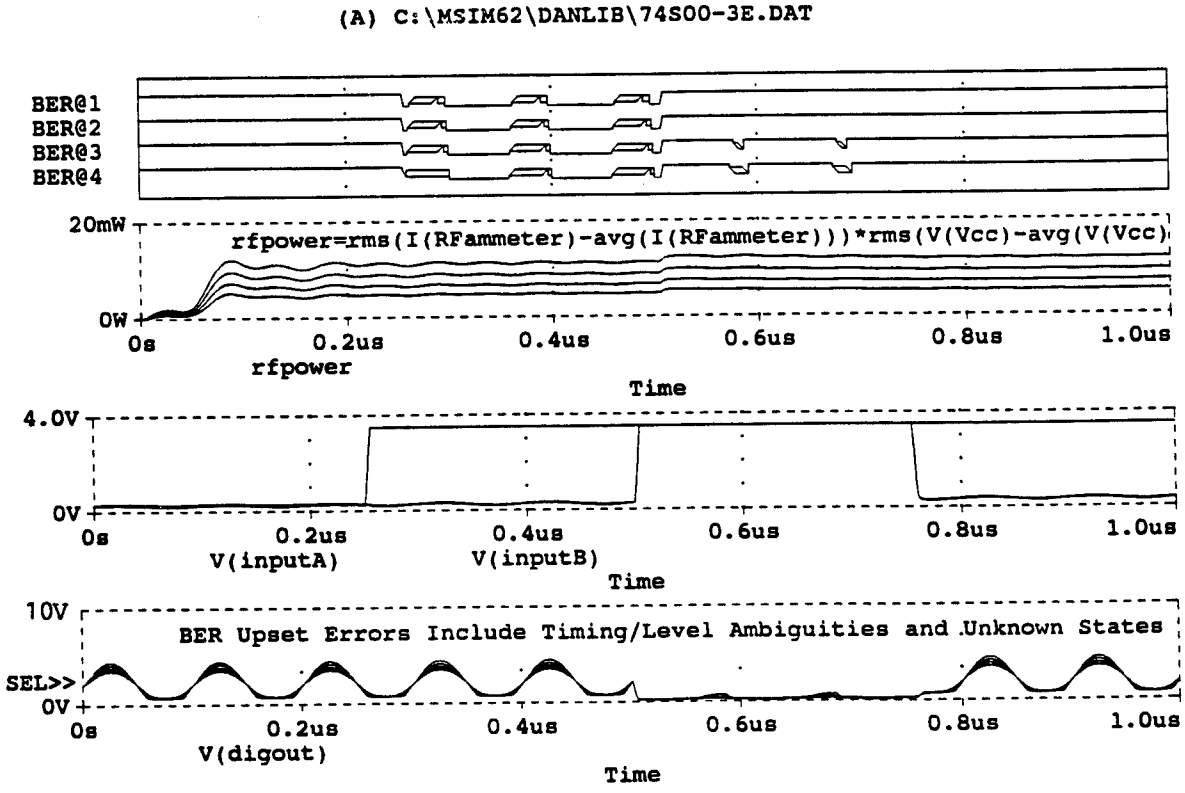


Figure 5-2 Test Gate with 10 MHz Voltage Source in Series with Vcc Bias Rail

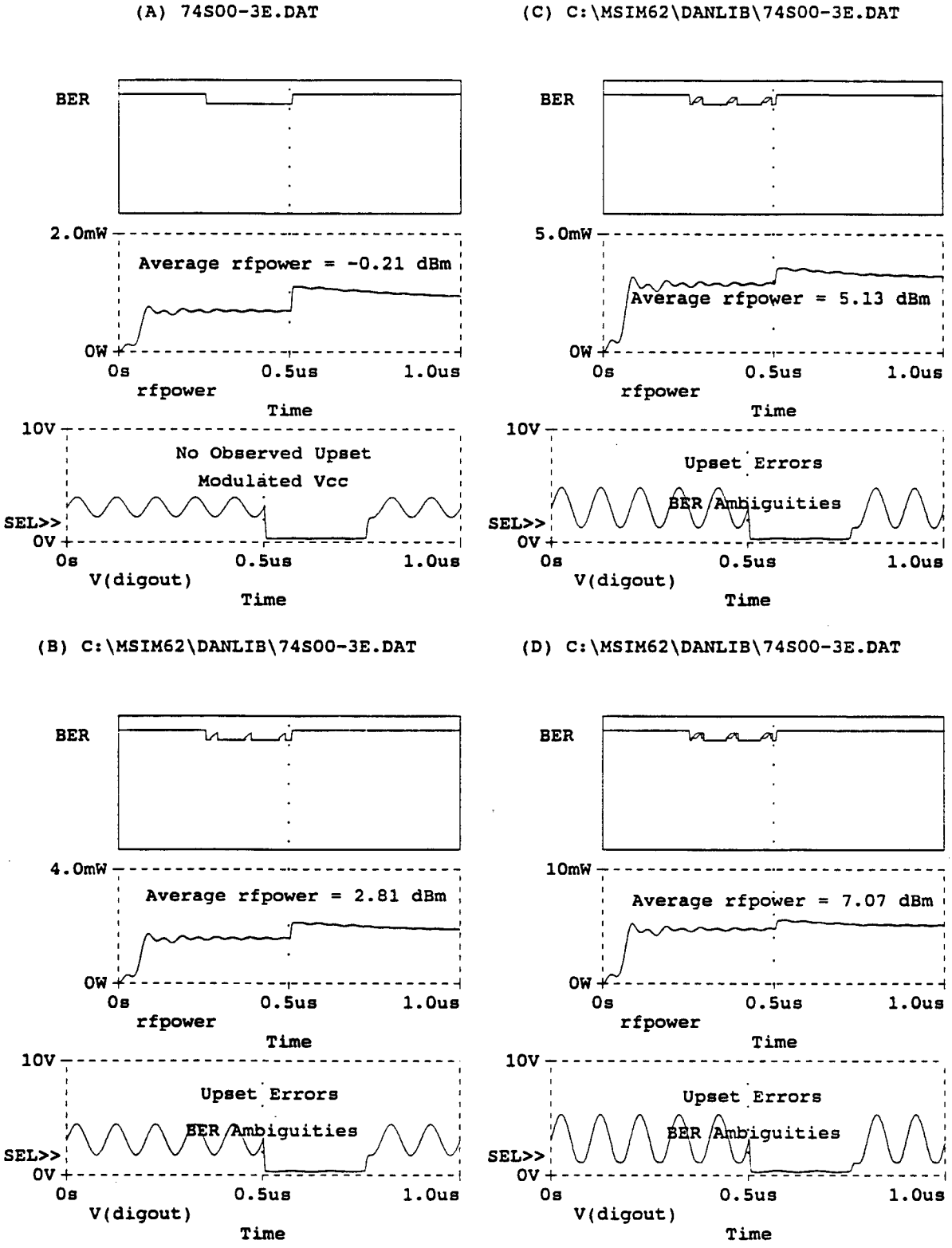


Figure 5-3 Detail Data susceptibility Build-Up

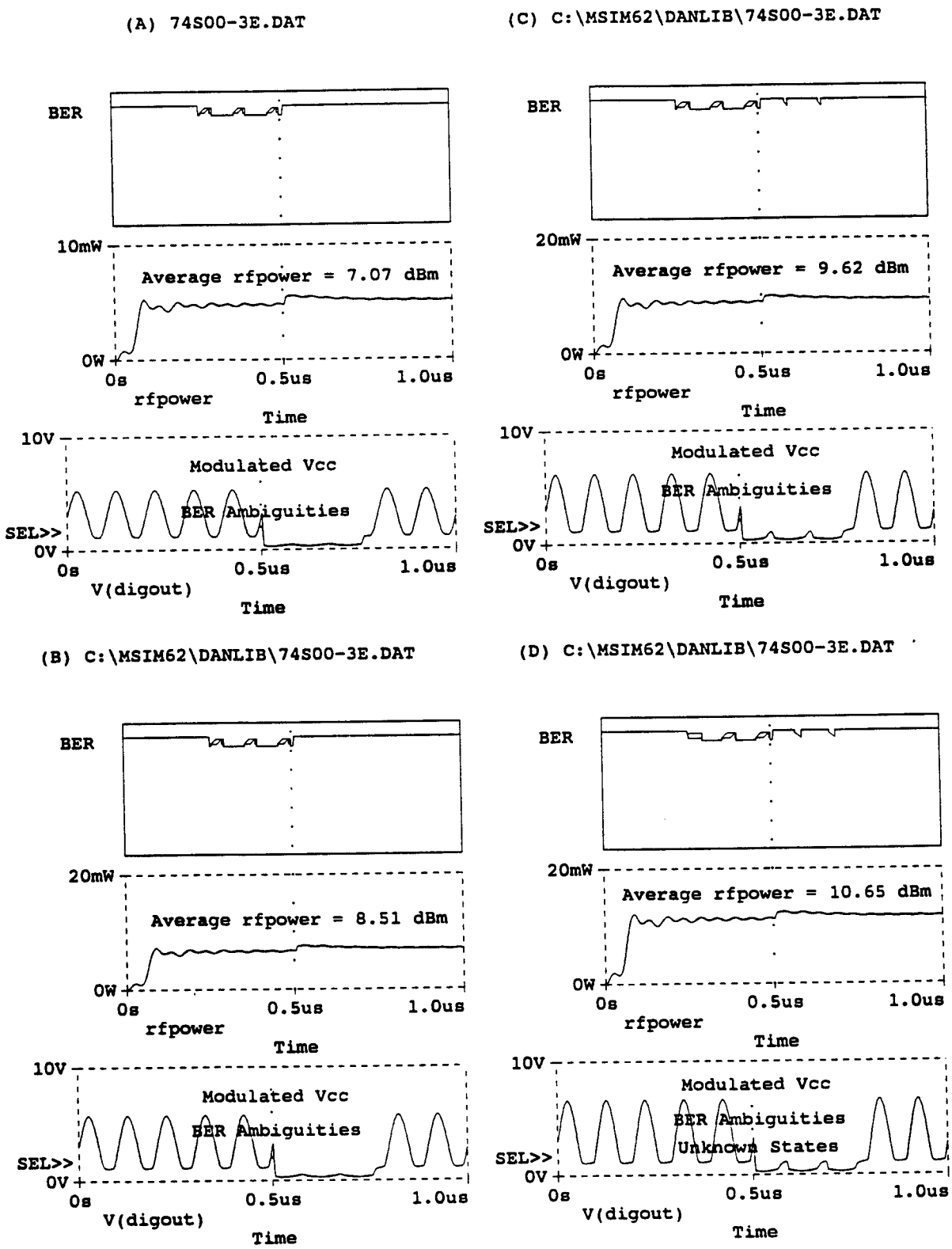
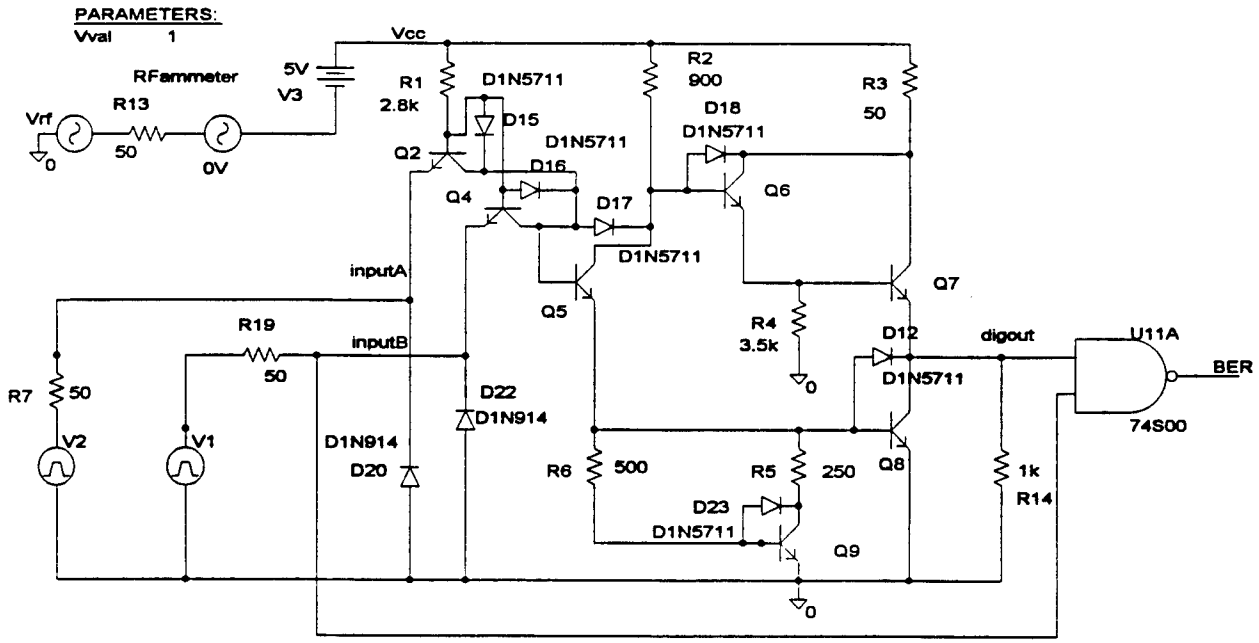


Figure 5-4 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (20MHz) EM @ Series Driven Vcc Rail

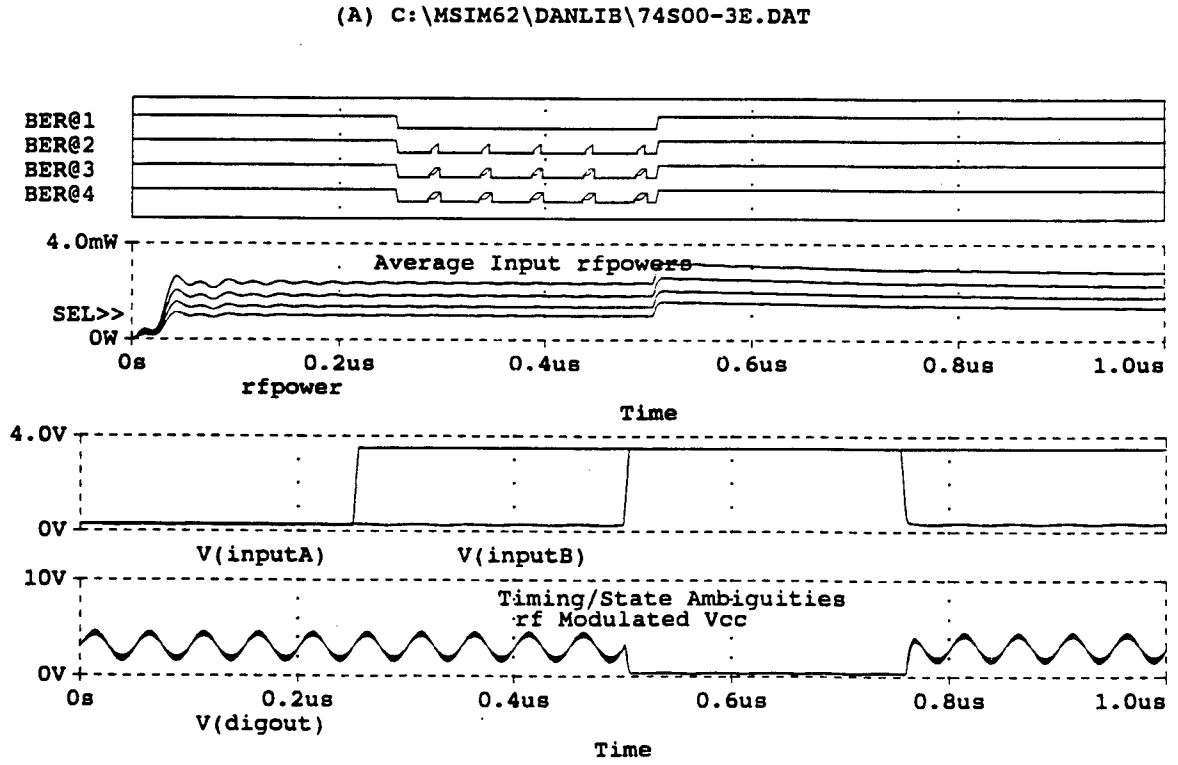


Figure 5-5 Test Gate with 20 MHz Voltage Source in Series with Vcc Bias Rail

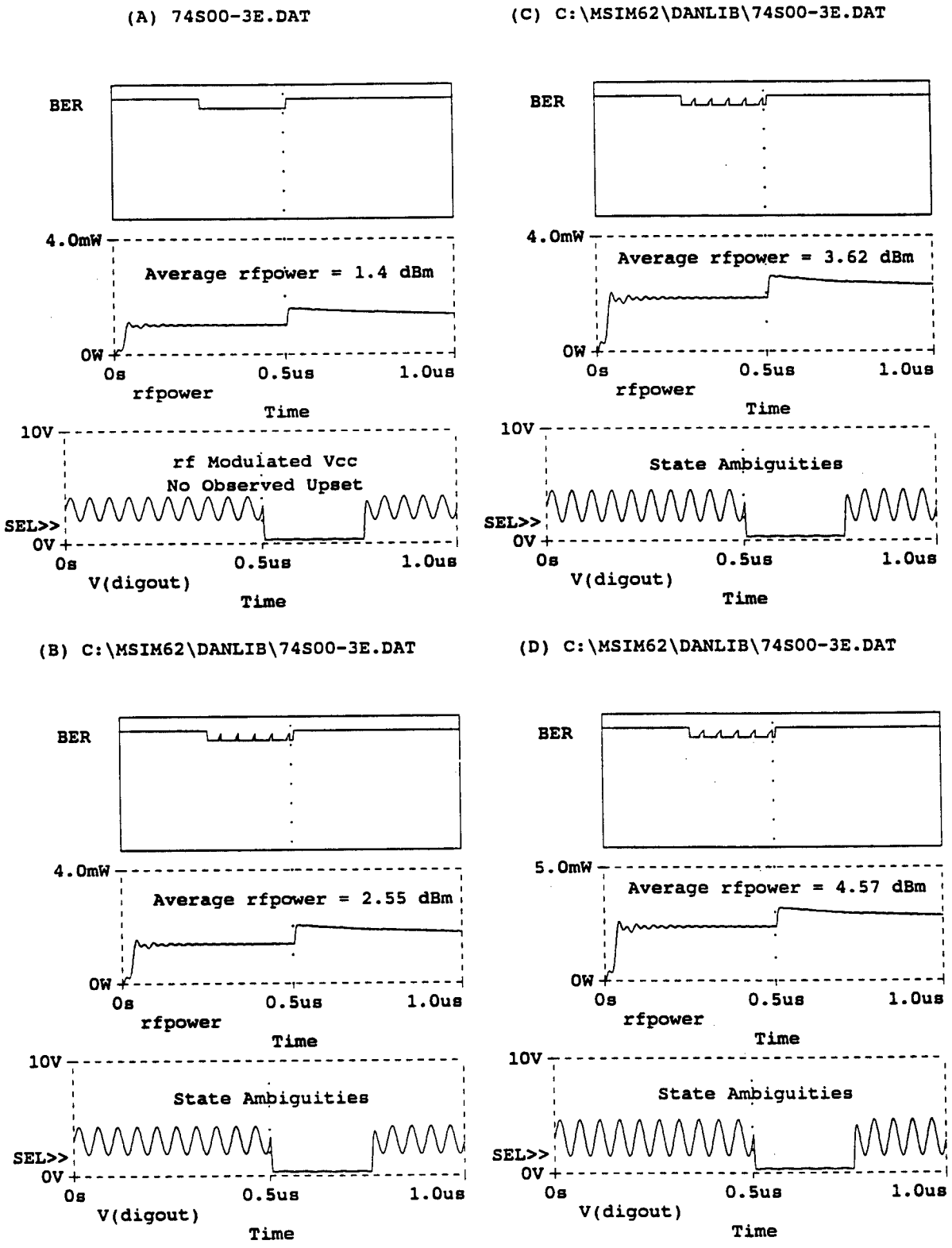
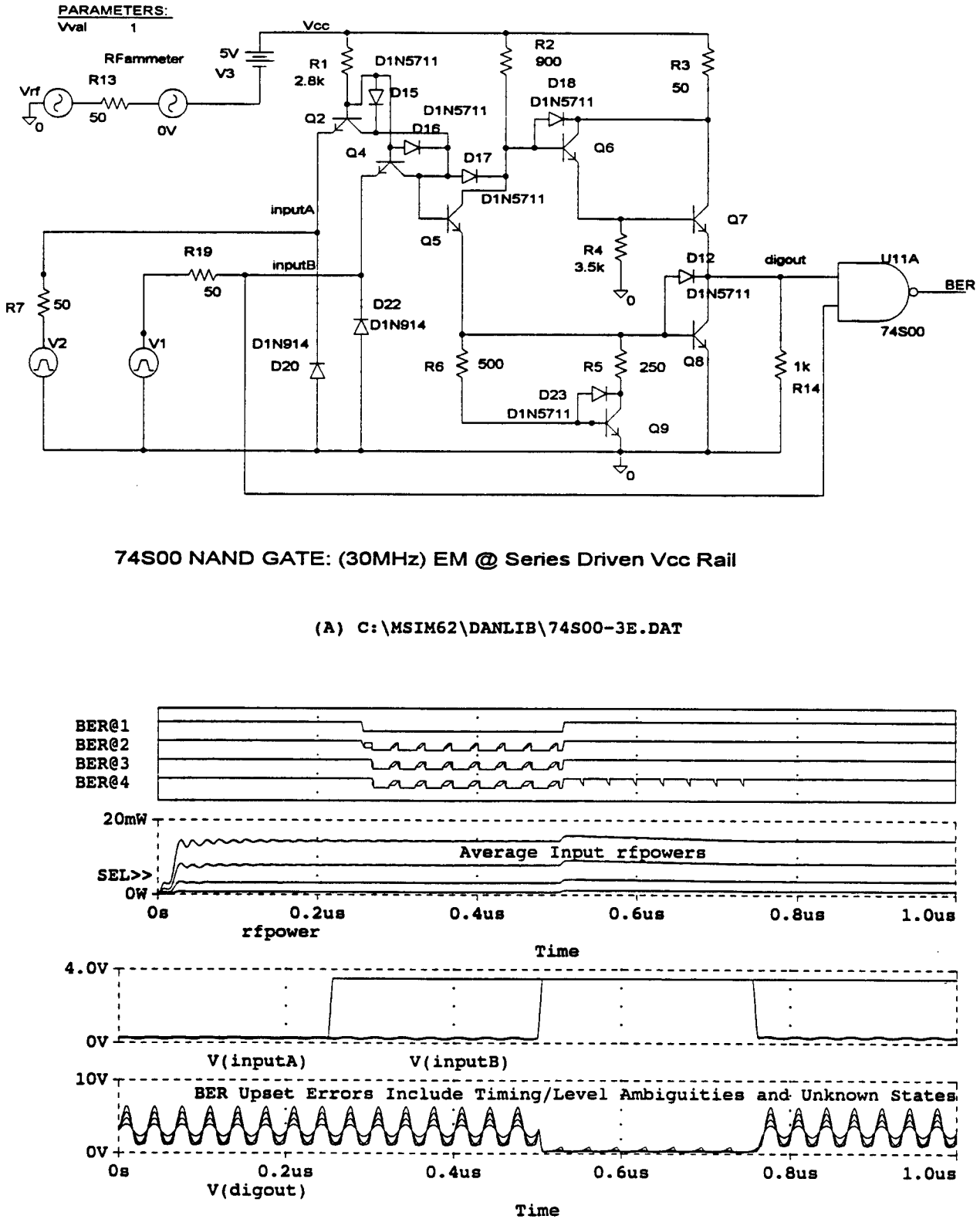


Figure 5-6 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (30MHz) EM @ Series Driven Vcc Rail

(A) C:\MSIM62\DANLIB\74S00-3E.DAT

Figure 5-7 Test Gate with 30 MHz Voltage Source in Series with Vcc Bias Rail

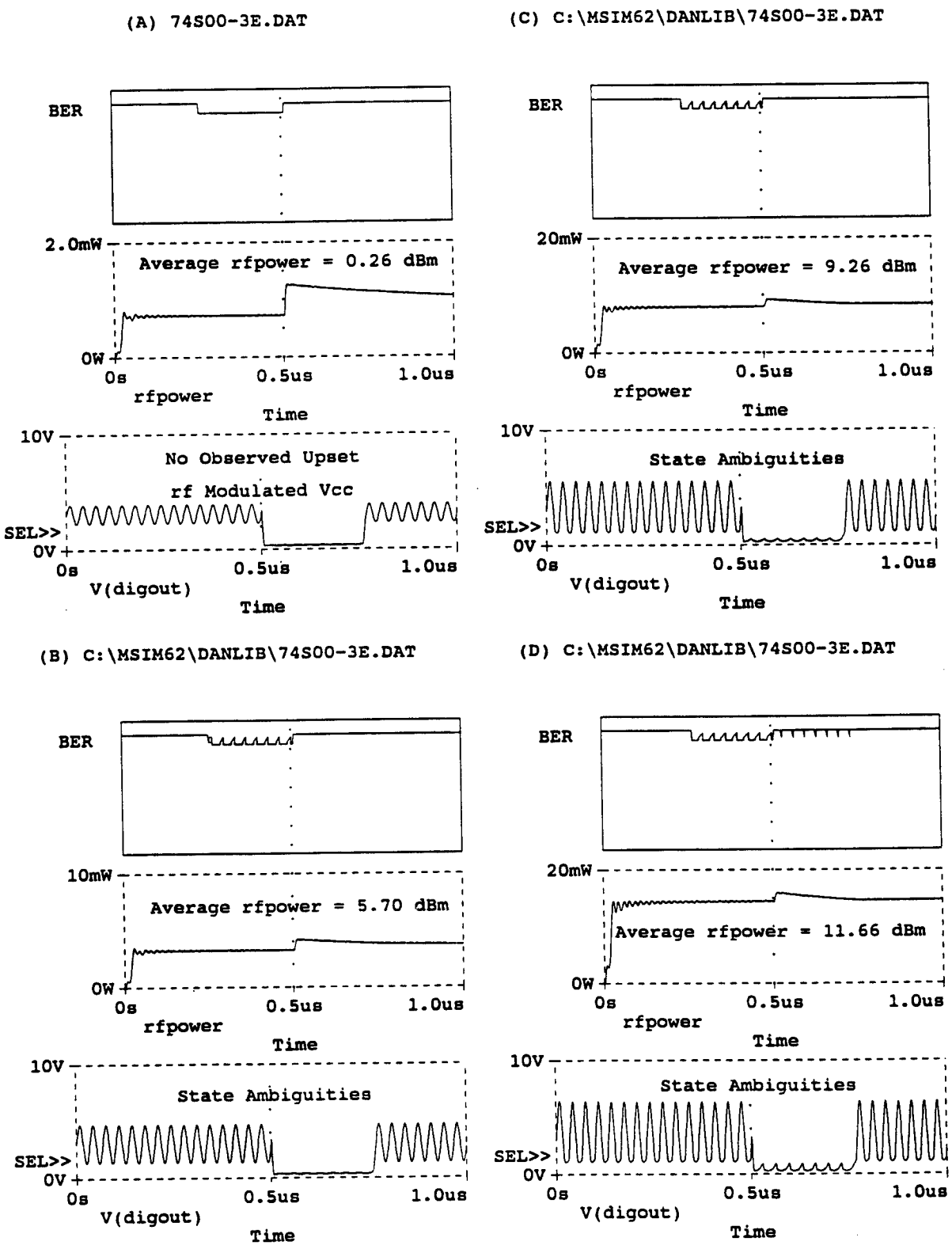
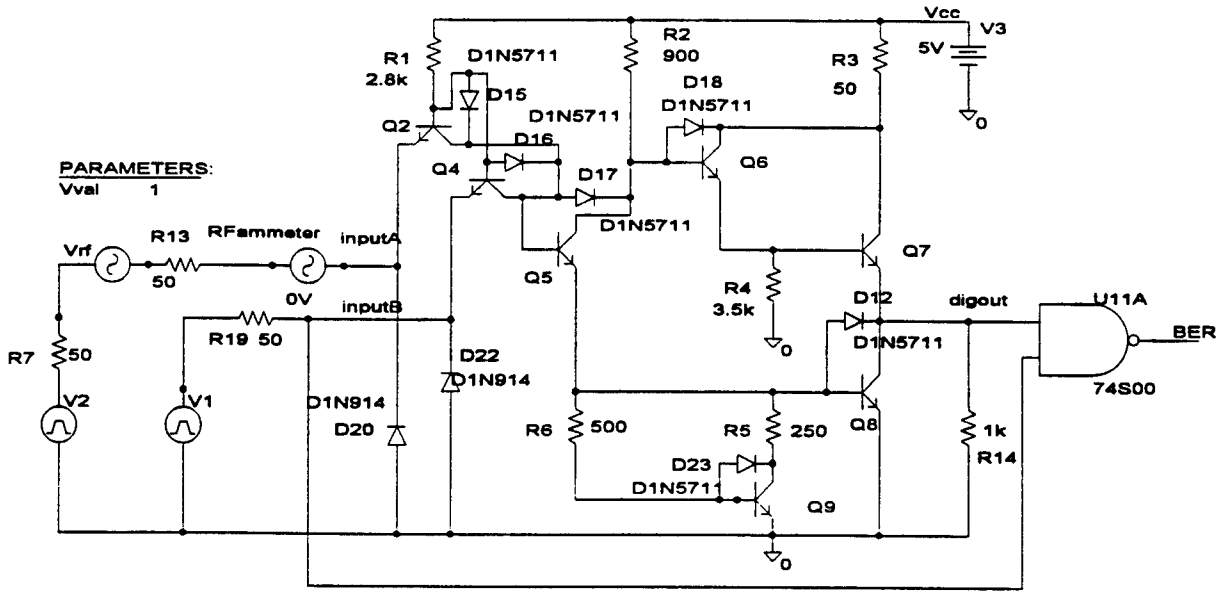


Figure 5-8 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (10MHz) EM Series Driven

(A) C:\MSIM62\DANLIB\74S00-3D.DAT

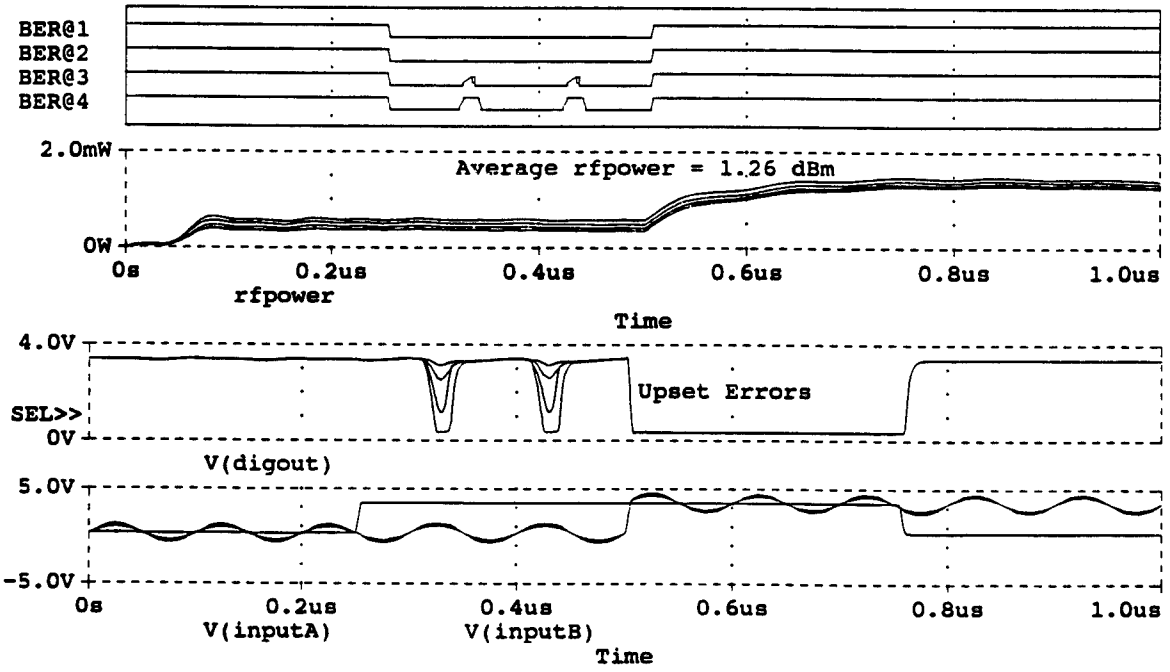


Figure 5-9 Test Gate with 10 MHz Voltage Source in Series with Logic InputA

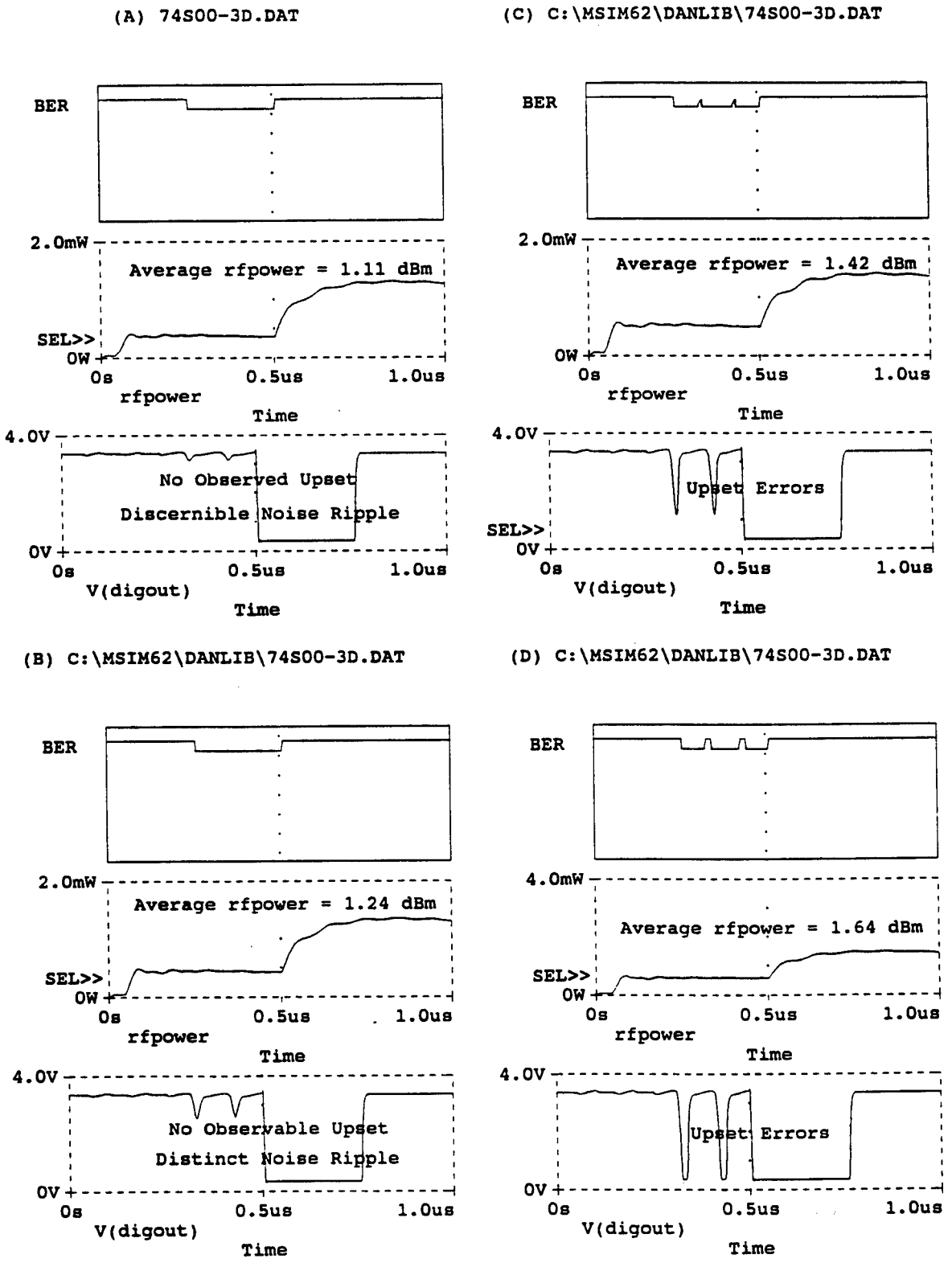
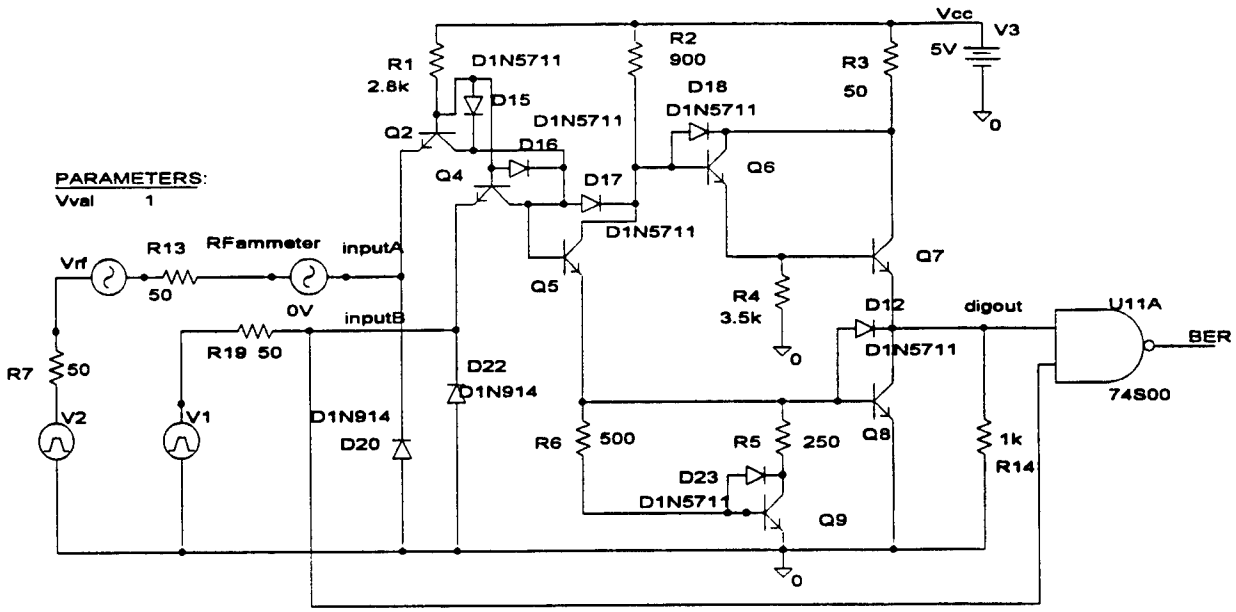


Figure 5-10 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (20MHz) EM Series Driven

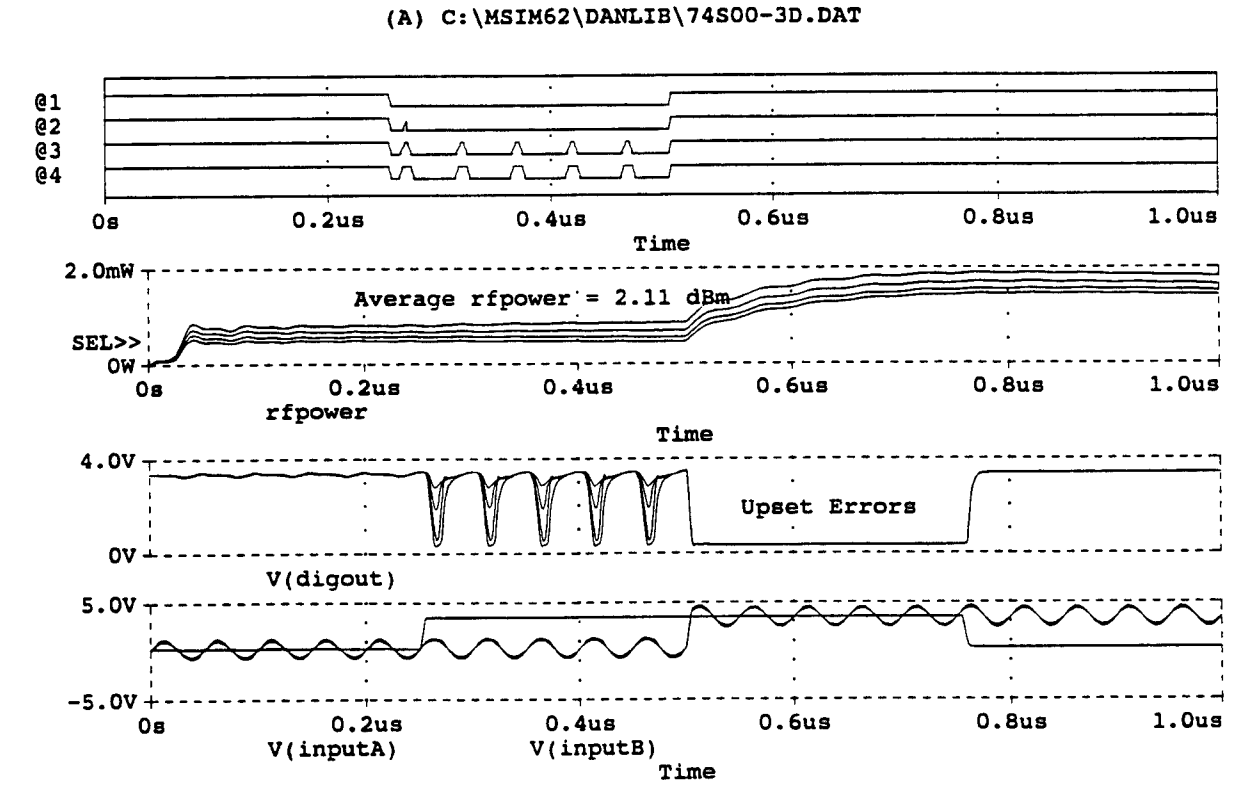


Figure 5-11 Test Gate with 20 MHz Voltage Source in Series with Logic InputA

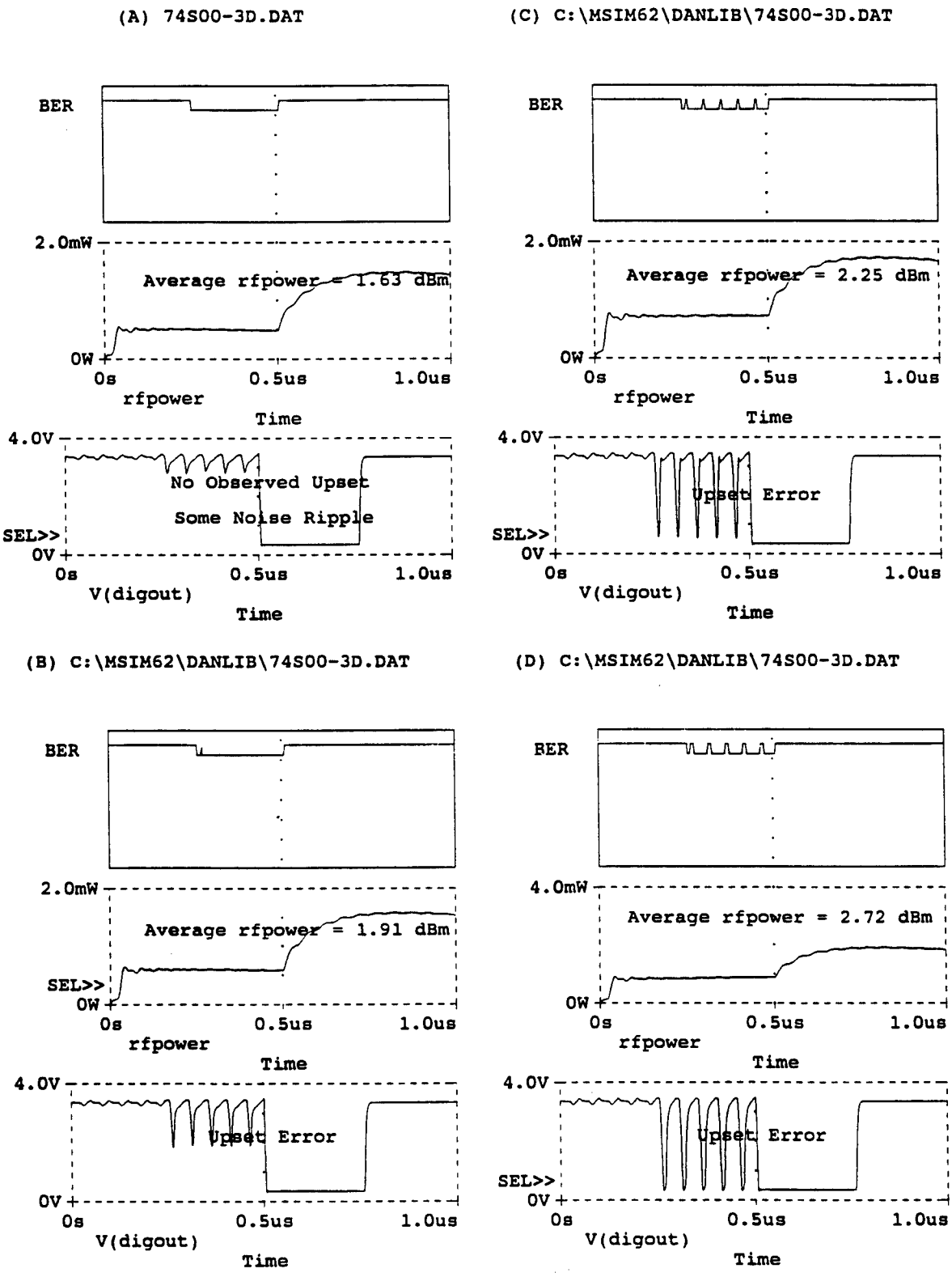
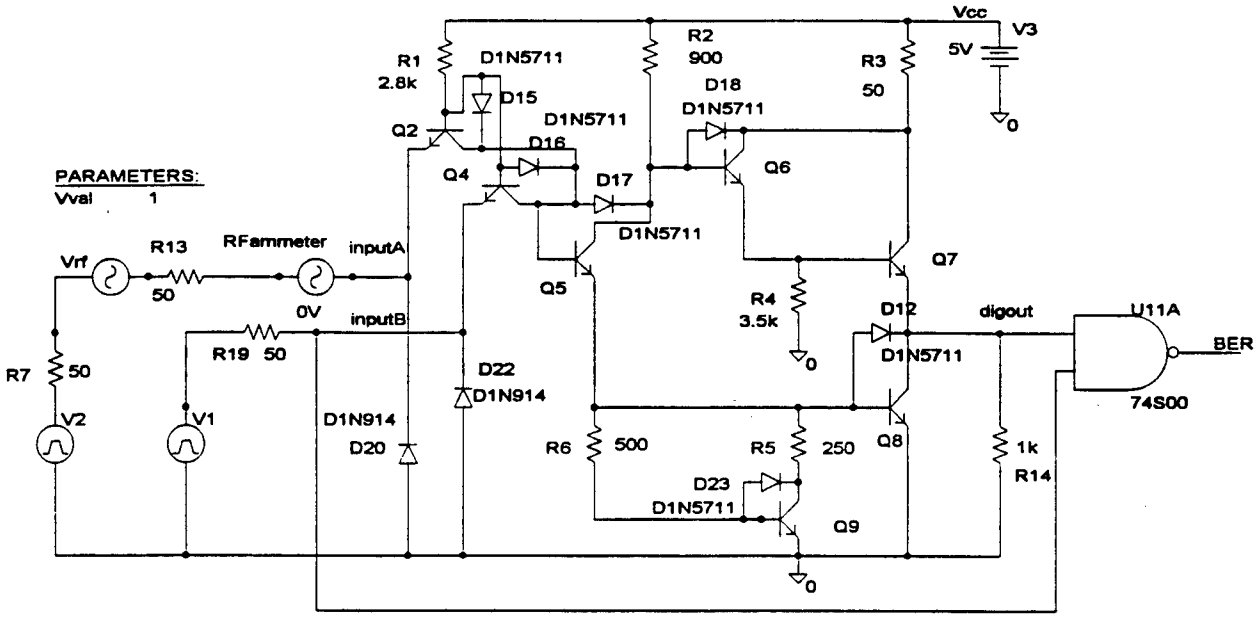


Figure 5-12 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (30MHz) EM Series Driven

(A) C:\MSIM62\DANLIB\74S00-3D.DAT

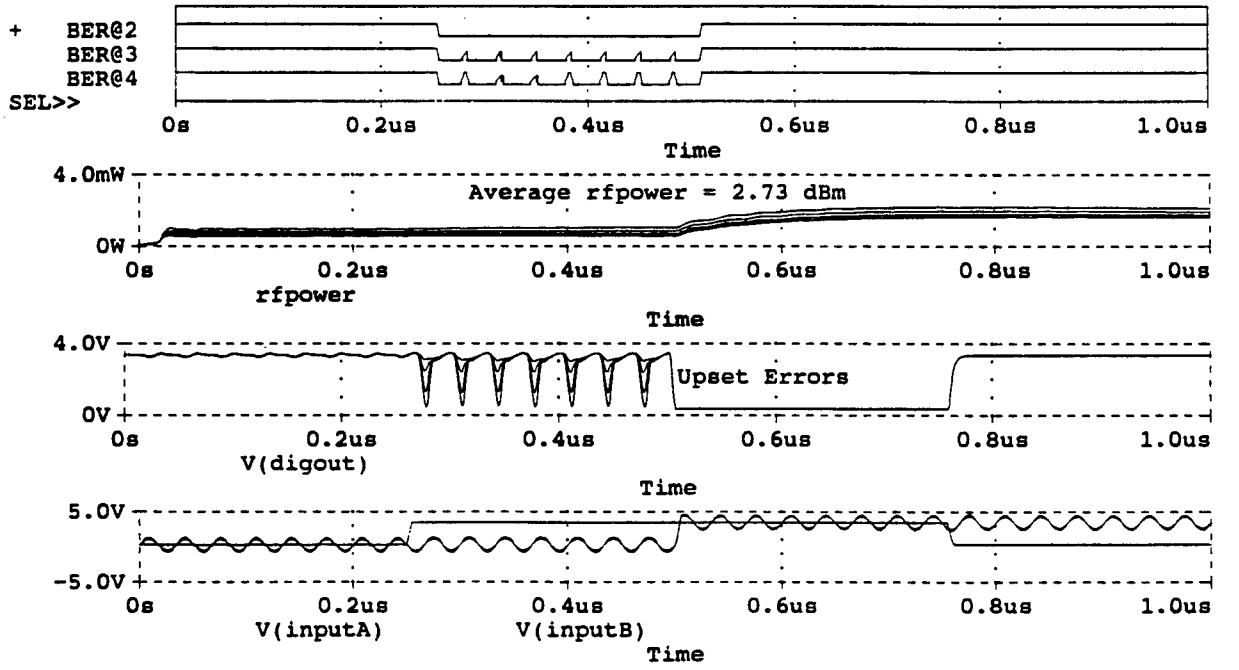


Figure 5-13 Test Gate with 30 MHz Voltage Source in Series with Logic InputA

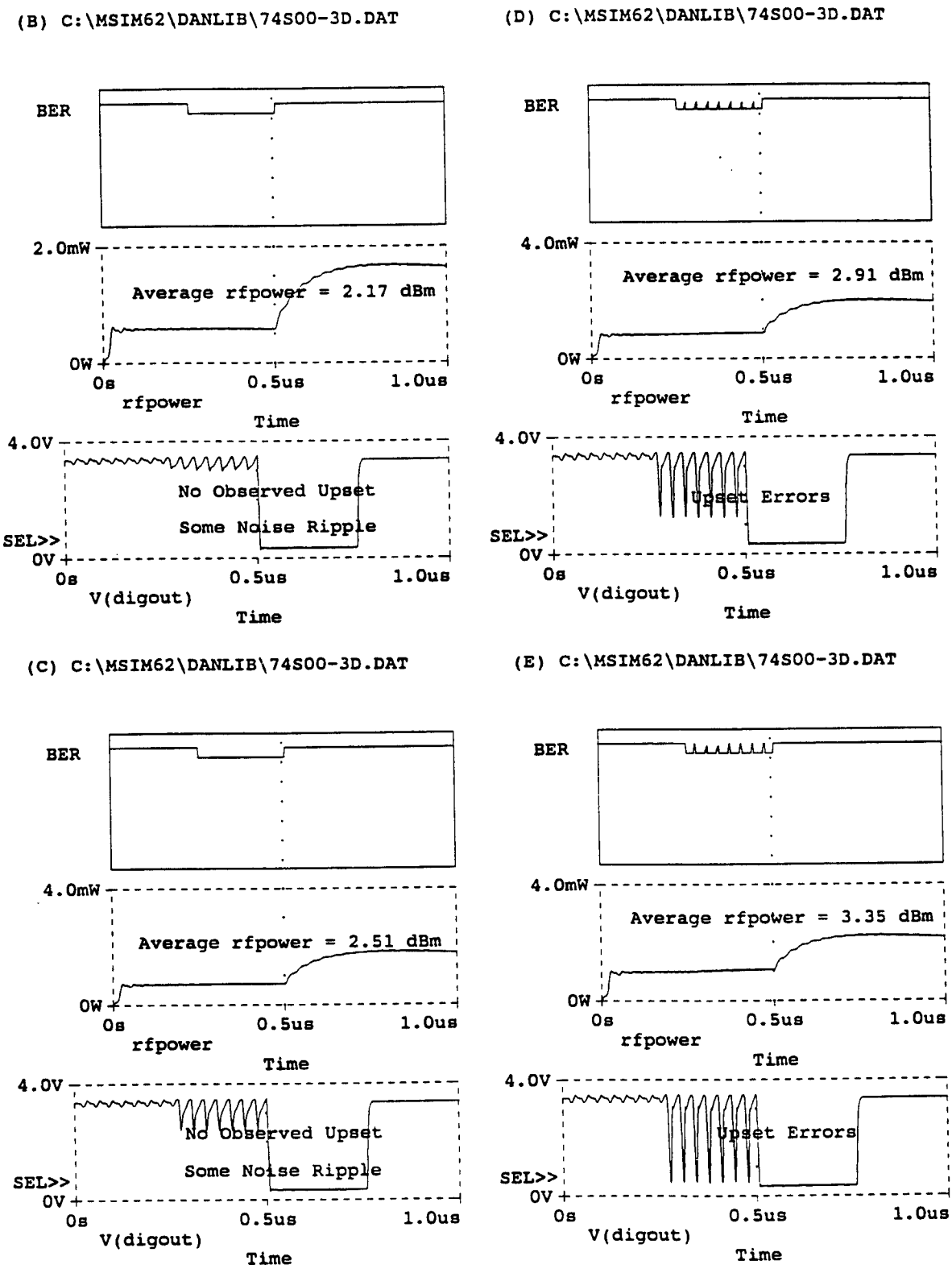
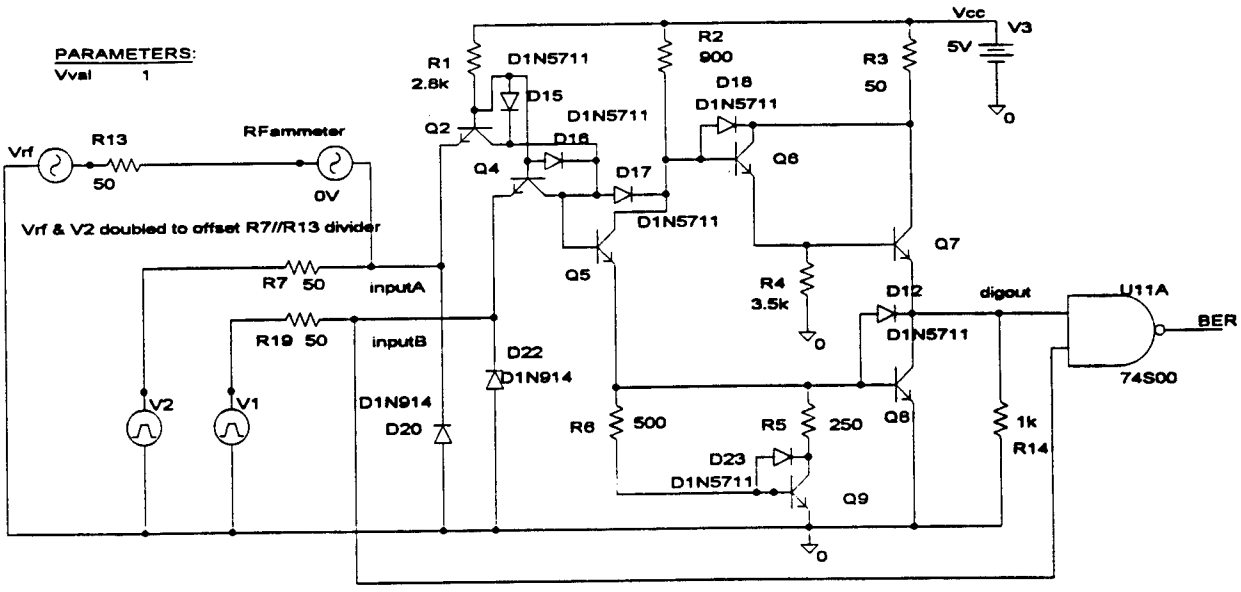


Figure 5-14 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (10MHz) EM Parallel Driven

(A) C:\MSIM62\DANLIB\74S00-3B.DAT

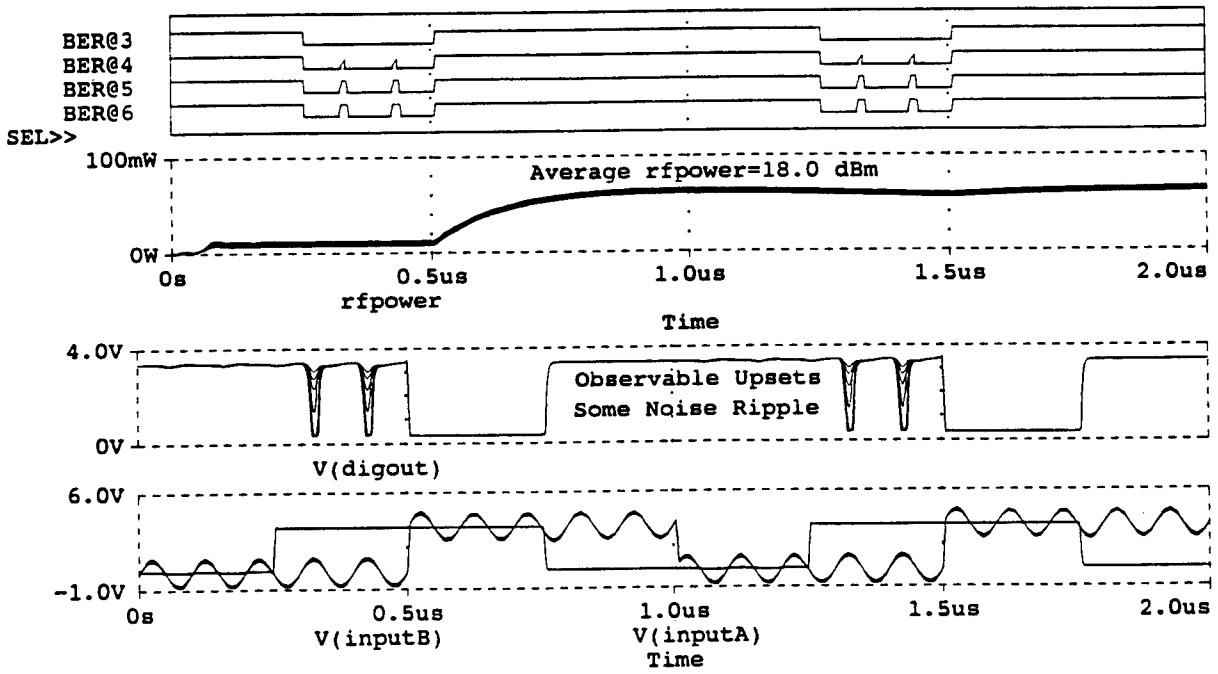


Figure 5-15 Test Gate with 10 MHz Voltage Source in Parallel with Logic InputA

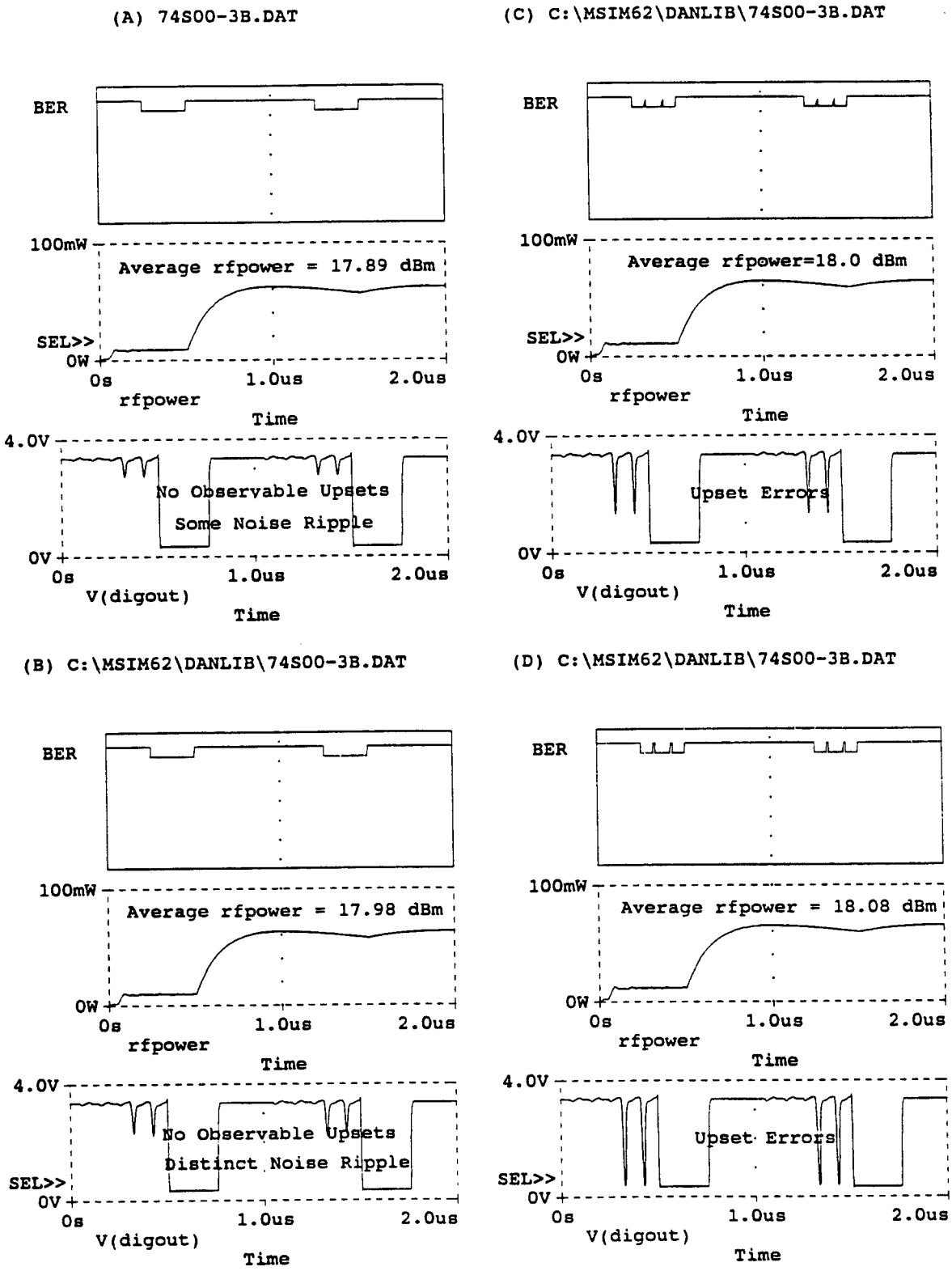
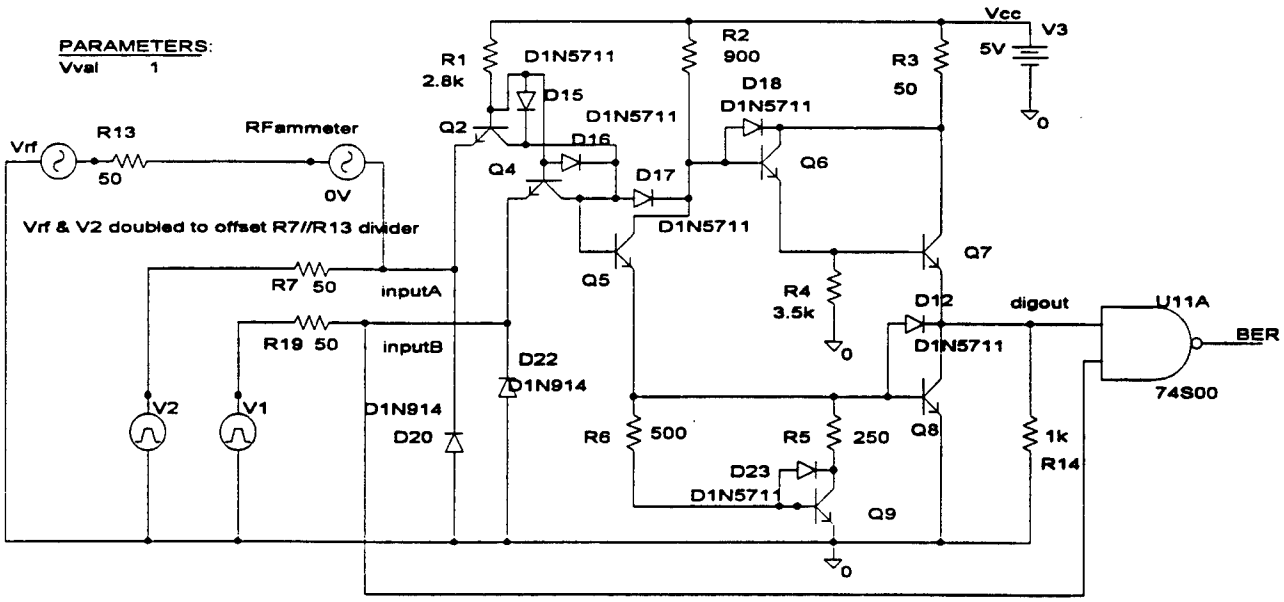


Figure 5-16 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (20MHz) EM Parallel Driven

(A) C:\MSIM62\DANLIB\74S00-3B.DAT

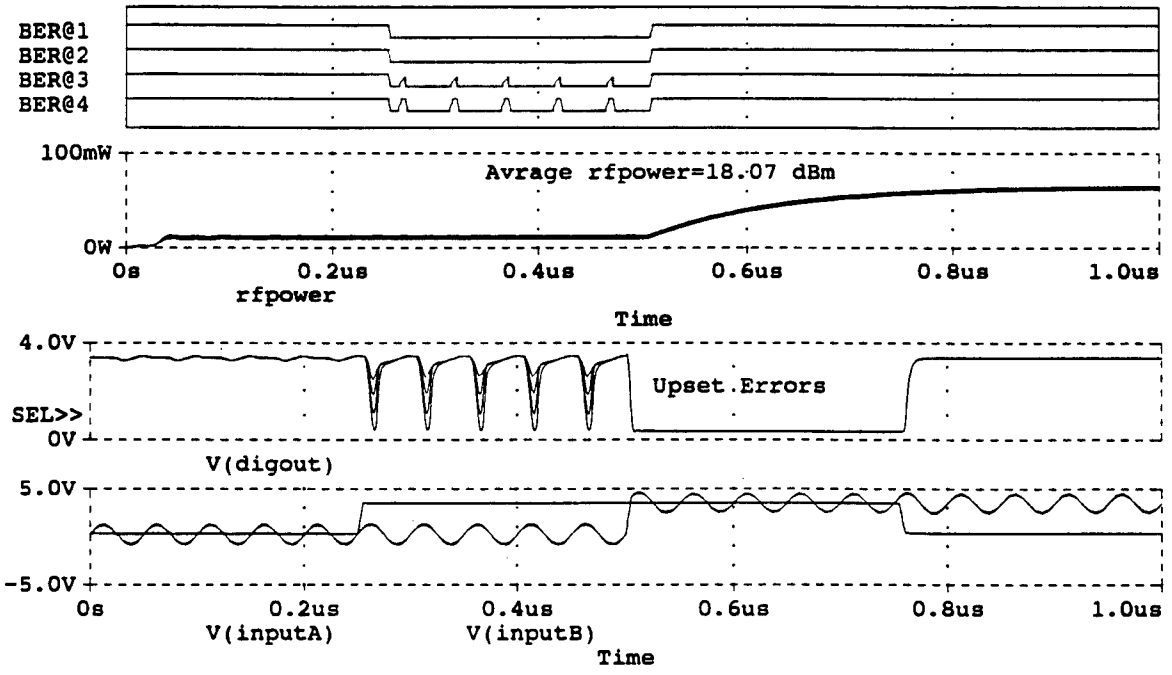


Figure 5-17 Test Gate with 20 MHz Voltage Source in Parallel with Logic InputA

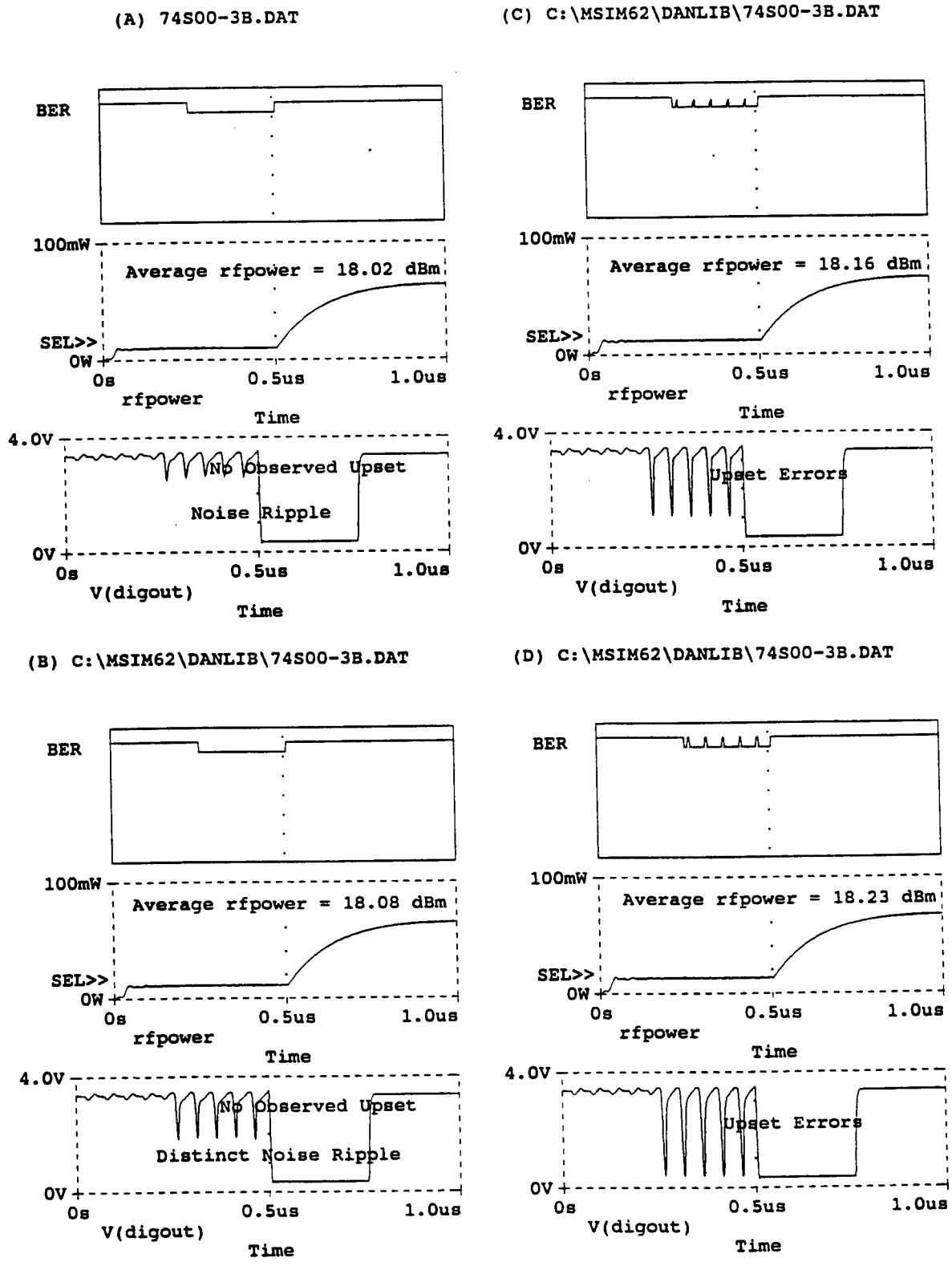
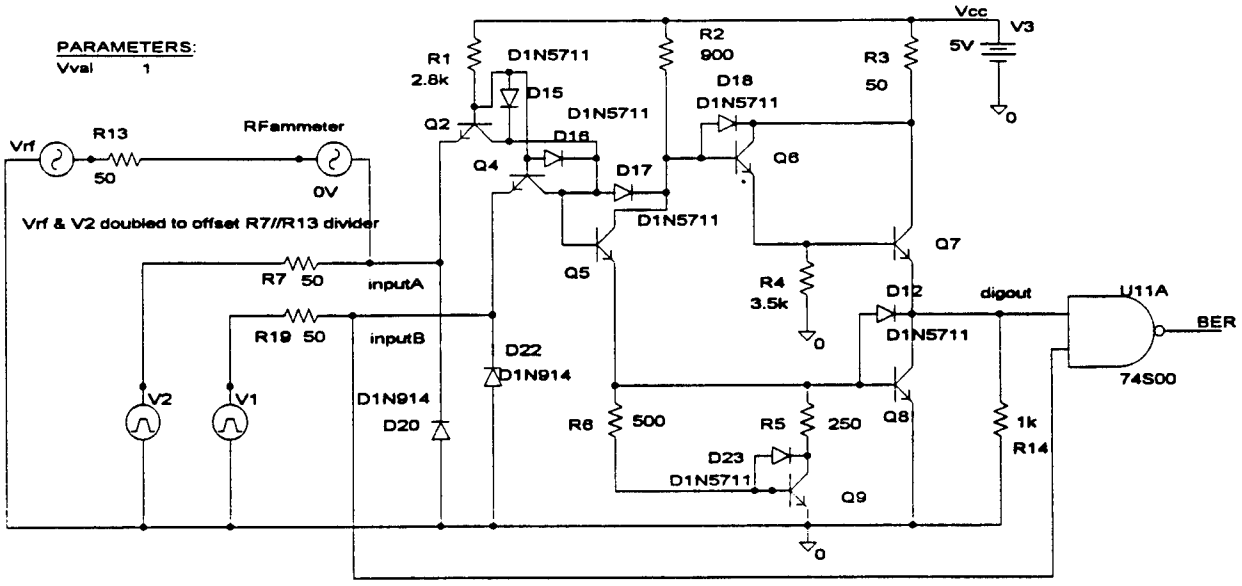


Figure 5-18 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (30MHz) EM Parallel Driven

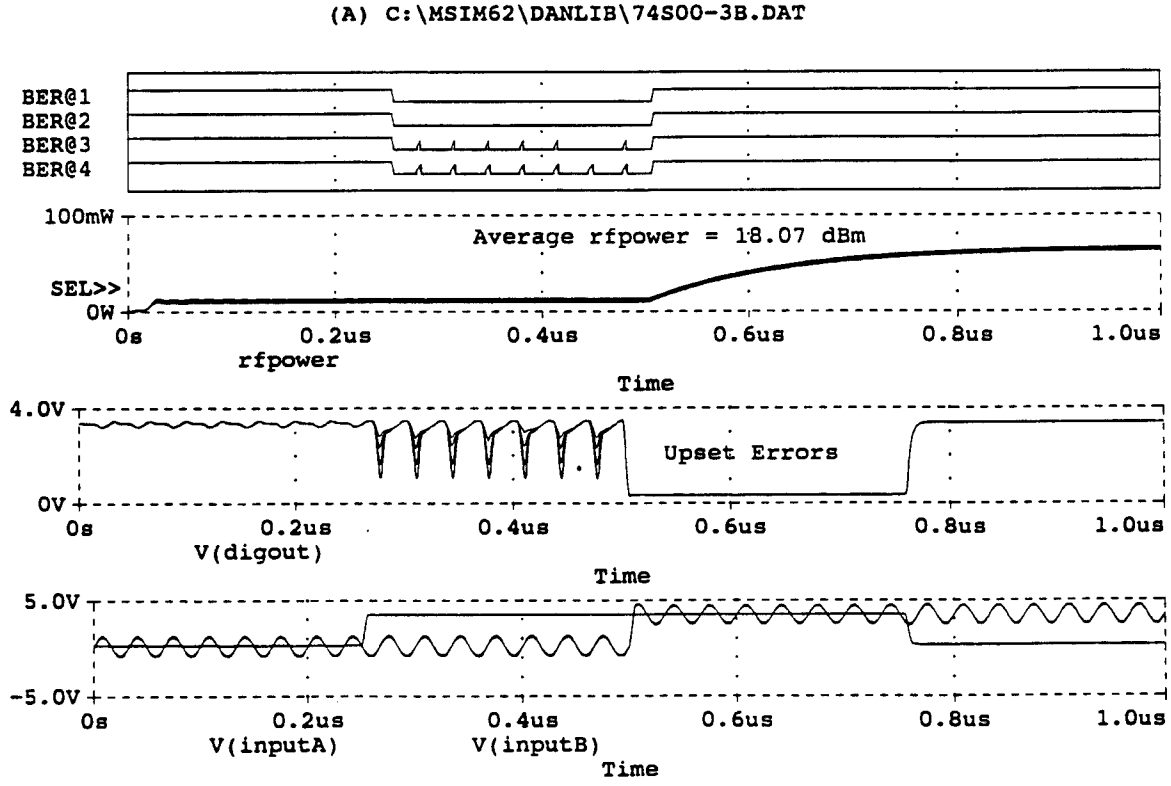


Figure 5-19 Test Gate with 30 MHz Voltage Source in Parallel with Logic InputA

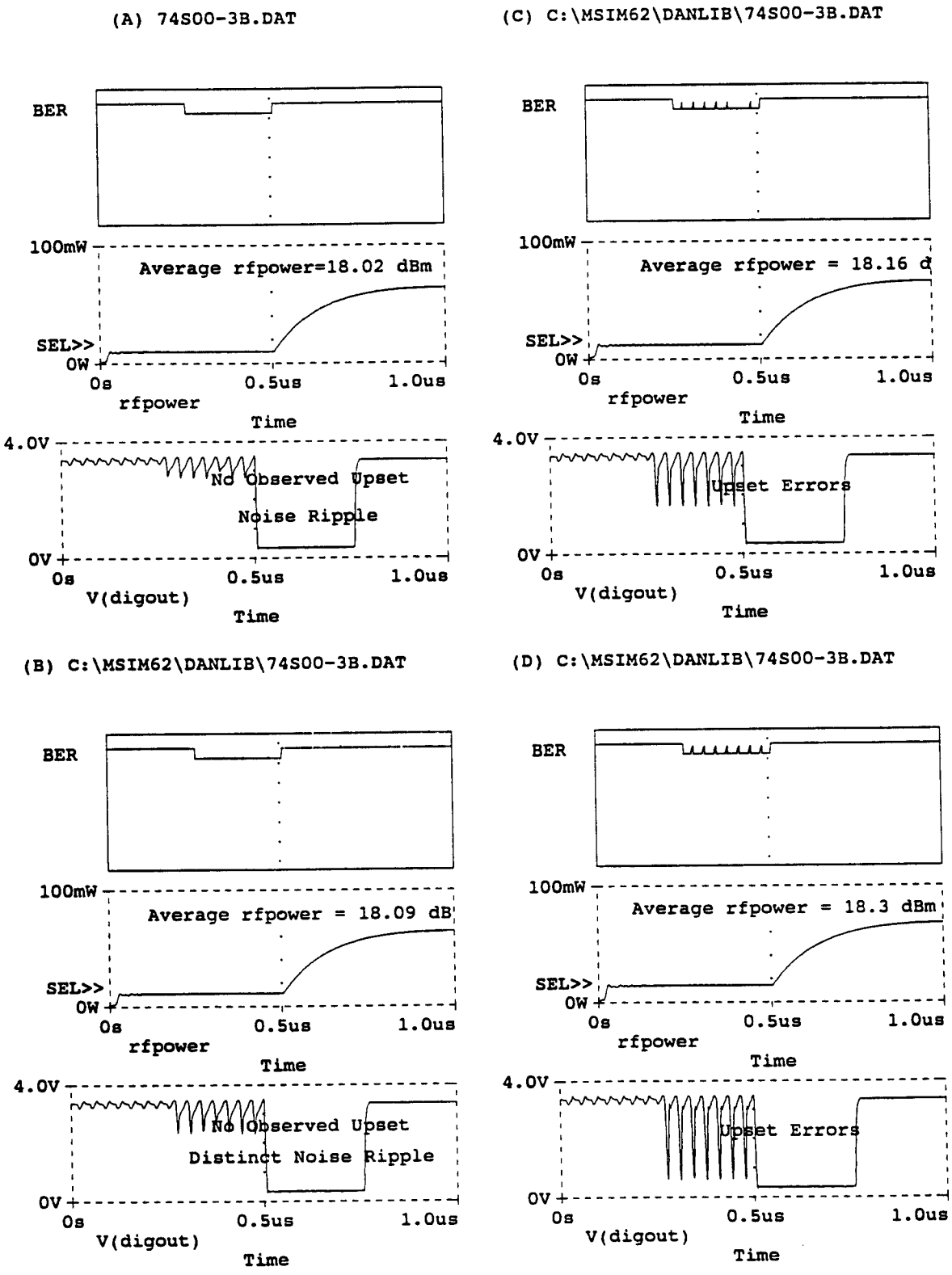
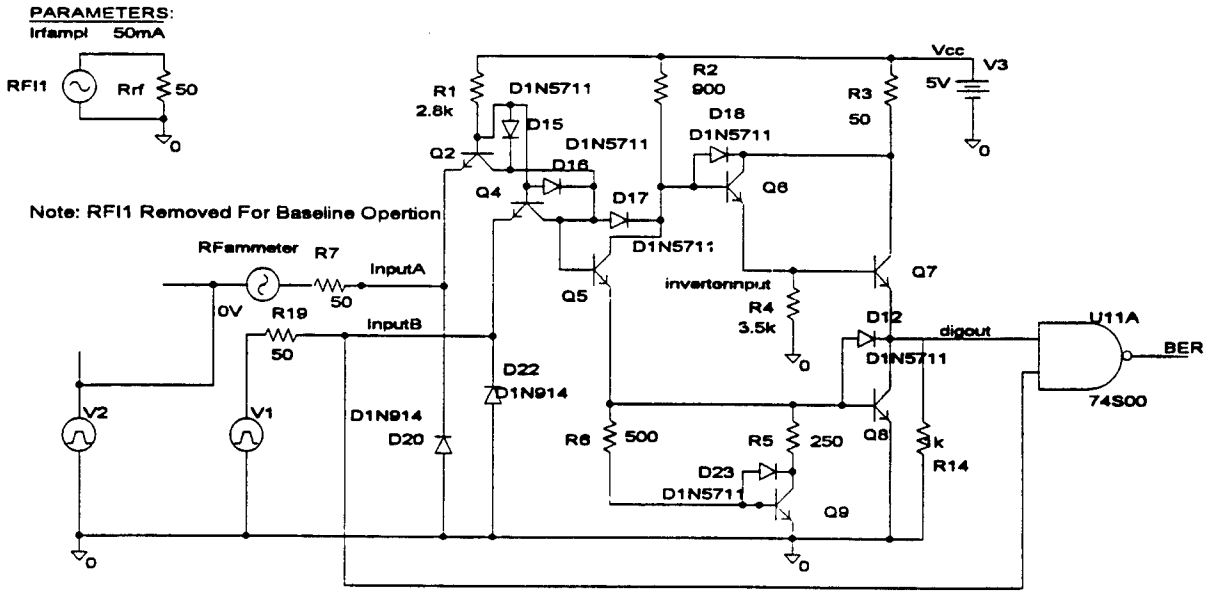


Figure 5-20 Detail Data Susceptibility Build-Up



74S00 NAND GATE: BASELINE OPERATION

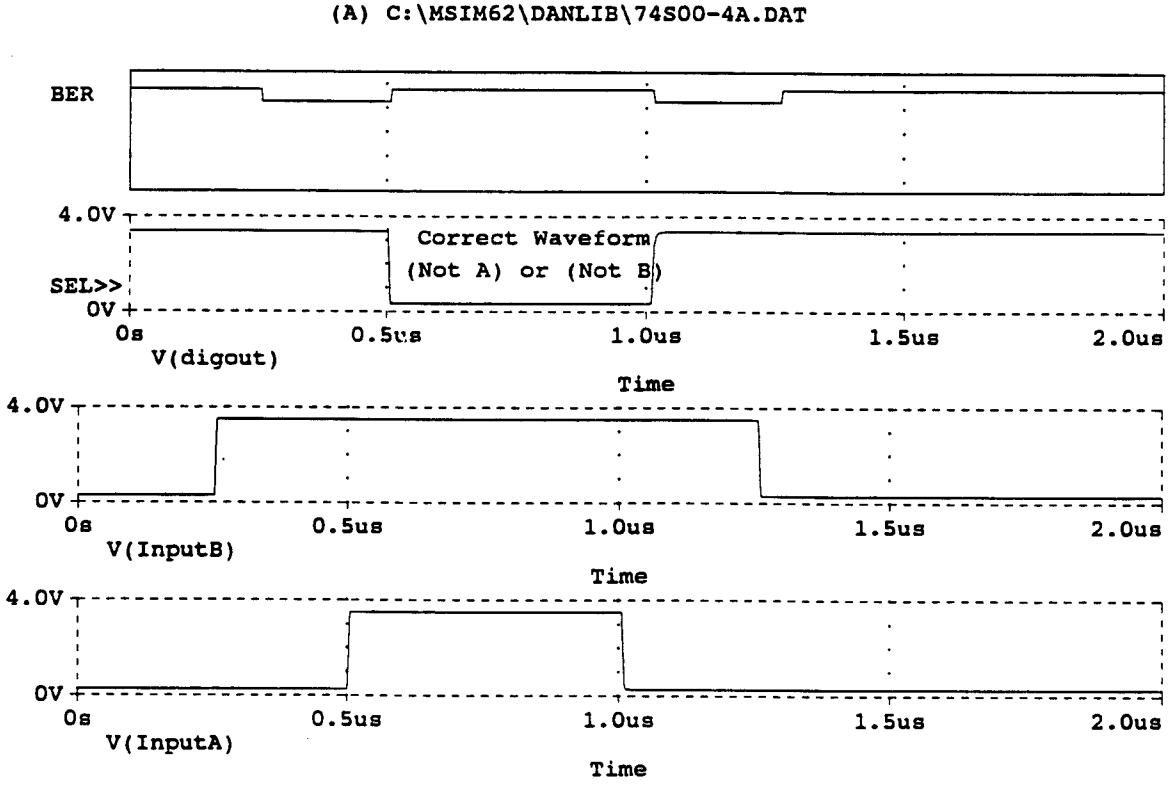
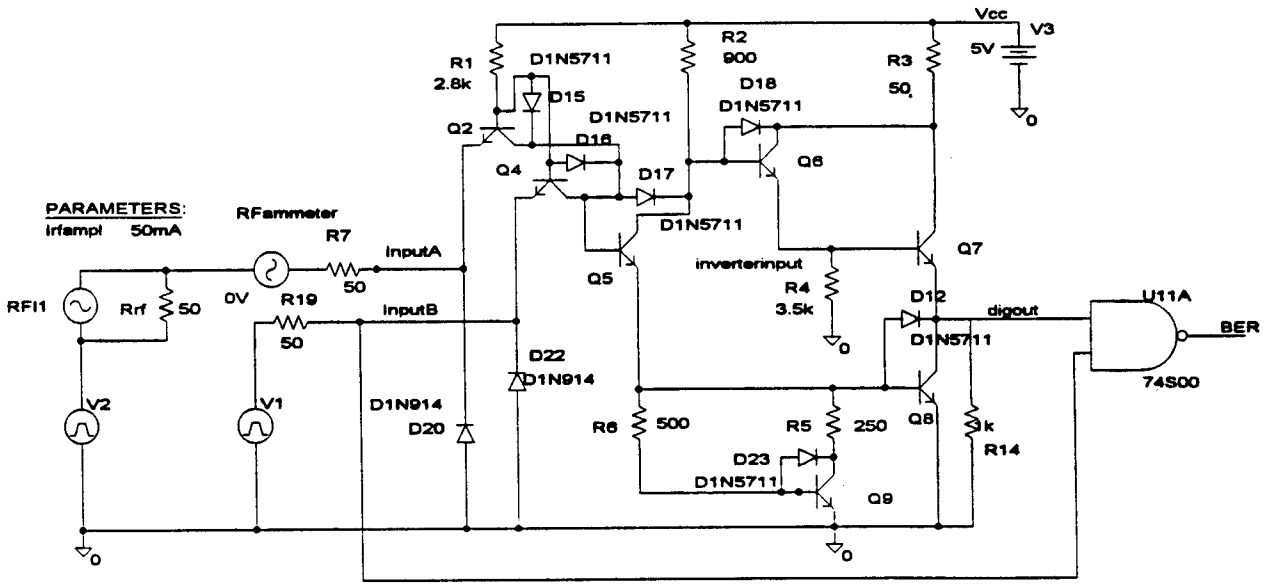


Figure 5-21 Baseline Gate and Logic Responses for Current Source Testing



74S00 NAND GATE: (30 MHz) EM ISource @ Series Driven InputA

(A) C:\MSIM62\DANLIB\74S00-4A.DAT

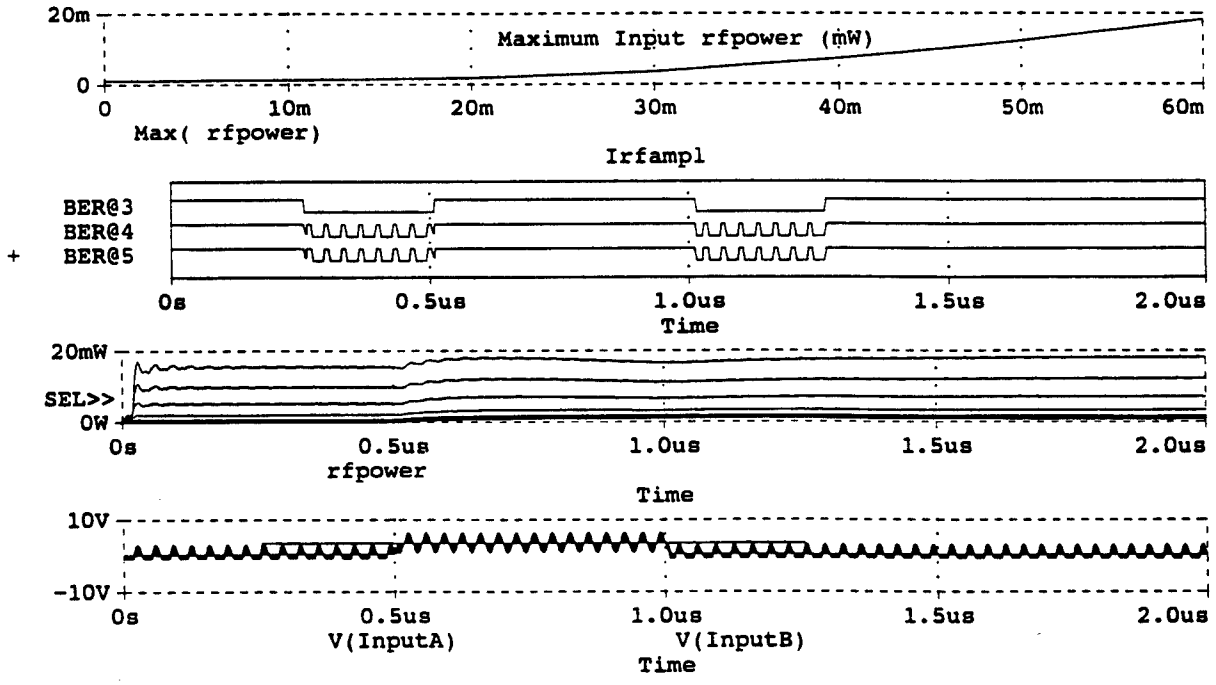


Figure 5-22 Test Gate with 30 MHz Current Source in Series with Logic InputA

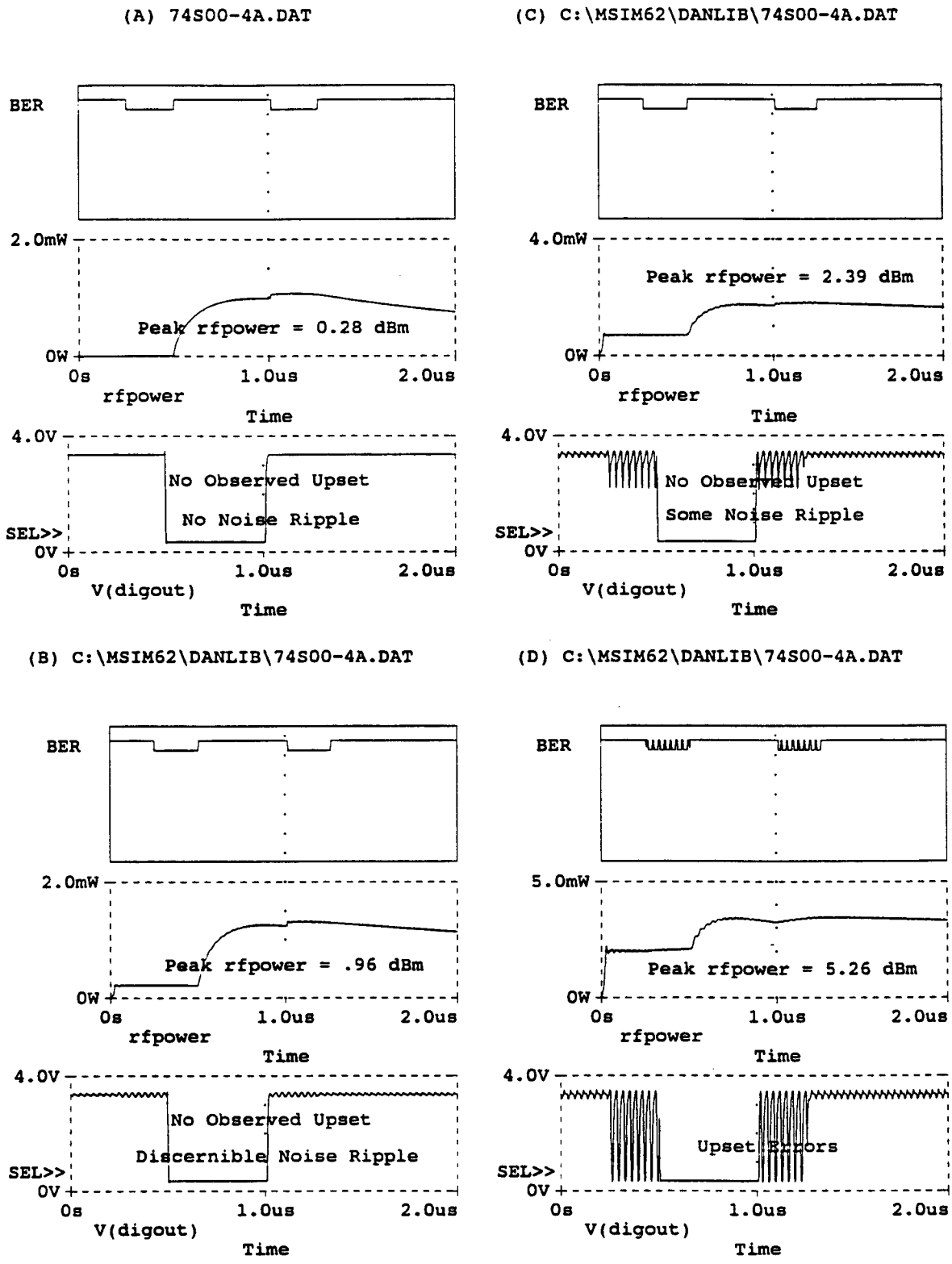
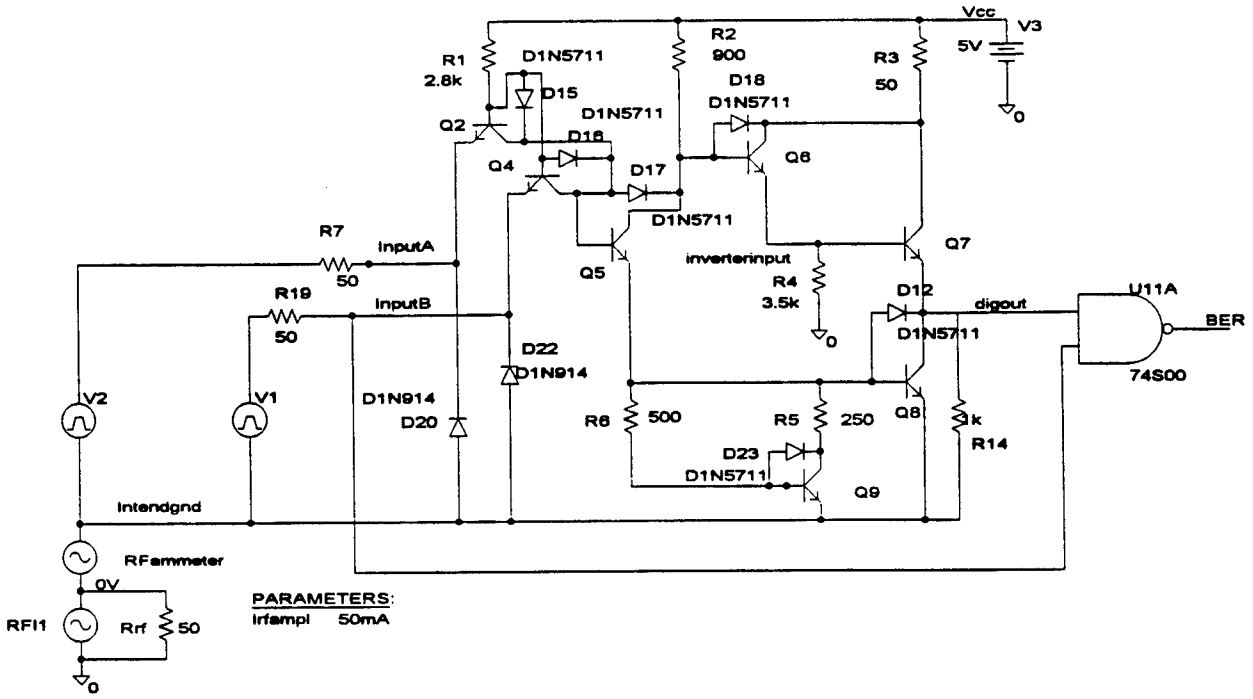


Figure 5-23 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (30 MHz) EM ISource @ Series Driven Intended Ground

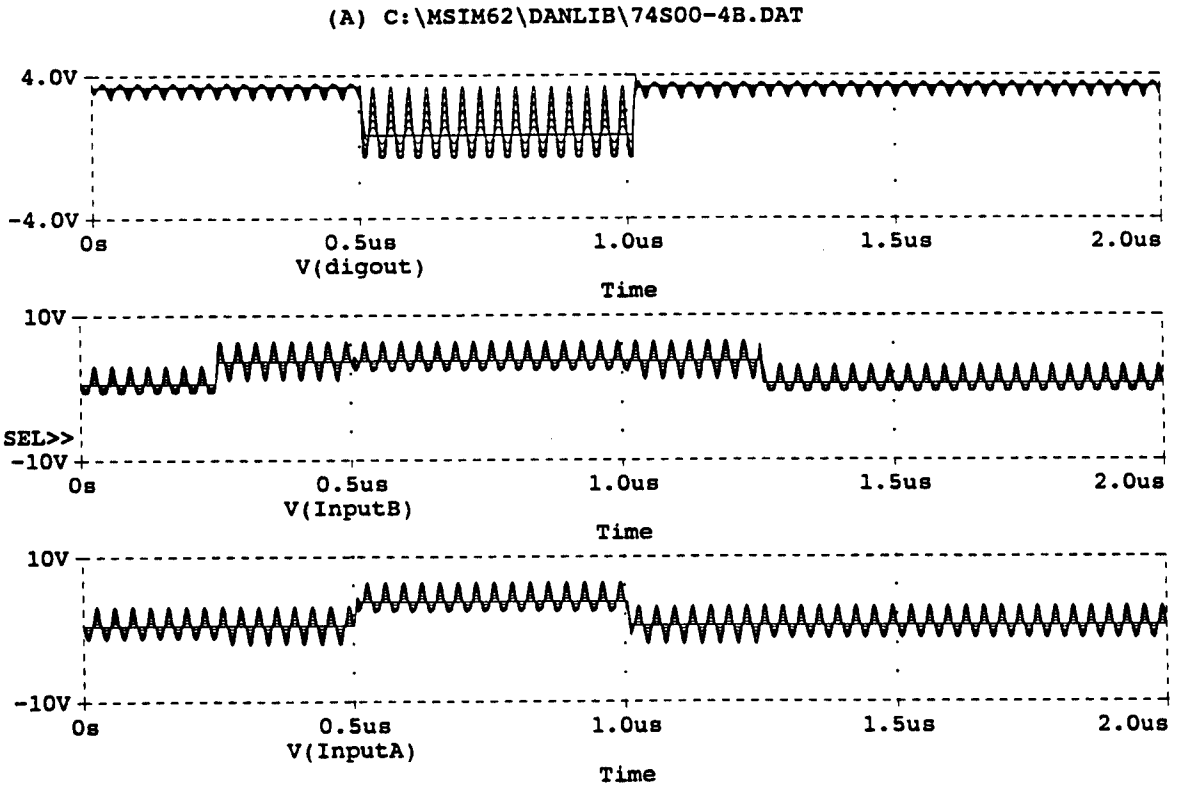


Figure 5-24 Test Gate with 30 MHz Current Source in Series with Intended Ground

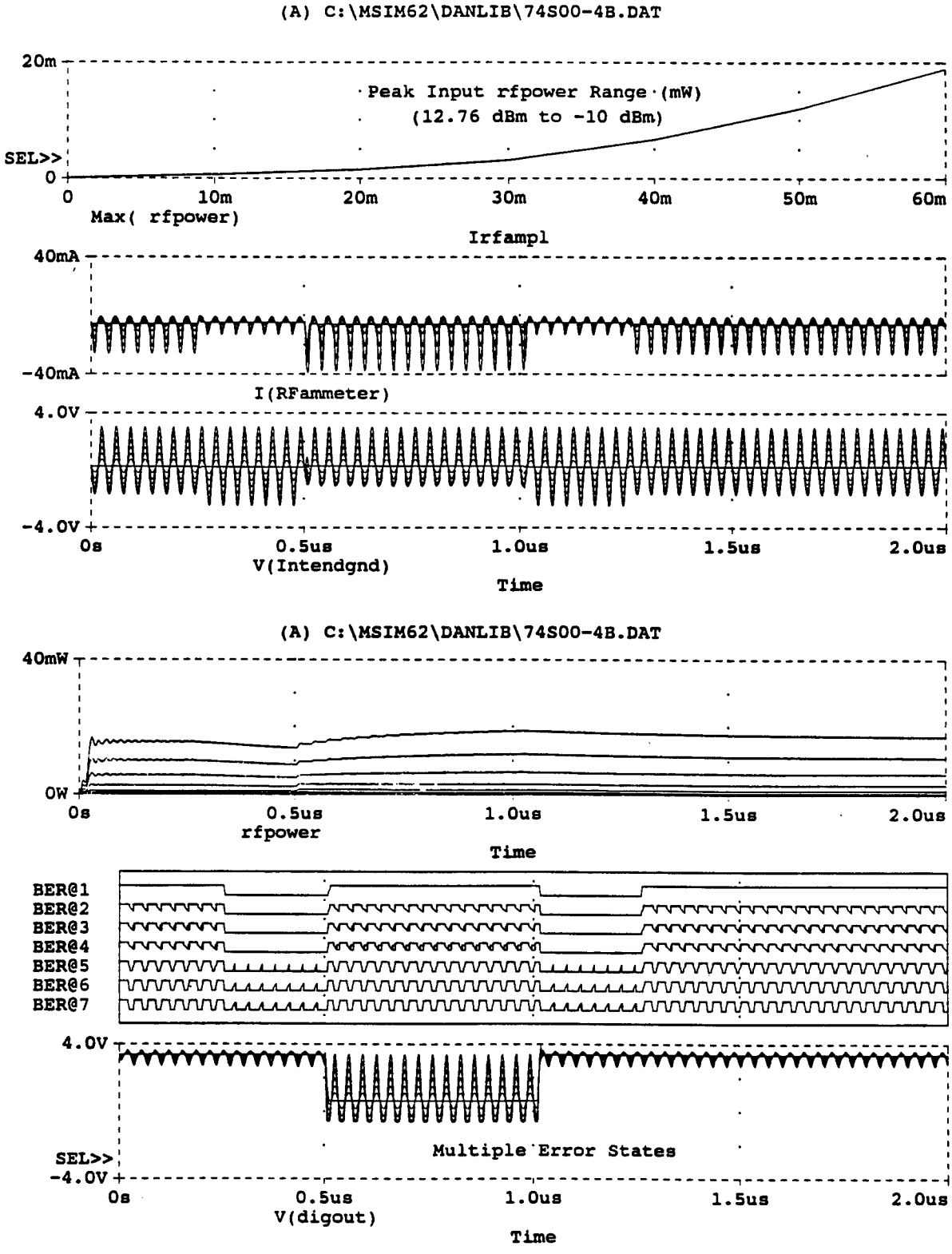
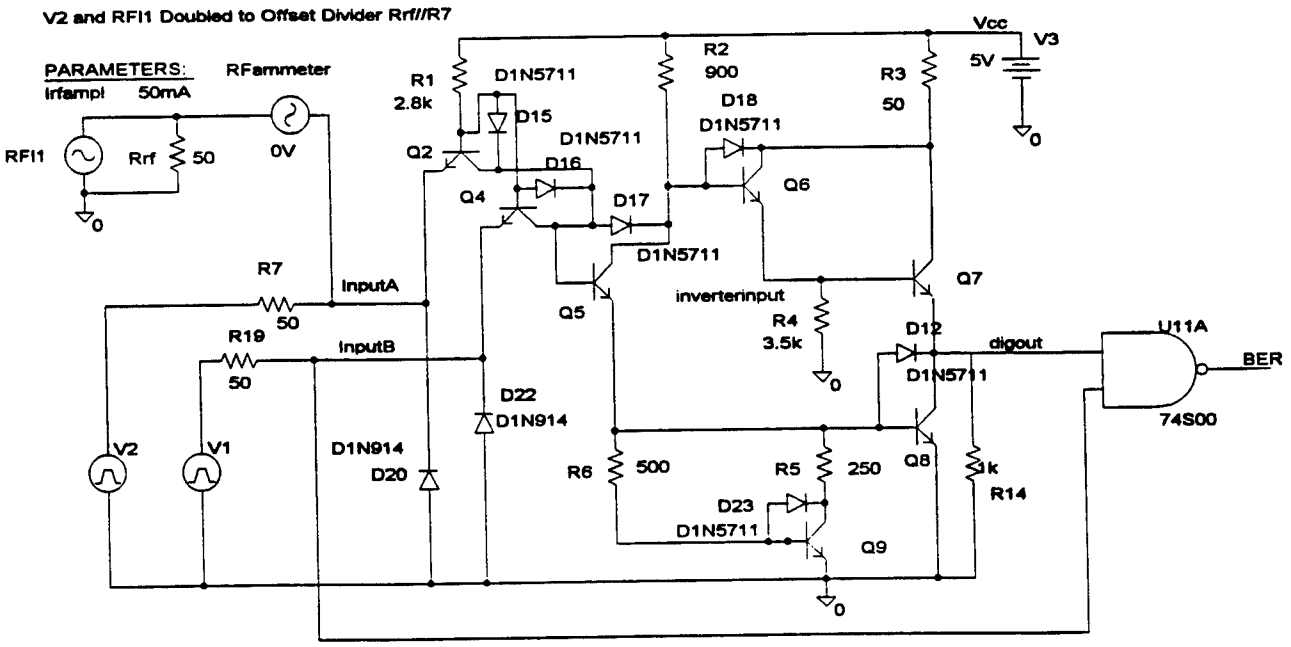


Figure 5-25 Detail Data susceptibility Build-Up



74S00 NAND GATE: (10 MHz) EM ISource @ Parallel Driven InputA

(A) C:\MSIM62\DANLIB\74S00-4A.DAT

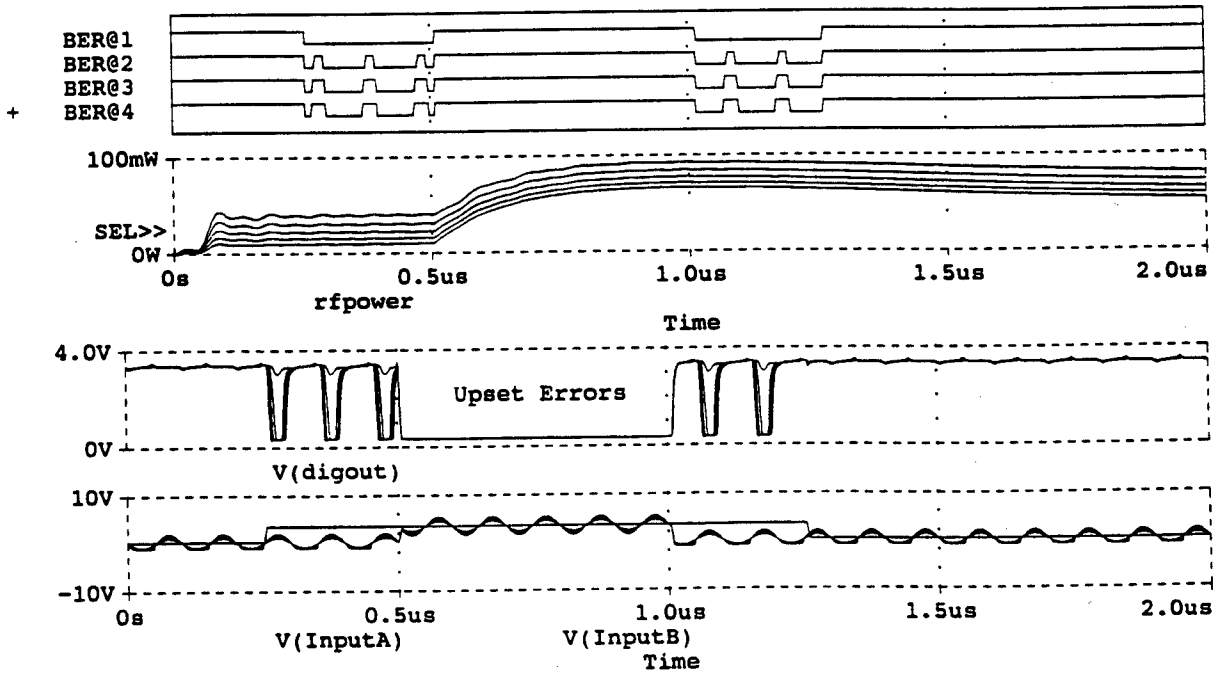


Figure 5-26 Test Gate with 10 MHz Current Source in Parallel with Logic InputA

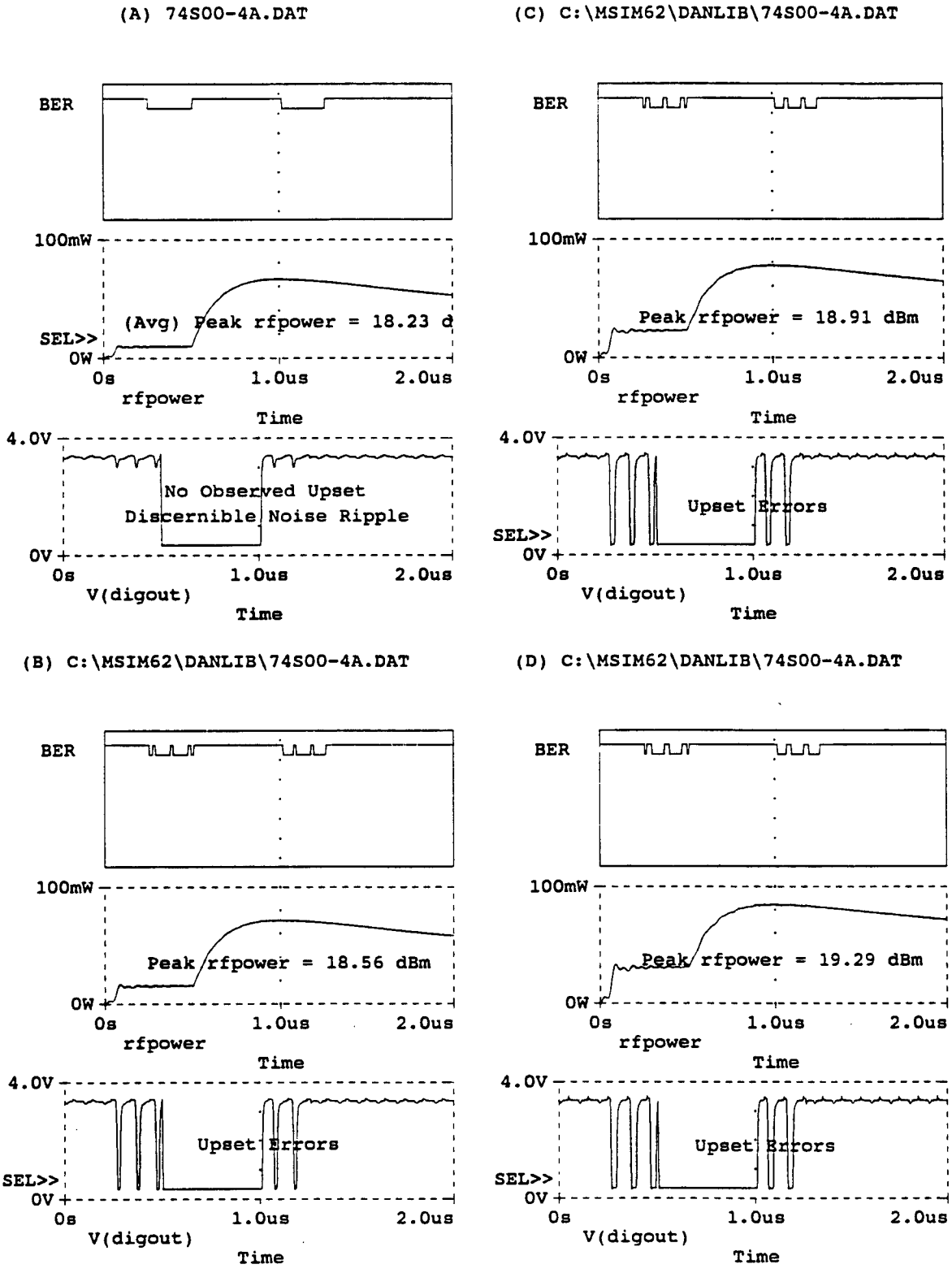
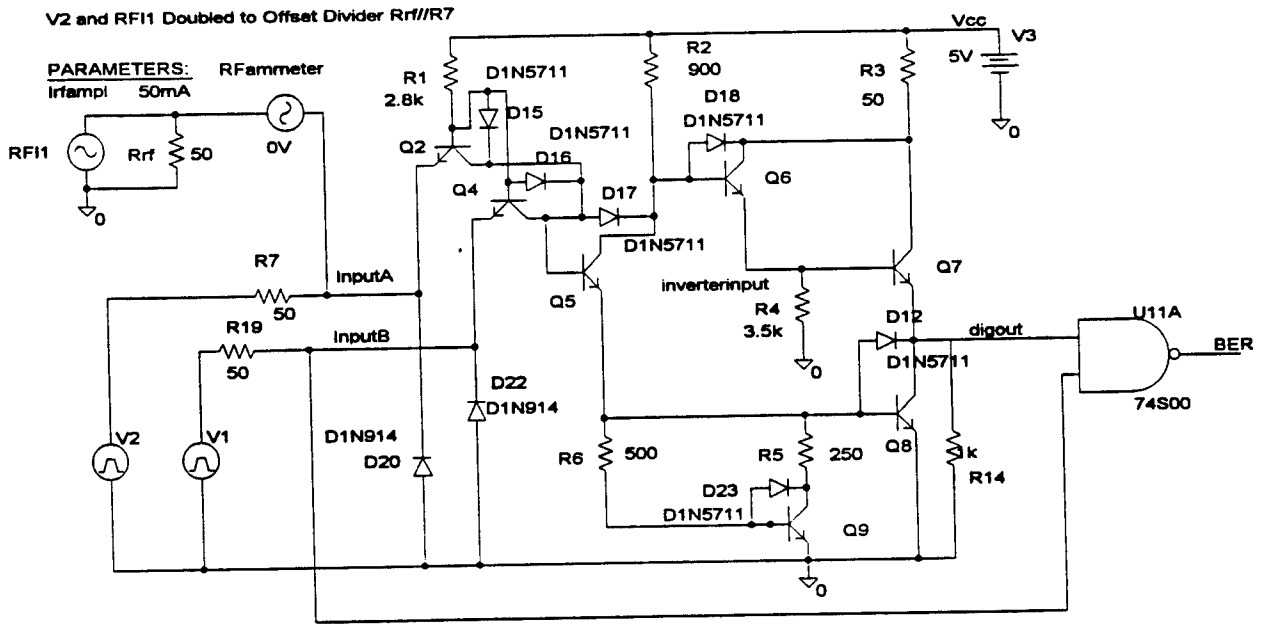


Figure 5-27 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (20 MHz) EM ISource @ Parallel Driven InputA

(A) C:\MSIM62\DANLIB\74S00-4A.DAT

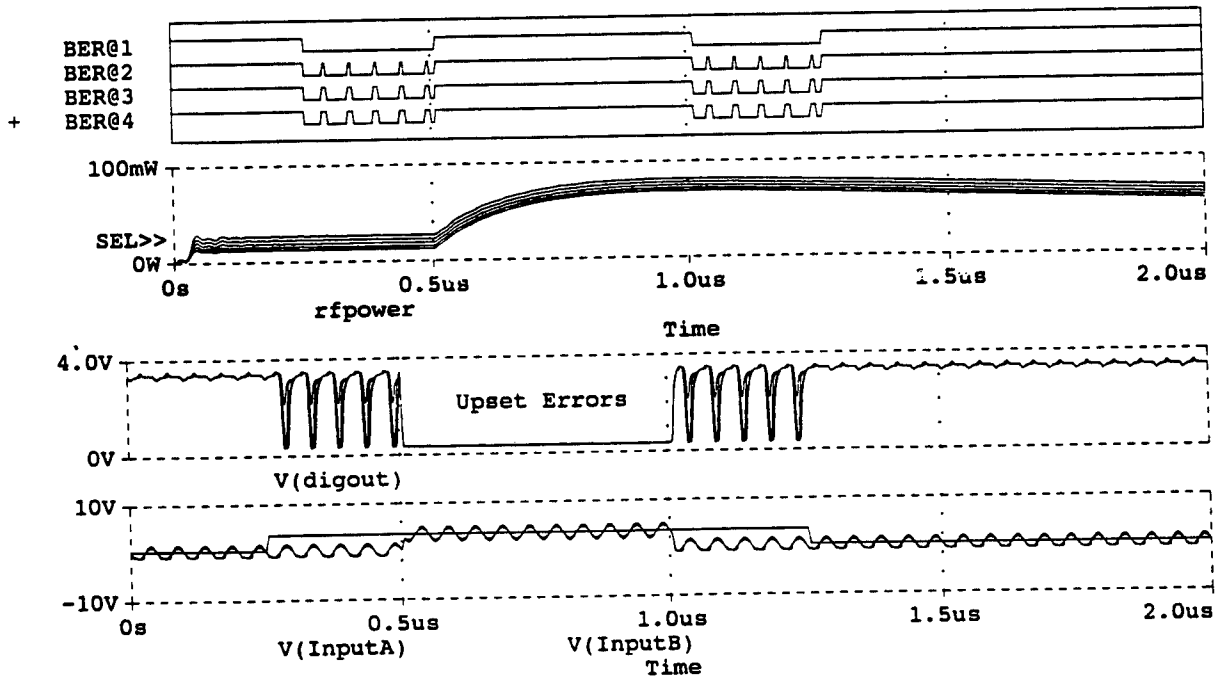


Figure 5-28 Test Gate with 20 MHz Current Source in Parallel with Logic InputA

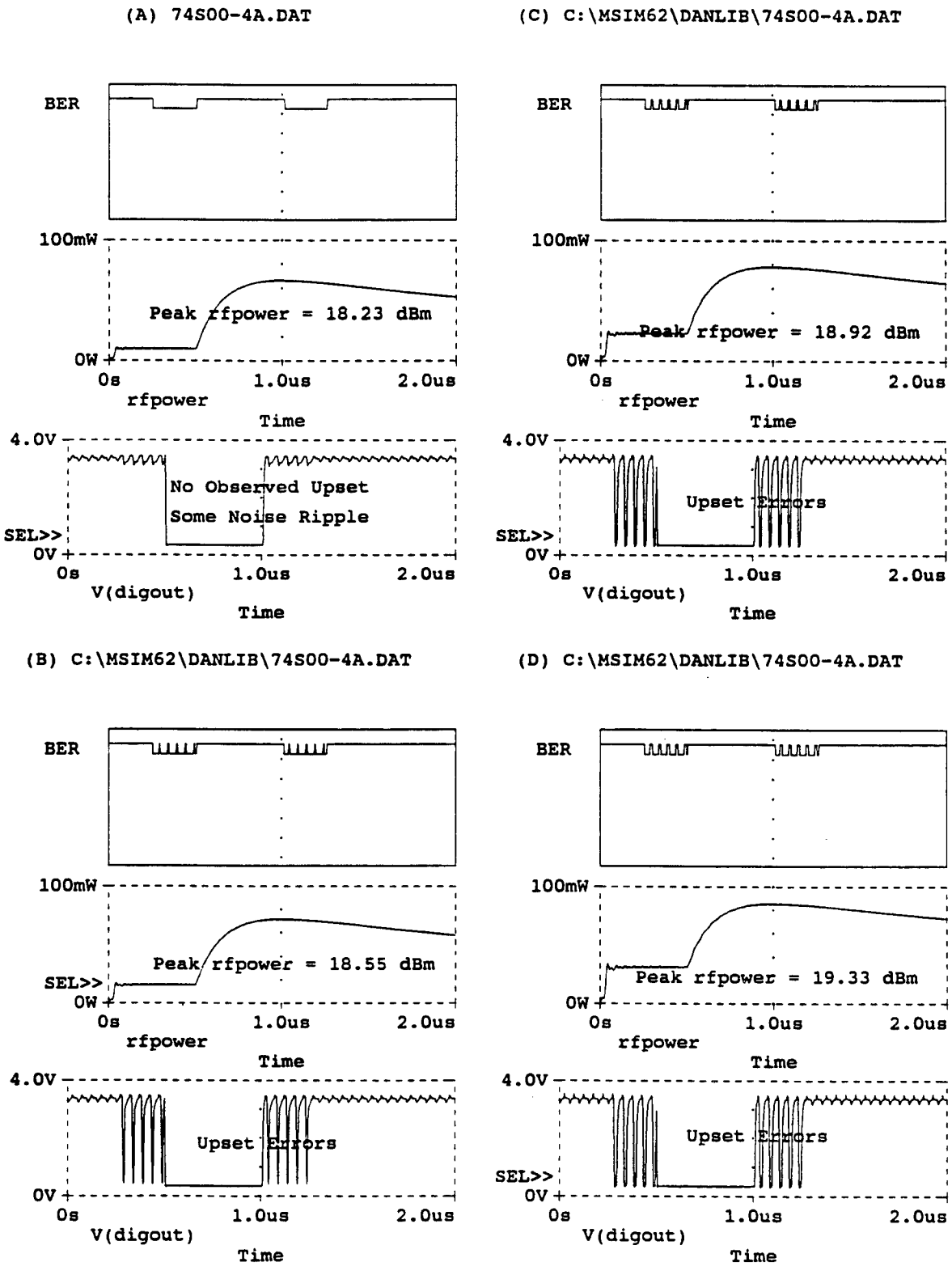
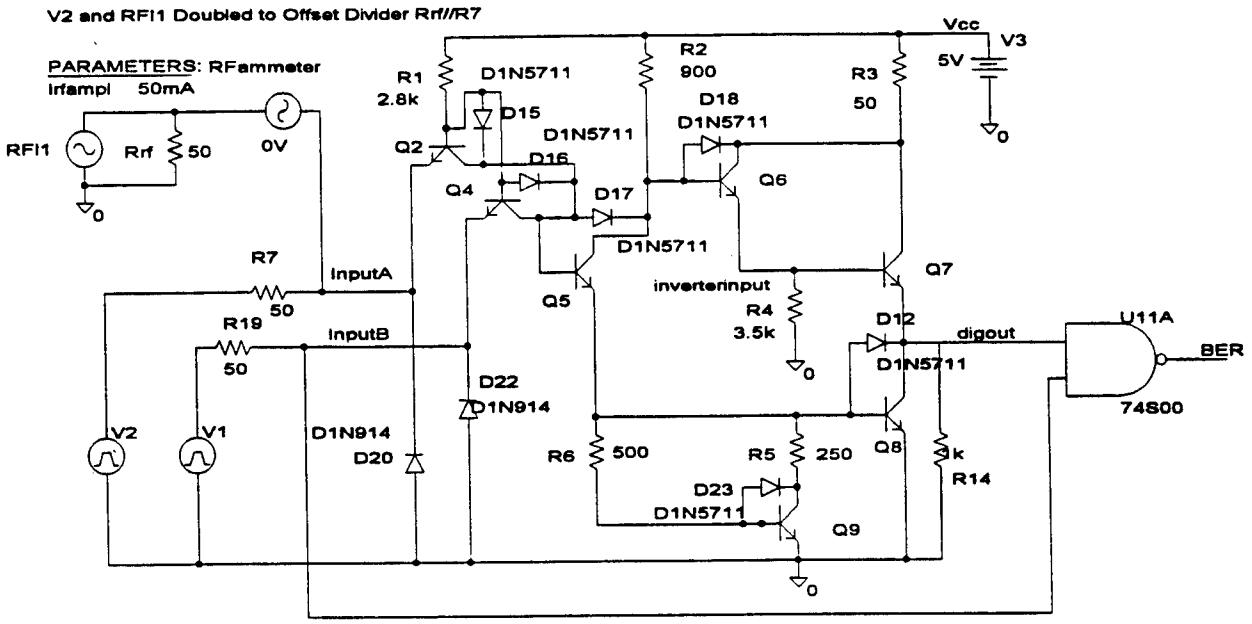


Figure 5-29 Detail Data Susceptibility Build-Up



74S00 NAND GATE: (30 MHz) EM ISource @ Parallel Driven InputA

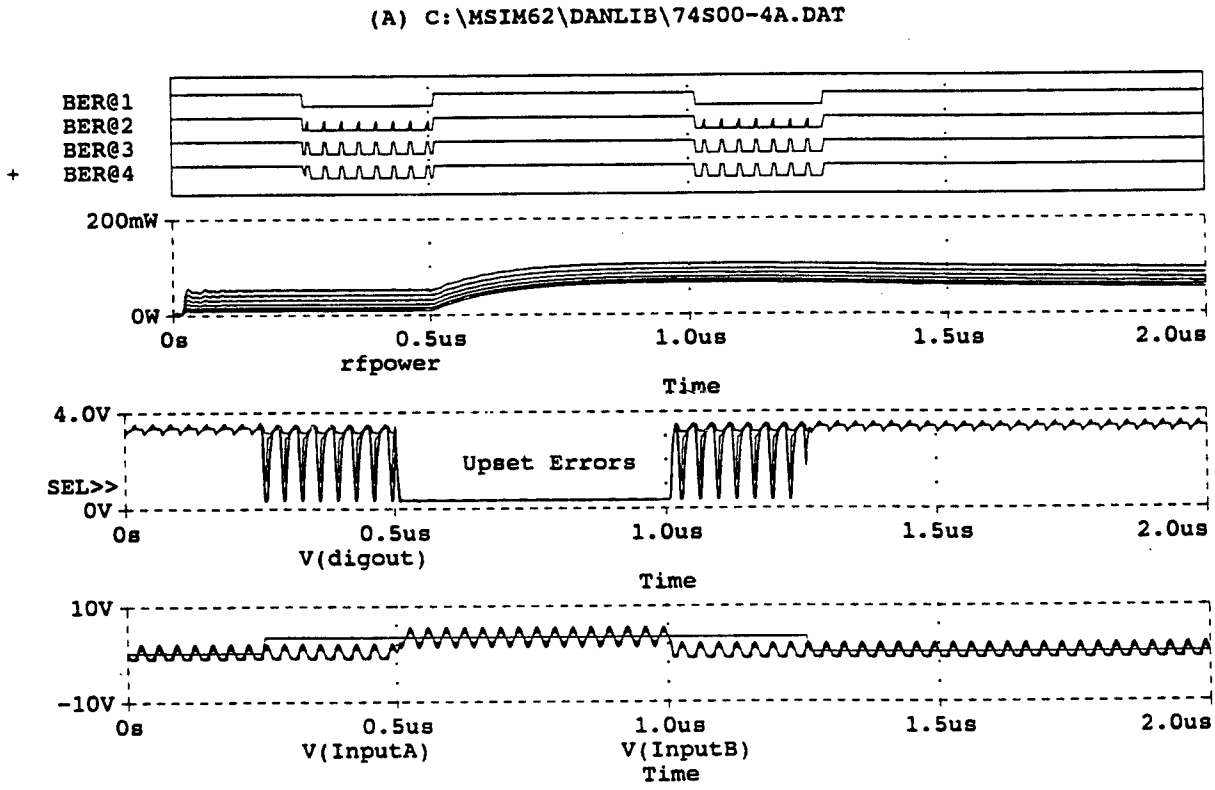


Figure 5-30 Test Gate with 30 MHz Current Source in parallel with Logic InputA

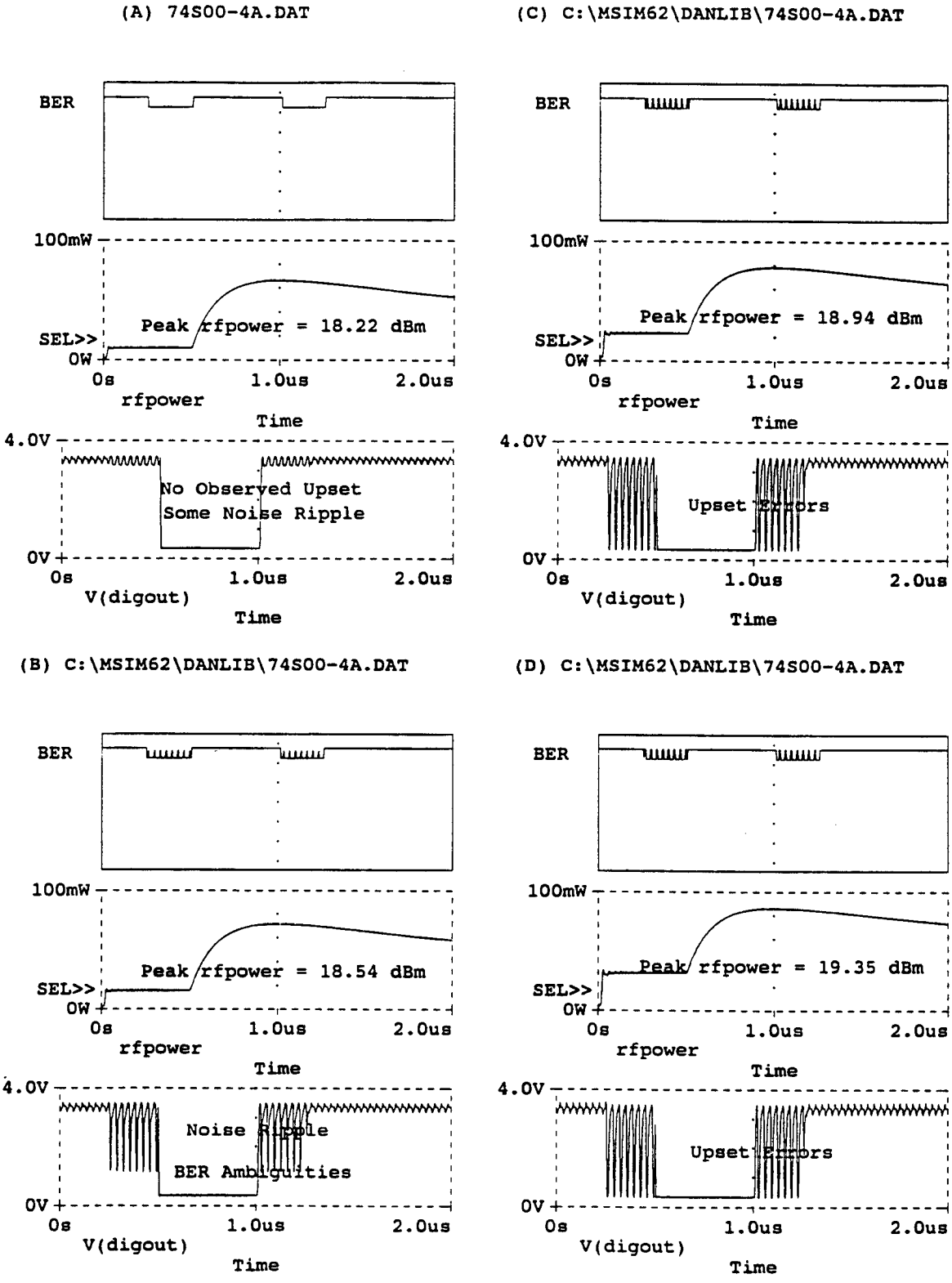
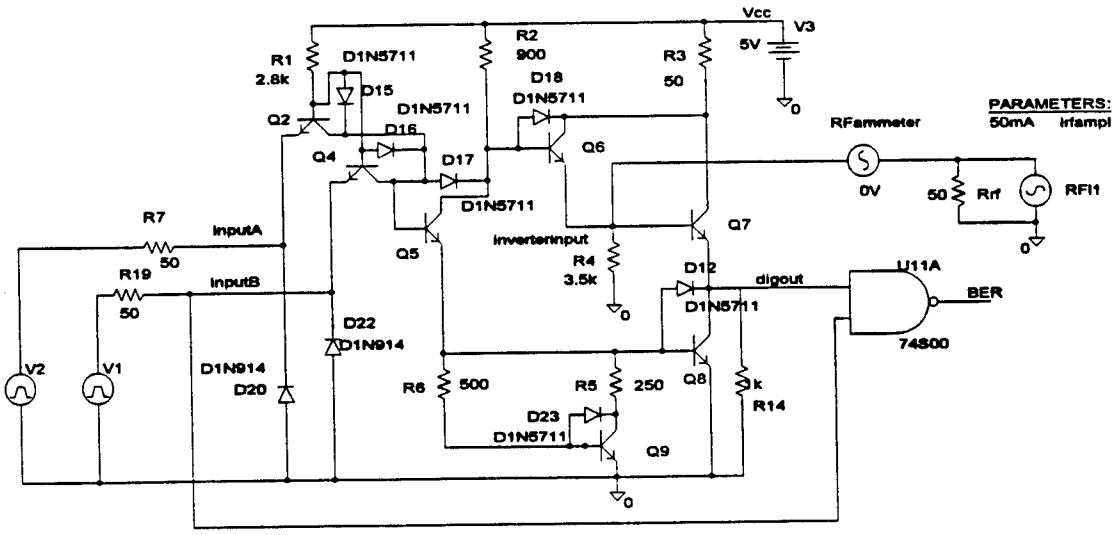


Figure 5-31 Detail Data susceptibility Build-Up



74S00 NAND GATE: (10 MHz) EM ISource @ Inverter Input

(A) C:\MSIM62\DANLIB\74S00-4A.DAT

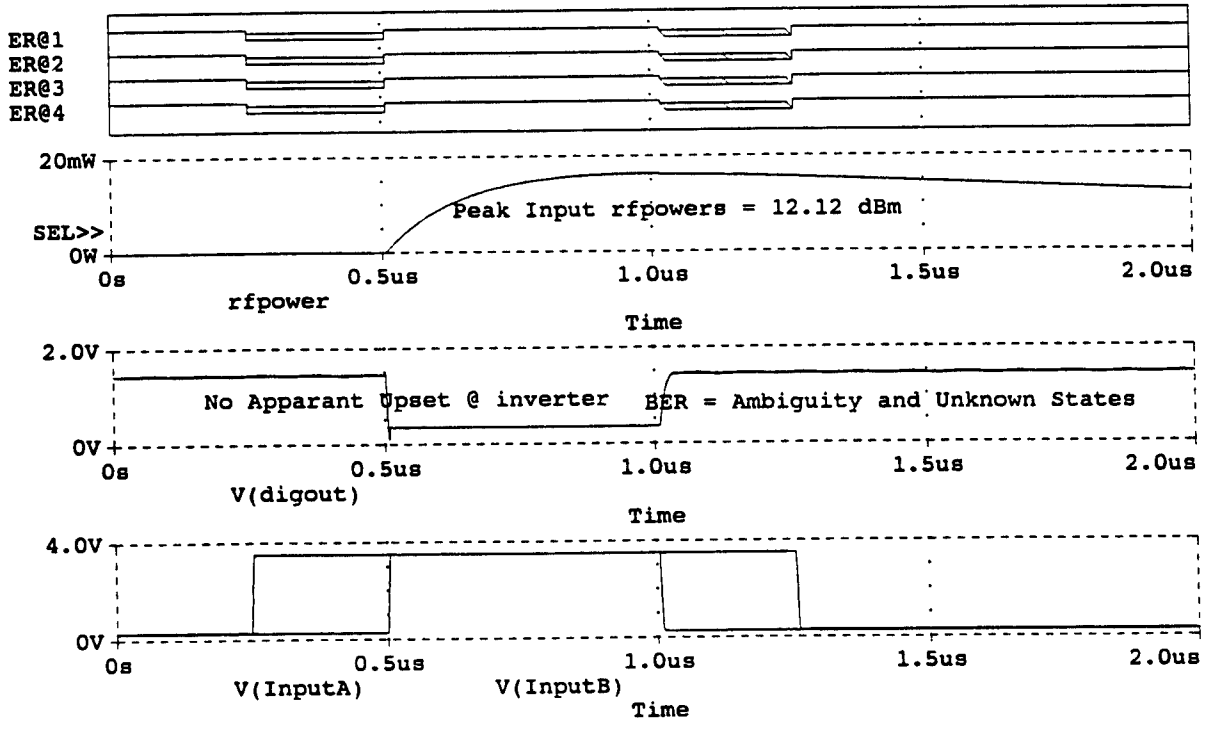
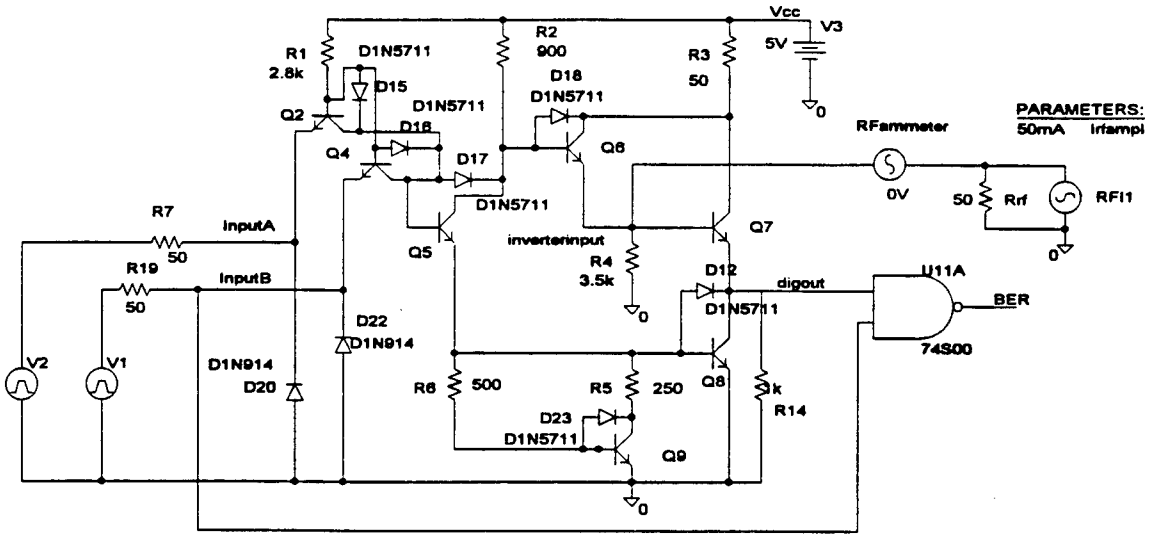


Figure 5-32 Test Gate with 10 MHz Current Source at Inverter Input



74S00 NAND GATE: (20 MHz) EM ISource @ Inverter Input

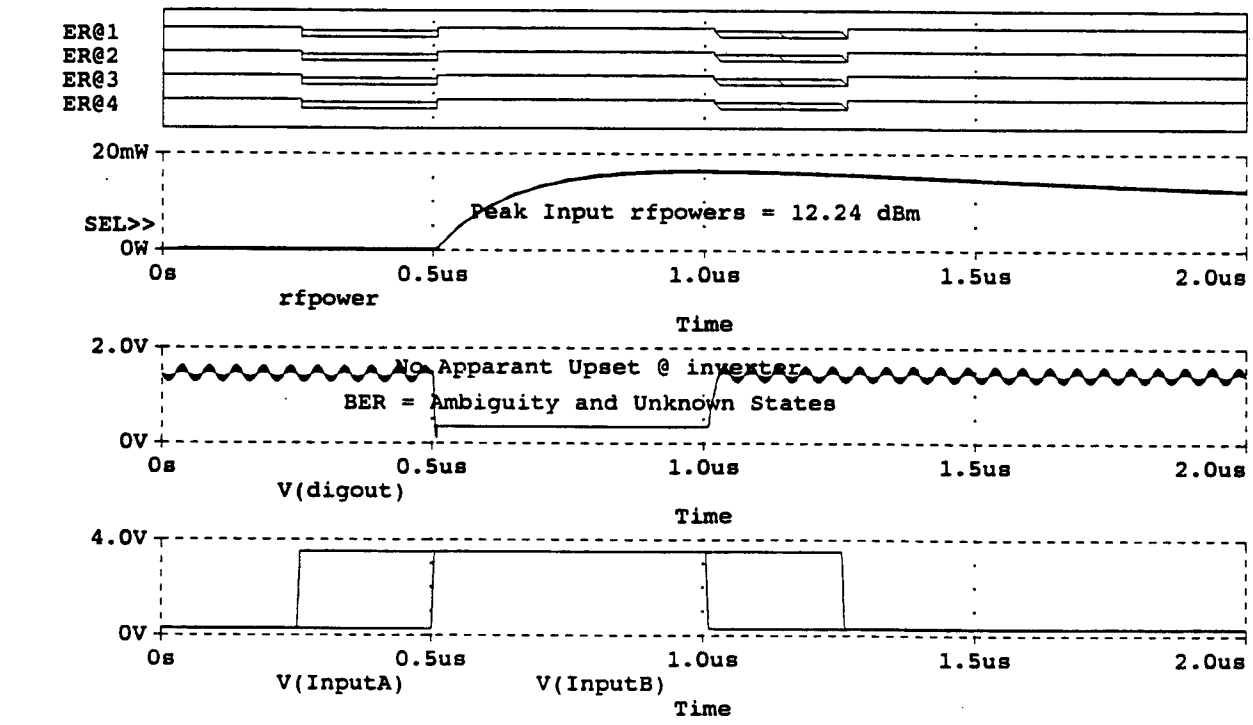
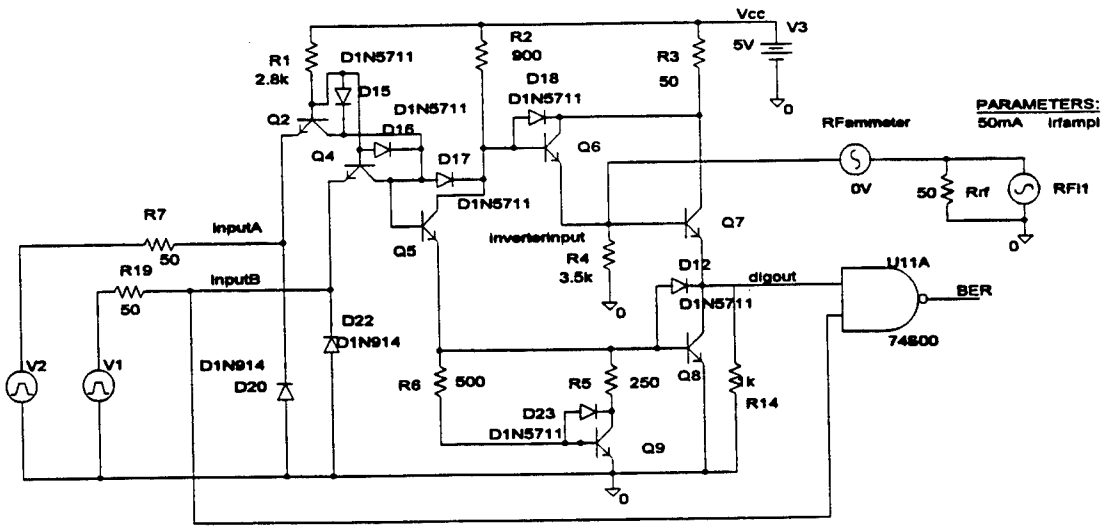


Figure 5-33 Test Gate with 20 MHz Current Source at Inverter Input



74S00 NAND GATE: (30 MHz) EM ISource @ Inverter Input

(A) C:\MSIM62\DANLIB\74S00-4A.DAT

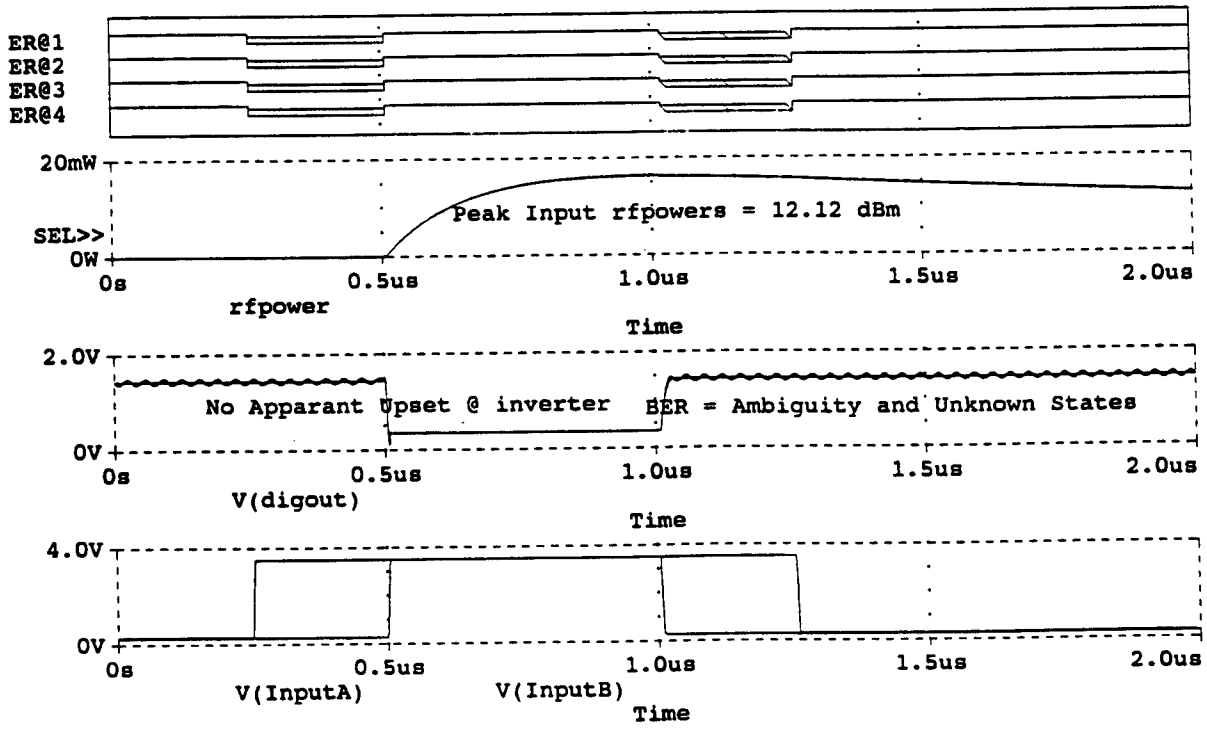
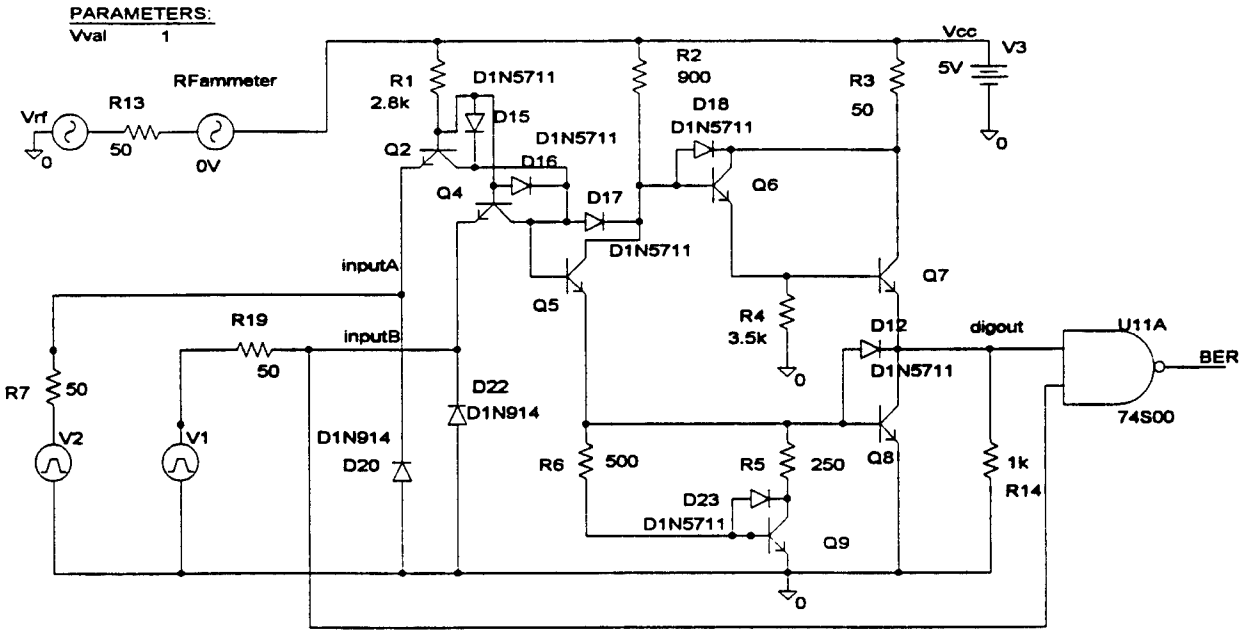


Figure 5-34 Test Gate with 30 MHz Current Source at Inverter Input



74S00 NAND GATE: (10MHz) EM @ Parallel Driven Vcc Rail

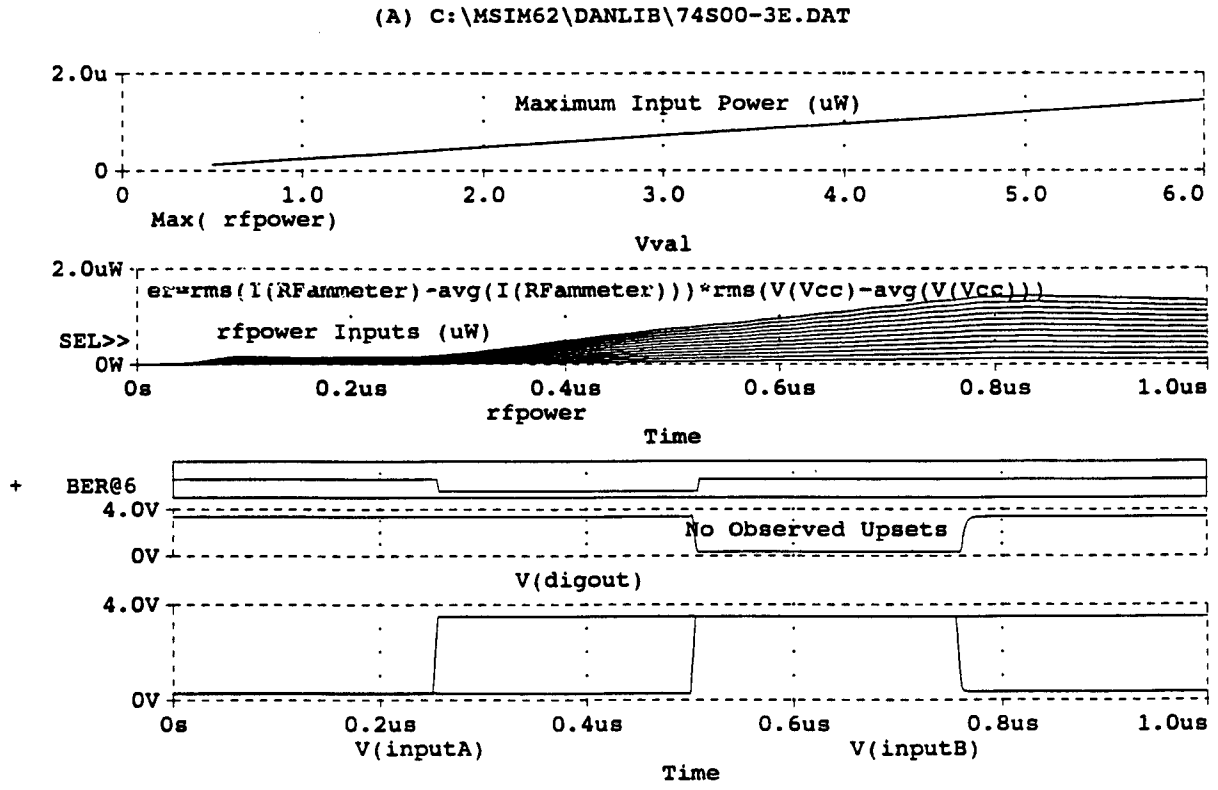
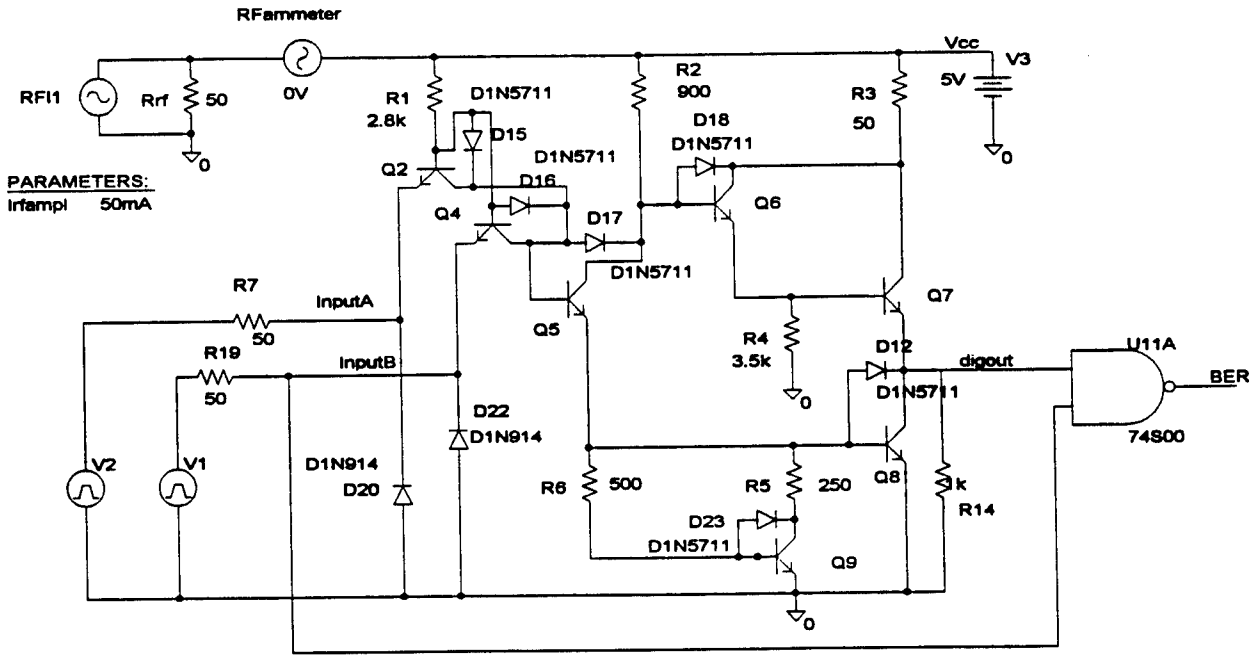


Figure 5-35 Test Gate with 10 MHz Voltage Source in Parallel with Vcc Bias Rail



74S00 NAND GATE: (10 MHz) EM ISource @ Parallel Driven Vcc Rail

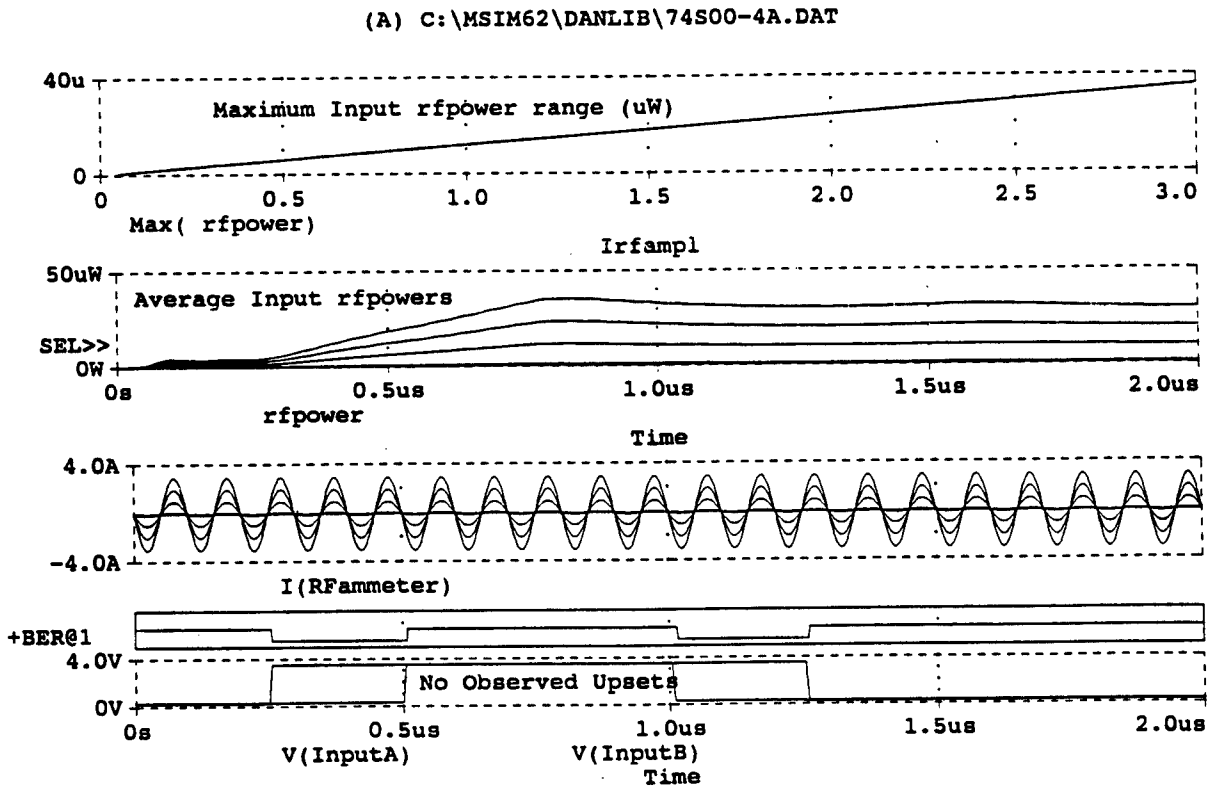


Figure 5-36 Test Gate with 10 MHz Current Source in Parallel with Vcc Bias Rail

6. EYE PATTERNS

The application of eye patterns for detection and assessments of EM driven digital upsets is now described and submitted here as a unique and novel concept developed in this program. Eye patterns of digital waveforms provide a new and innovative way to observe the build-up, event occurrence, and post thresholding responses of EM driven upsets. In this work, we considered better ways to detect and track digital upsets besides simply comparing an EM contaminated digital waveform with its manufacturer's specified baseline. This is not only tedious but does not account for lot or sample device statistics because of variability in device fabrication and production. While statistical criteria for upset were not developed in this work, we did find and implement better ways (macros) in PSPICE to detect and track EM driven upset events. The digital eye pattern is one of them.

Eye patterns are used by designers of digital, pulse coded modulation (PCM) communications systems to assure that timing recovery or symbol synchronization is achieved in a noisy environment of intersymbol interference. This is especially important for "non-return-to-zero" modulation schema that use timing-recovery circuits to phase lock with the transmission clock. Achieving and sustaining good timing-recovery is essential to designing PCM systems with minimum bit-error-rates (BER).

A traditional way to study intersymbol interference in a given digital waveform is to apply the waveform to the vertical plates of an oscilloscope and a sawtooth sweep to the horizontal plates. If the sweep frequency in adjusted to be equal to the transmitted symbol rate or bit rate (or integer multiples), then the digital waveform will be displayed as folding over at each of its bit transitions and will appear as an "eye". The number of foldover times is related to the number of total bits transmitted or the total time sampled. Figure 6-1 shows an "eye" generated from the baseline output of a 74S00 NAND gate over two data periods with a bit period of 500 ns. and a clock rate of 1 MHz. The eye pattern display shows all the data periods in the waveform being analyzed as superimposed

onto one sweep. The effect on the display is to generate a opening that resembles an "eye" where its horizontal dimension is the time axis and its vertical dimension is the bit state level. In practice, the eye is typically oval shaped with a horizontal major axis related to the timing margins and a vertical minor axis related to the noise margins.

The amount of "opening" in the eye is directly related to the transmission BER. A large opening implies minimal BER. The slope at either end of the foldover is a measure of timing (and level) sensitivity and is determined by how fast the eye closes with the advent of timing and level jitter. Steeper slopes mean less susceptibility to noise jitter. Eye width is a measure of maximum allowed sampling time of the received waveform for minimal distortion. Maximum width also means less susceptibility to clock phase errors. Eye height is a measure of voltage noise margins. Maximum height obviously means less susceptibility to additive noise and interference. In a noisy environment with intersymbol interference, timing and level distortions in the received digital waveforms cause the eye (actually, the "lids" as we shall soon demonstrate) to begin to droop and to eventually close. In this situation, a communication system in such a noisy environment is said to be susceptible to intersymbol interference because it cannot avoid the bit errors implied by its closed detection eye.

The application of eye patterns to assessments and mitigation of EM driven upsets seems a natural extension. The idea behind its use is simple. Eye patterns capture and display temporal and state distortion in output digital waveforms resulting from EM coupling into device ports, and the subsequent increase of BER in the victim device. Previously, we used identical logic gates of comparable technology (to those being simulated and tested) to detect and track upset thresholds. That was a considered improvement over "eye-balling" the digital waveforms and comparing them to manufacturer's data. These comparable logic blocks functioned as comparators and made EM driven upset decisions more consistently and realistically. Now with eye patterns, we add another magnitude of improvement. The upset threshold data in the following runs easily demonstrate

marked improvements in both upset detection sensitivity and accuracy.

The eye sweep shown in figure 6-1 use a special algorithm [1] to generate the required sweep instead of using an analog oscilloscope. As a matter of interest, an analog oscilloscope was implemented in PSPICE with ABM's in this program for comparison purposes; it performed as expected but was too cumbersome for serious analysis. Instead, the algorithm sweep was implemented as a macromodel in all the following data runs. The algorithms for an eye sweep are as follows:

pi = 4*atan(1),

mod(a,b) = (b)*(atan(tan(((a)/(b))*pi - pi/2)) + pi/2)/pi,

eye_sweep (p,d) = mod(time + (p)/2 + (d), p) - ((p)/2 + (d)), where

a = time + (p)/2 + (d), and

b = p

The first macro simply computes the value of π. The modulo macro is a floating point modulo function in arguments a and b that relate to the digital data period "p" and the eye sweep display delay time "d". The eye_sweep macro generates a foldover sweep centered at 1/2 the data period "p" plus the display sweep delay time "d". Note, that negative p's and d's are allowed.

To use the algorithm, write it as a macro and save all its lines to a named macro file while in the PROBE analysis mode. Then, while still in PROBE, call up the trace waveform of interest and simply change from a time axis variable to the eye_sweep (p,d) function desired. Eye_sweep will then generate the required foldover and display the entire digital time line in one sweep. In practice, some tweaking may be needed, especially with the delay time which is usually a very sensitive display parameter. Also, in the following data runs, we found the rf phase of the EM sources to be very eye pattern sensitive. In all the following plots, a macro for computing average rf power which was developed previously was run off-line and is as follows:

rfpower = rms(V(InputA)-avg(V(InputA)))*rms(I(RFammeter)-avg(I(RFammeter))).

The test device selected was the TI 74S00 NAND Gate. Data runs were computed for an EM voltage source at 10 MHz connected in series with the logic pin InputA of the gates under test.

Figure 6-1 shows the idealized eye_sweep display discussed earlier. Figure 6-2 shows the baseline gate to be tested. It is configured with additional inverter and DSTM (digital stimulus) driven, comparable gates. These two gates make up an improved BER detector over the ones used previously in section 5. Both BER detectors exhibited identical baselines but the latter is now driven with an independent logic source, DSTM, instead of a sample of inputB as was done previously on page 5-6. While no anomalies were found, it seemed best to decouple the two logic inputs. Figure 6-3 shows the logic response waveforms and a pristine eye pattern for the baseline gate. The eye shown is for a 1 MHz bit rate and for bits with 500 ns periods. Figure 6-4 shows the test gate EM driven with a 10 MHz voltage source in series with its logic InputA. Figure 6-5 shows the gate driven with 1.85 dBm of rf power. Figure 6-6 show the gate driven with 1.93 dBm of rf power.

Figure 6-7 shows the response to 2.02 dBm of rf power. Note, there is a hint of ripple outside the V(digout) analog pulse width while the BER is still flat and correct. Figure 6-8 shows the upset hint becoming discernible ripple at rf power of 2.12 dBm, a change of only 1/10 of a dB or 2.33 %. This kind of sensitivity will be prevalent throughout. Figure 6-9 shows the gate response to 2.23 dBm of rf power; again, a 2.6 % change. Note, there is observable eye drooping very evident in the pattern suggesting an onset of BER errors even though the BER detector output is still (!) flat and correct. This suggests a sensitivity greater than that provided by the comparable logic gates used previously. Figure 6-10 shows the eye lid almost half closed for an rf power level of 2.36 dBm and the first indication of BER errors. This rf power is the threshold level of upset as determined with the new BER detector and eye pattern display. It is interesting to compare this threshold level of 2.36 dBm (as detected by the modified BER detector and displayed by the eye pattern) with the threshold

level of 1.42 dBm using the old detector and no eye pattern display, as shown in figure 5-10 on page 5-15. This difference in threshold resolution of about 1 dB or 20 % probably warrants further study. Figure 6-11 shows the eye lid now almost closed for rf power level of 2.53 dBm and BER errors. Figures 6-12 through 6-20 shows further progressive closure of the eye lid for rf power levels ranging from 2.72 dBm through 7.48 dBm, respectively.

Figure 6-21 shows the test gate EM driven with a 10 MHz voltage source in parallel with its logic InputA. Figures 6-22 and 6-23 show the undisturbed gate driven by 17.25 dBm and 17.49 dBm, respectively. Figure 6-24 shows the gate driven by 17.54 dBm and the eye showing a hint of droop while the ripple in V(digout) is apparent; at the same time, the BER output is still correct. Figures 6-25 and 6-26 show the eye lid closing for rf power levels of 17.6 dBm and 17.67 dBm, respectively. Figure 6-27 shows the eye lid status for rf power level of 17.74 dBm. The rf phase sensitivity is next shown in figure 6-28 which shows the eye lid status for the "same" rf power level. Note the marked difference in the eye pattern for a 180° rf phase shift (λ = 50 ns), suggesting considerable timing sensitivity. Figure 6-29 shows the eye lid droop for rf power level of 17.8 dBm and still no BER output. Figure 6-30 shows the eye lid status for an rf power level of 17.88 dBm and shows the onset or threshold of upset. This compares very favorably with data on comparable devices as shown in figure 5-16 on page 5-21 where the upset threshold is shown to be 18.0 dBm, within 2.7 % difference.

Figures 6-31 through 6-35 show the BER error states and progressive droopy closure of the eye patterns for rf power levels ranging from 17.96 dBm thru 18.75 dBm, respectively. Figure 6-36 at rf power level of 19.87 dBm shows the onset of an interesting new feature of the rf EM driven eye patterns - the onset of the lid reopening from the middle bottom of the eye pattern. Figures 6-37 and 6-38 show the continuing evolution of this lid reopening for increasing rf power levels from 20.8 dBm to 21.71 dBm, respectively. The last three plots indicate the lid regrowth as new symmetrical, left

and right hand openings. While it appears to be a double foldover, this new effect is not understood, at present. It may be somehow related to some unknown nonlinear device effects that are apparent in the rf clipping (and hard rectification) at the InputA pin of the test gate.

[1] Unknown Corporate Author, MicroSim Applications Newsletter, January 1993, MicroSim Corporation, 20 Fairbanks, Irvine, CA. 92718.

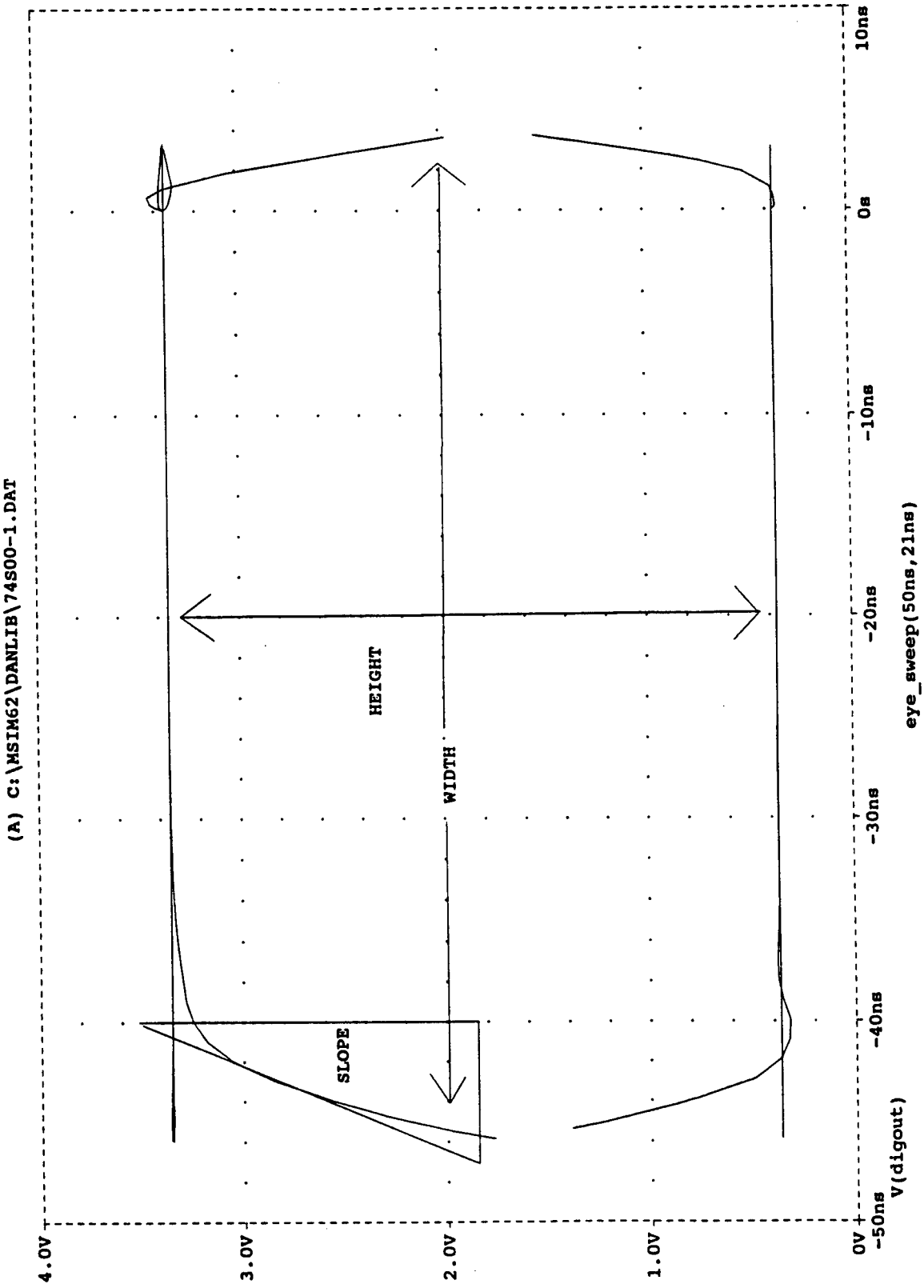


Figure 6-1 Digital Eye Pattern

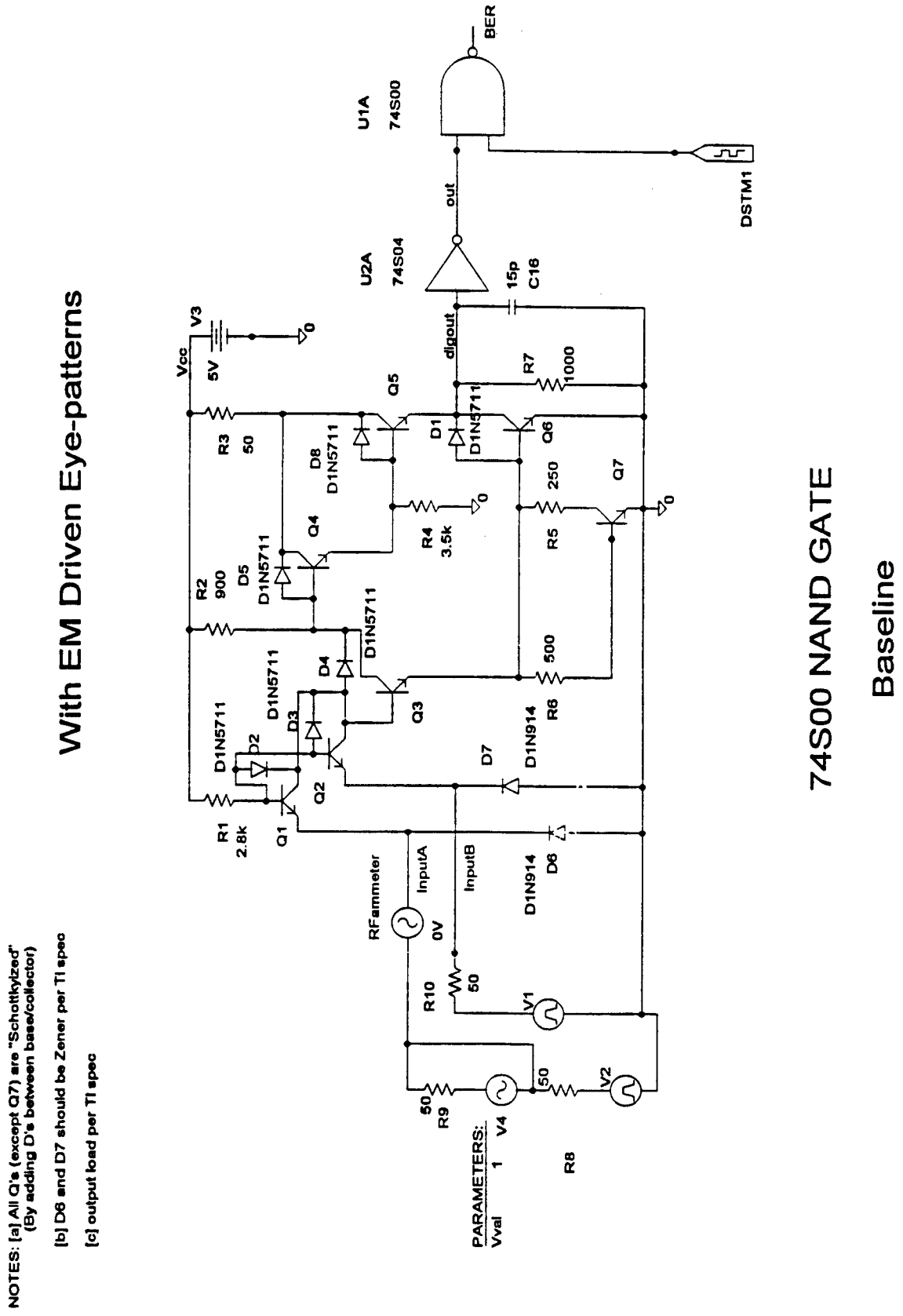


Figure 6-2 Baseline 74S00 NAND Gate for Eye Sweeps

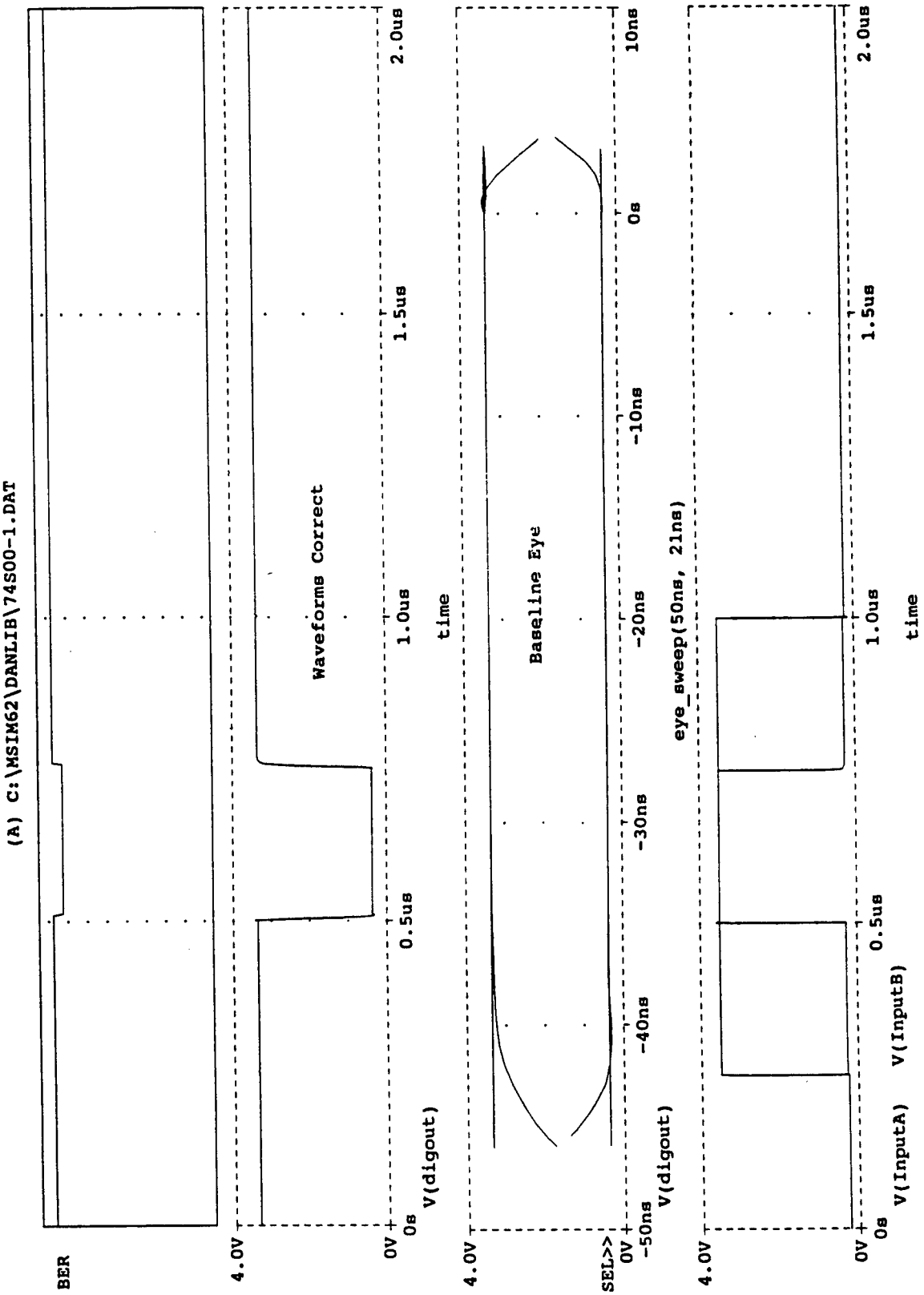


Figure 6-3 Baseline Digital Responses and Eye Sweeps

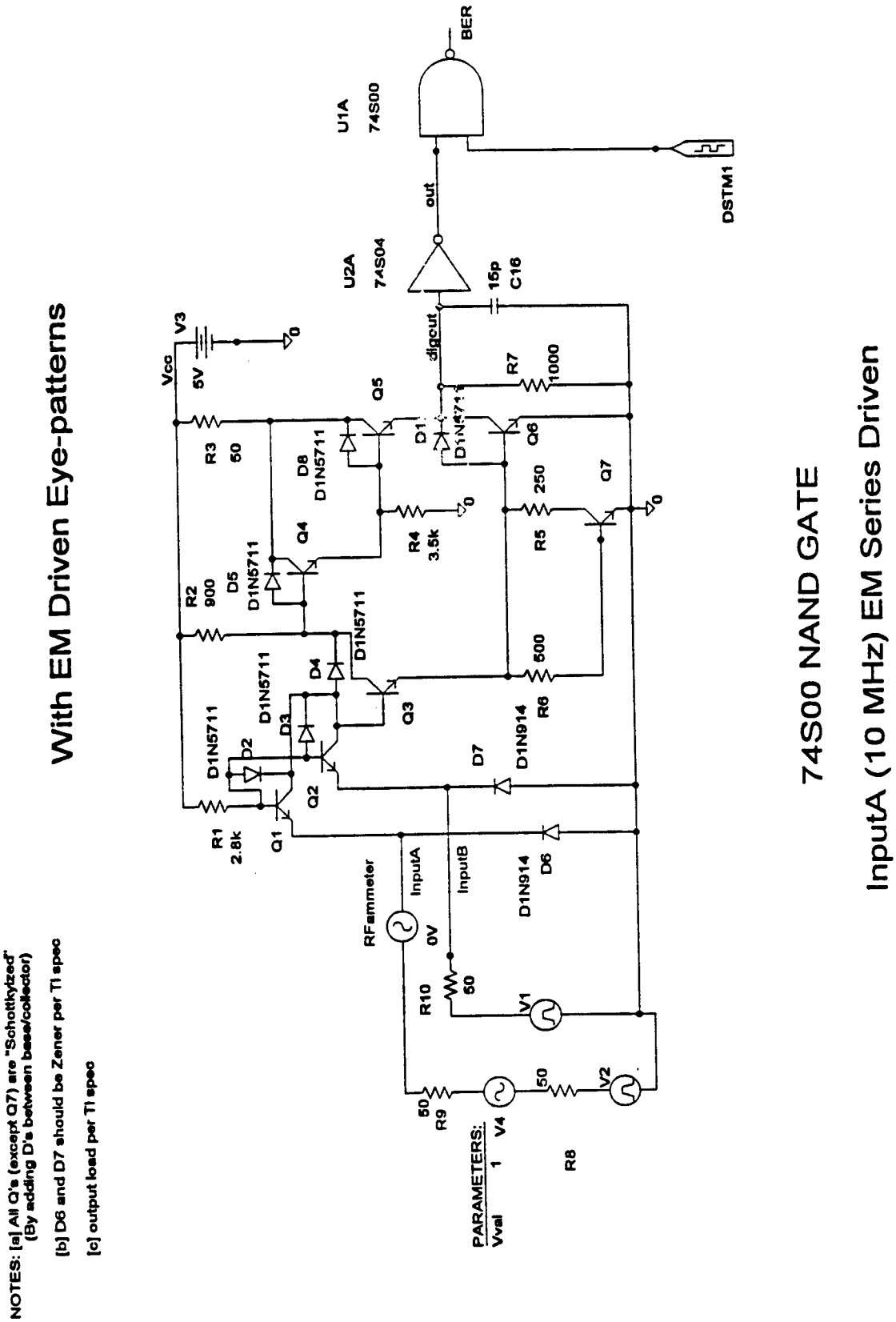


Figure 6-4 Test Gate EM Driven by 10 MHz Voltage Source in Series with Logic InputA

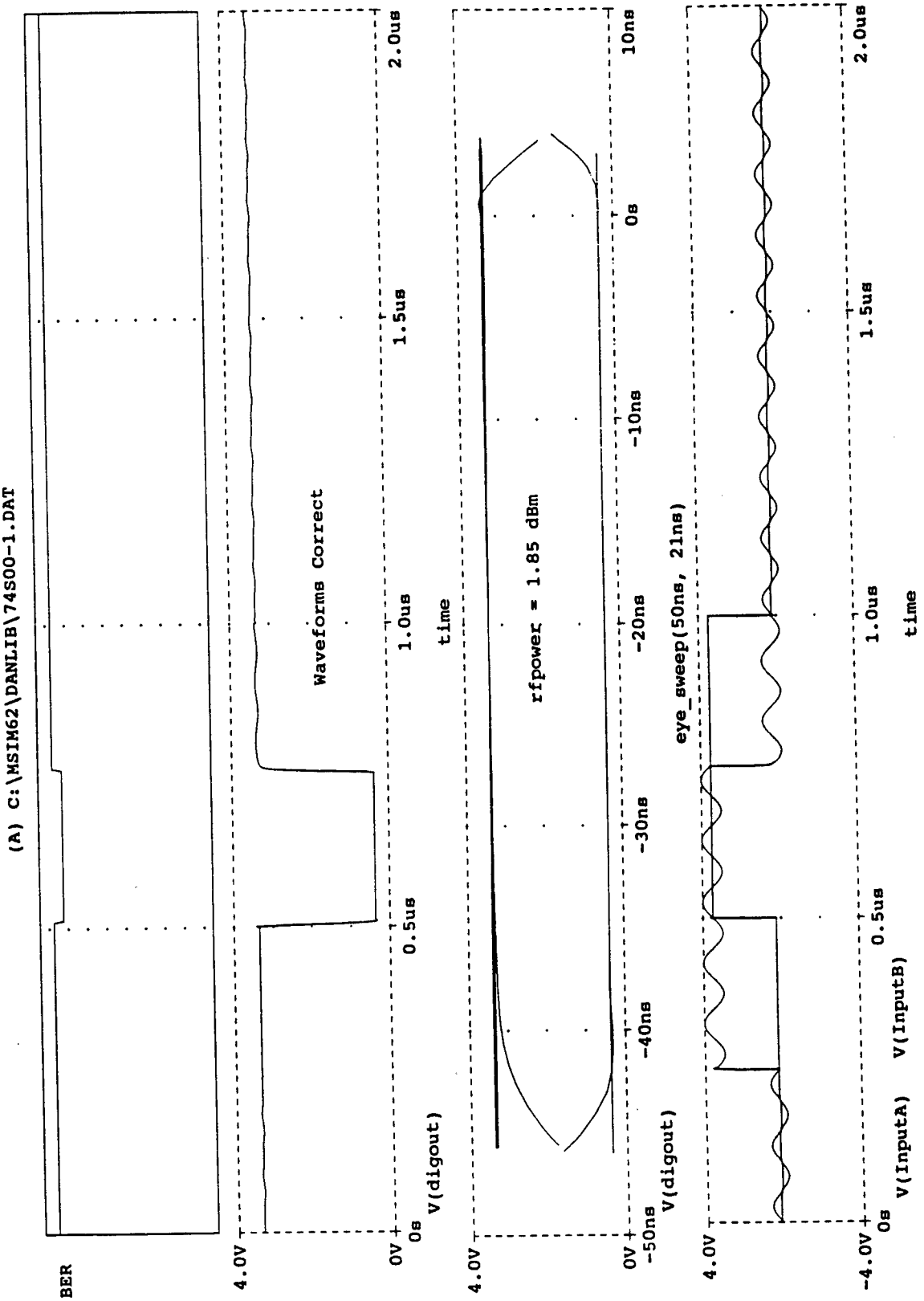


Figure 6-5 Gate Responses and Eye Pattern for 1.85 dBm Power

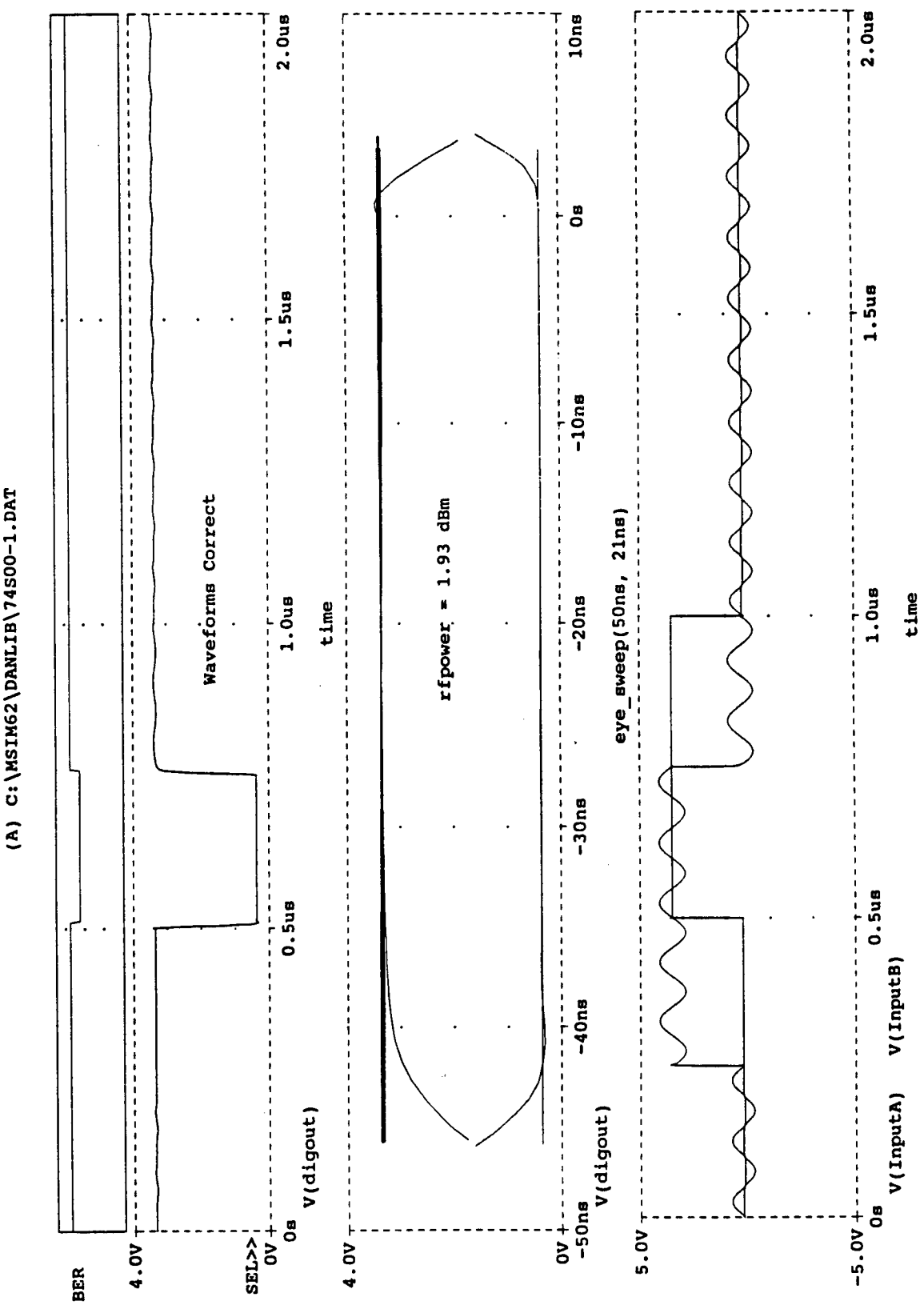


Figure 6-6 Gate Responses and Eye Pattern for 1.93 dBm Power

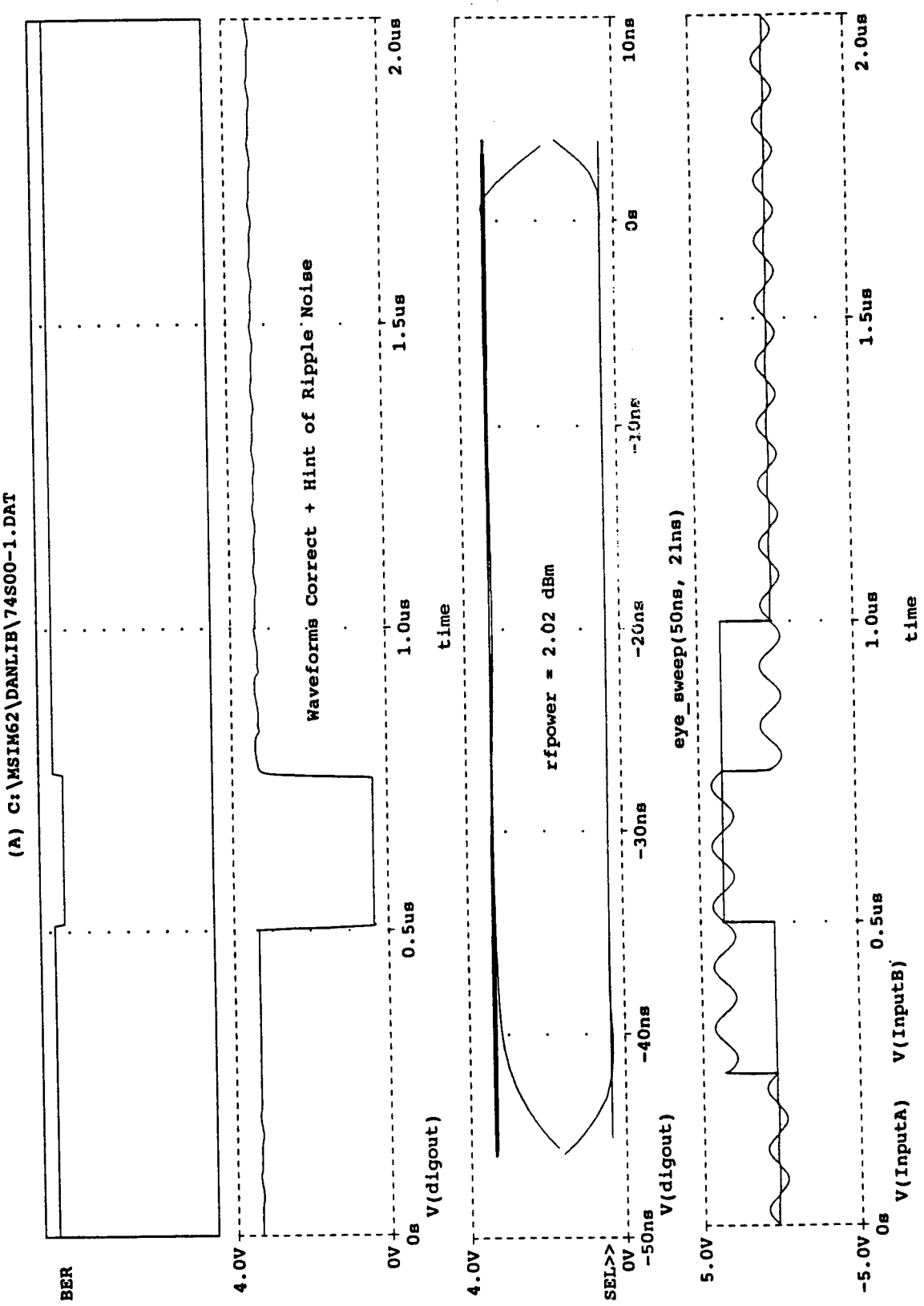


Figure 6-7 Gate Responses and Eye Pattern for 2.02 dBm Power

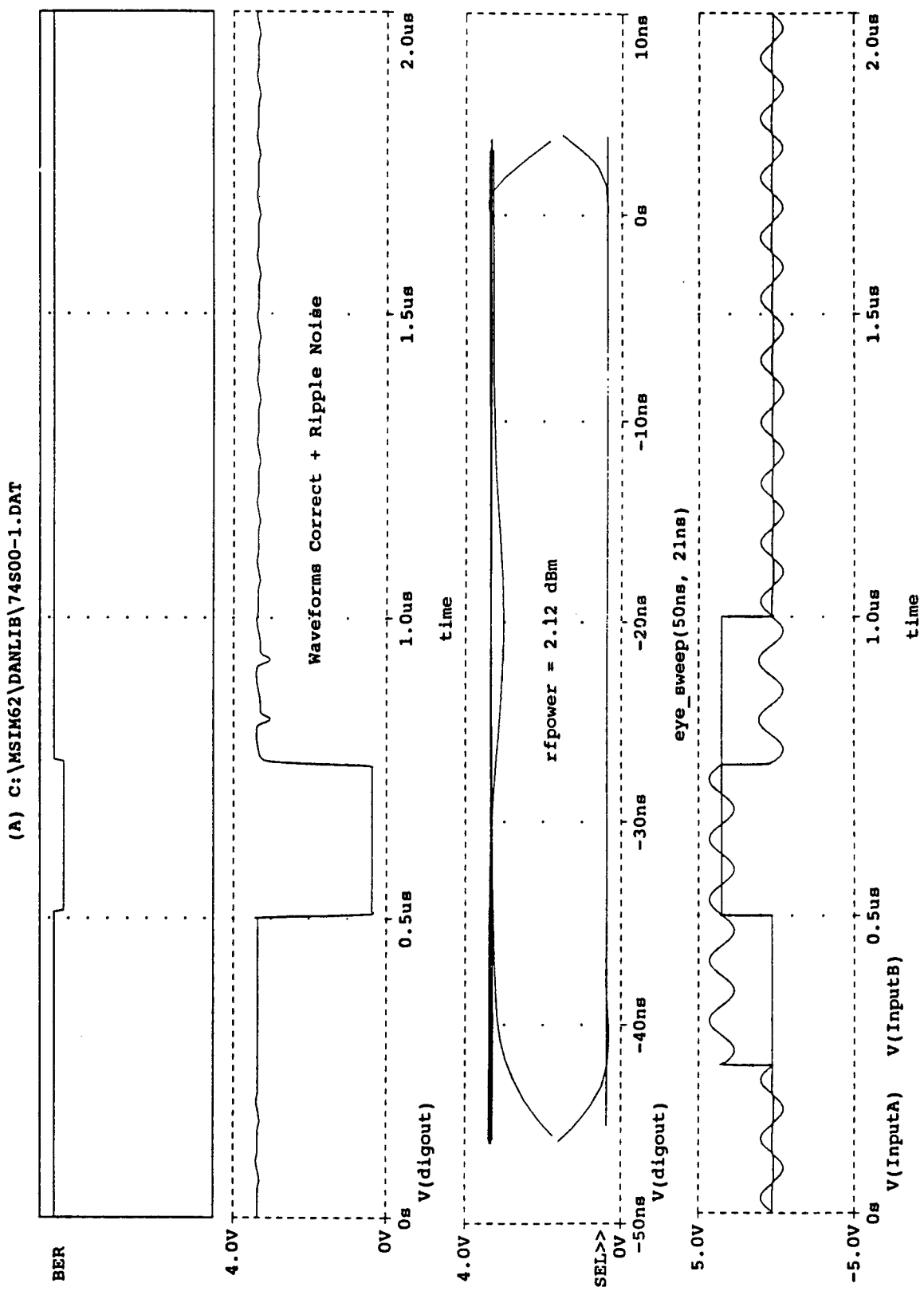


Figure 6-8 Gate Responses and Eye Pattern for 2.12 dBm Power

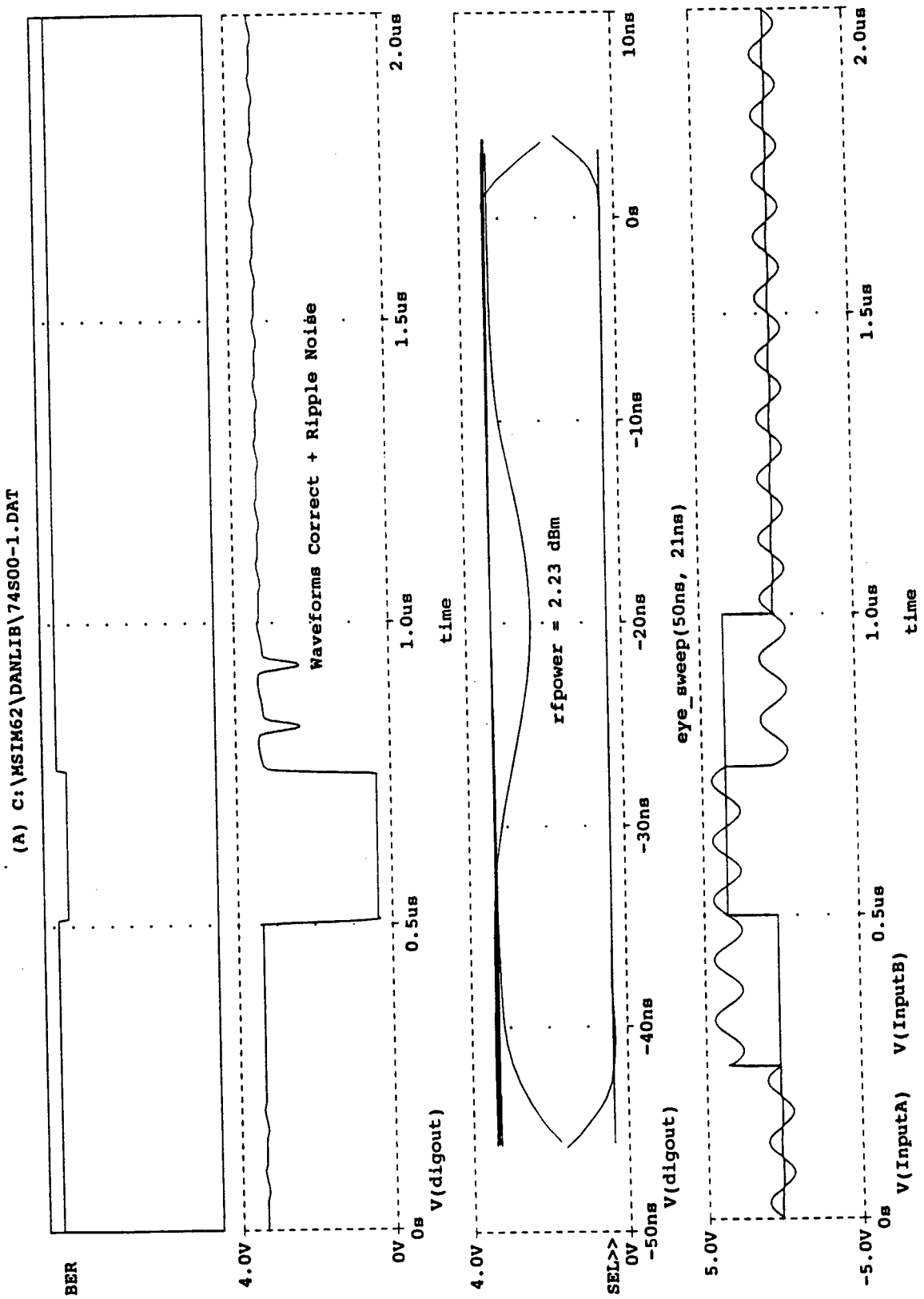


Figure 6-9 Gate Responses and Eye Pattern for 2.23 dBm Power

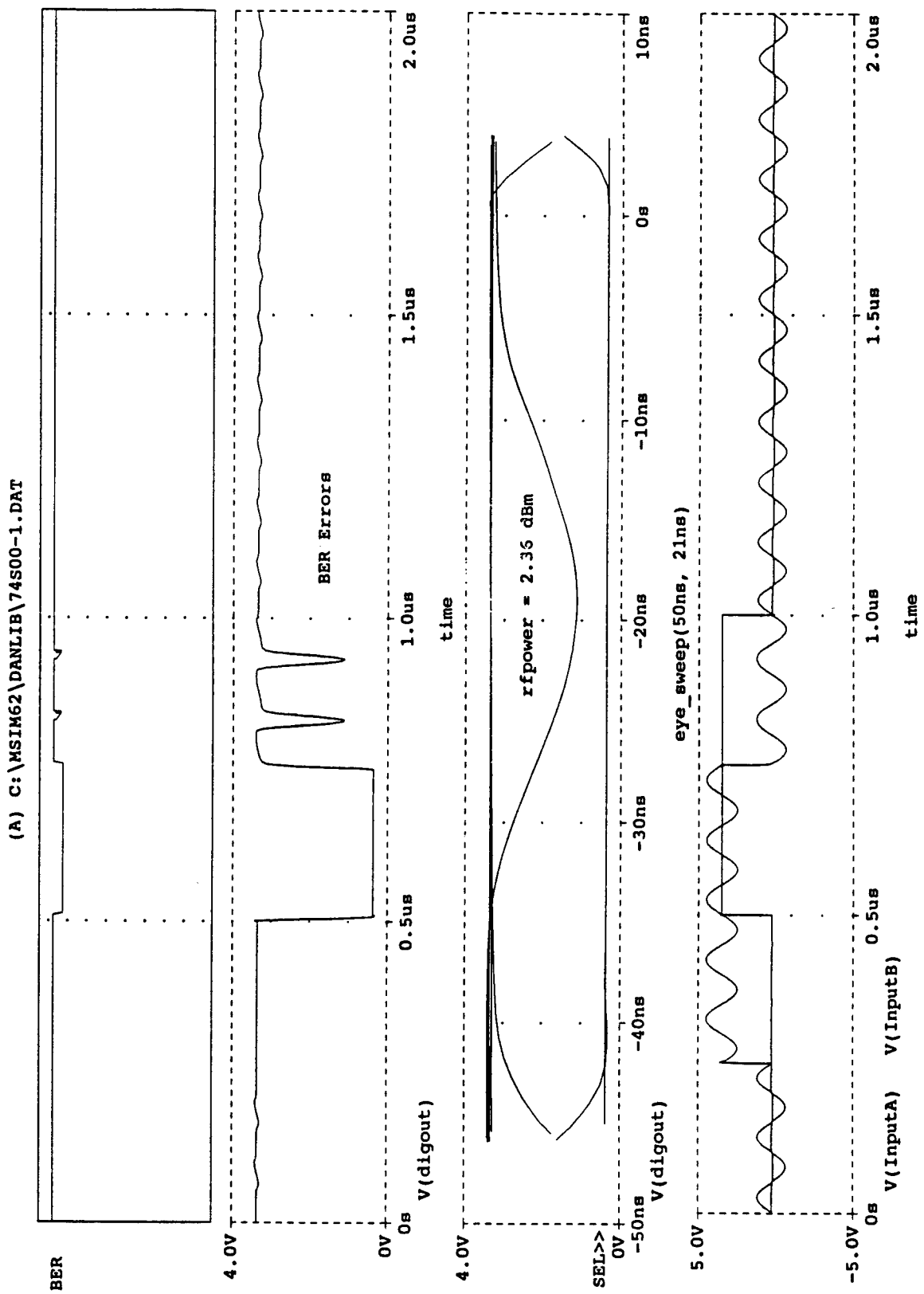


Figure 6-10 Gate Responses and Eye Pattern for 2.36 dBm Power

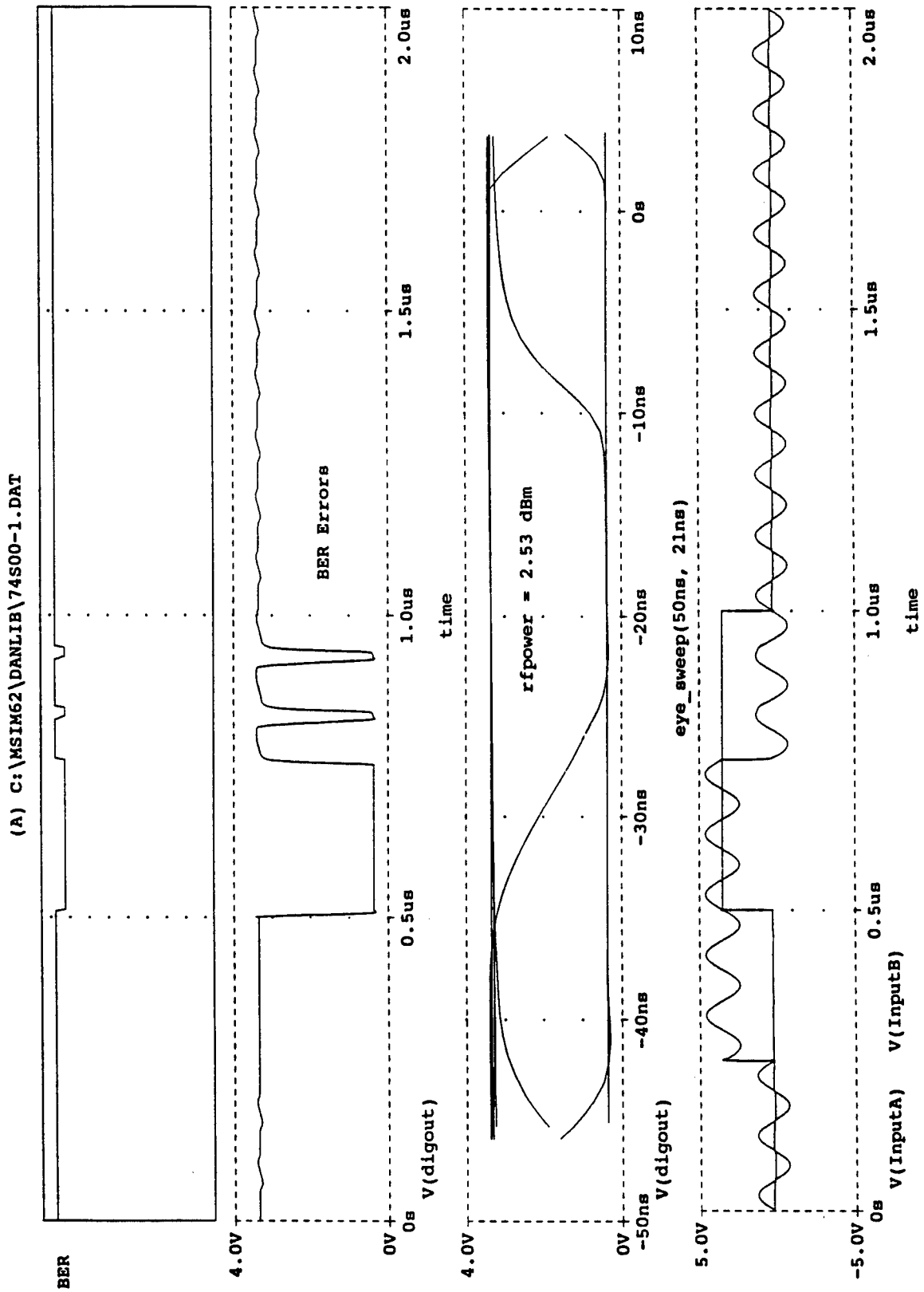


Figure 6-11 Gate Responses and Eye Pattern for 2.53 dBm Power

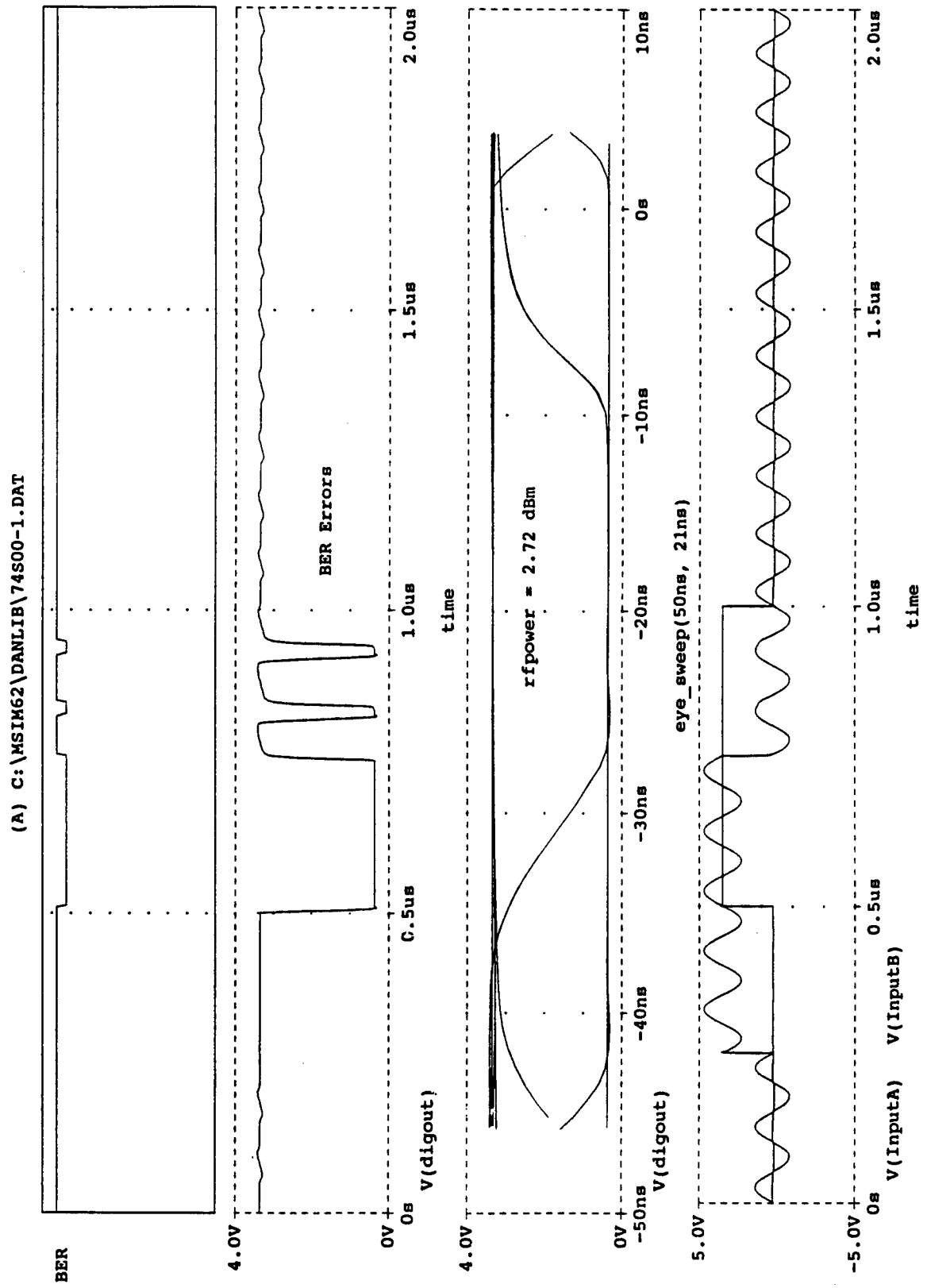


Figure 6-12 Gate Responses and Eye Pattern for 2.72 dBm Power

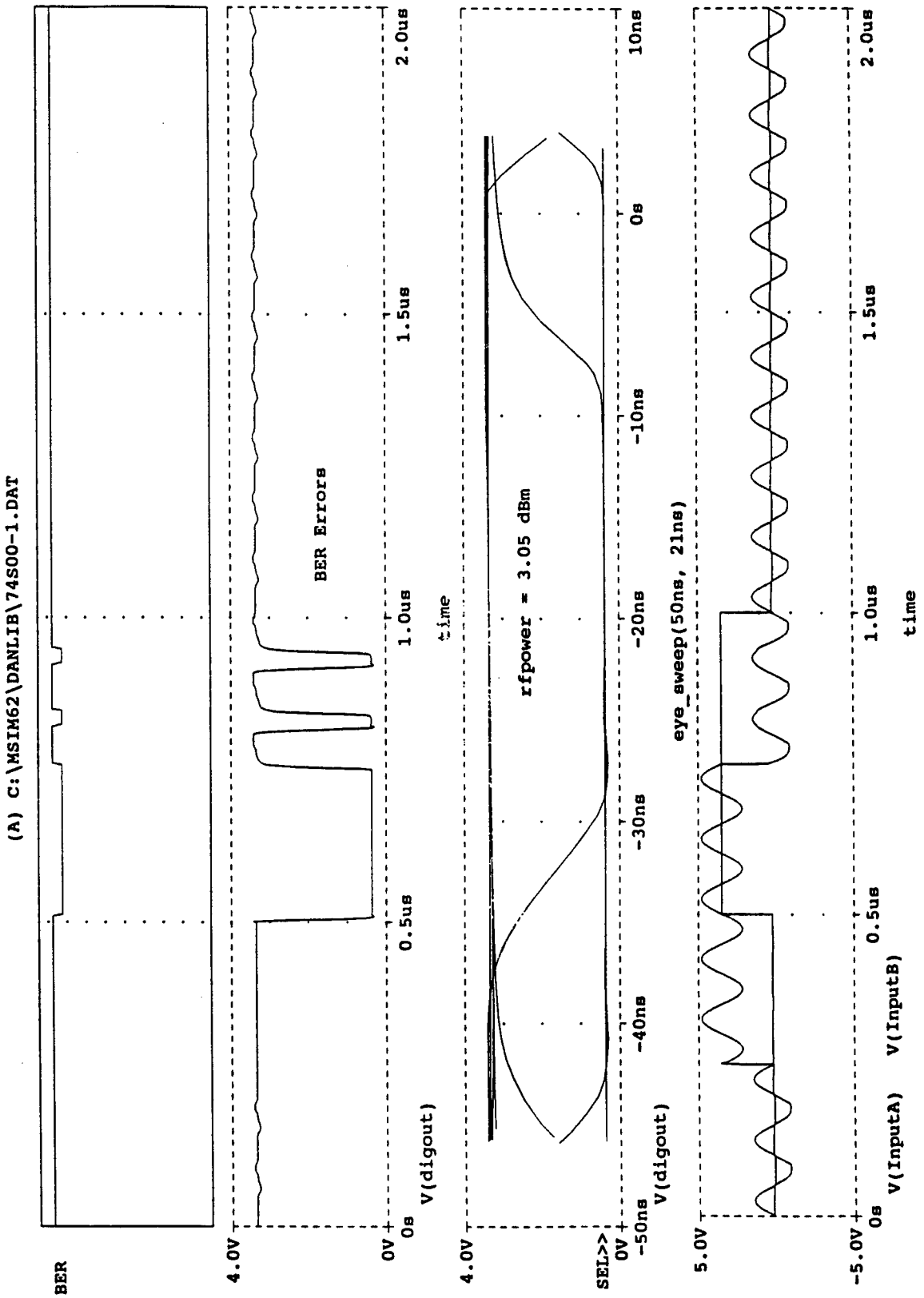


Figure 6-13 Gate Responses and Eye Pattern for 3.05 dBm Power

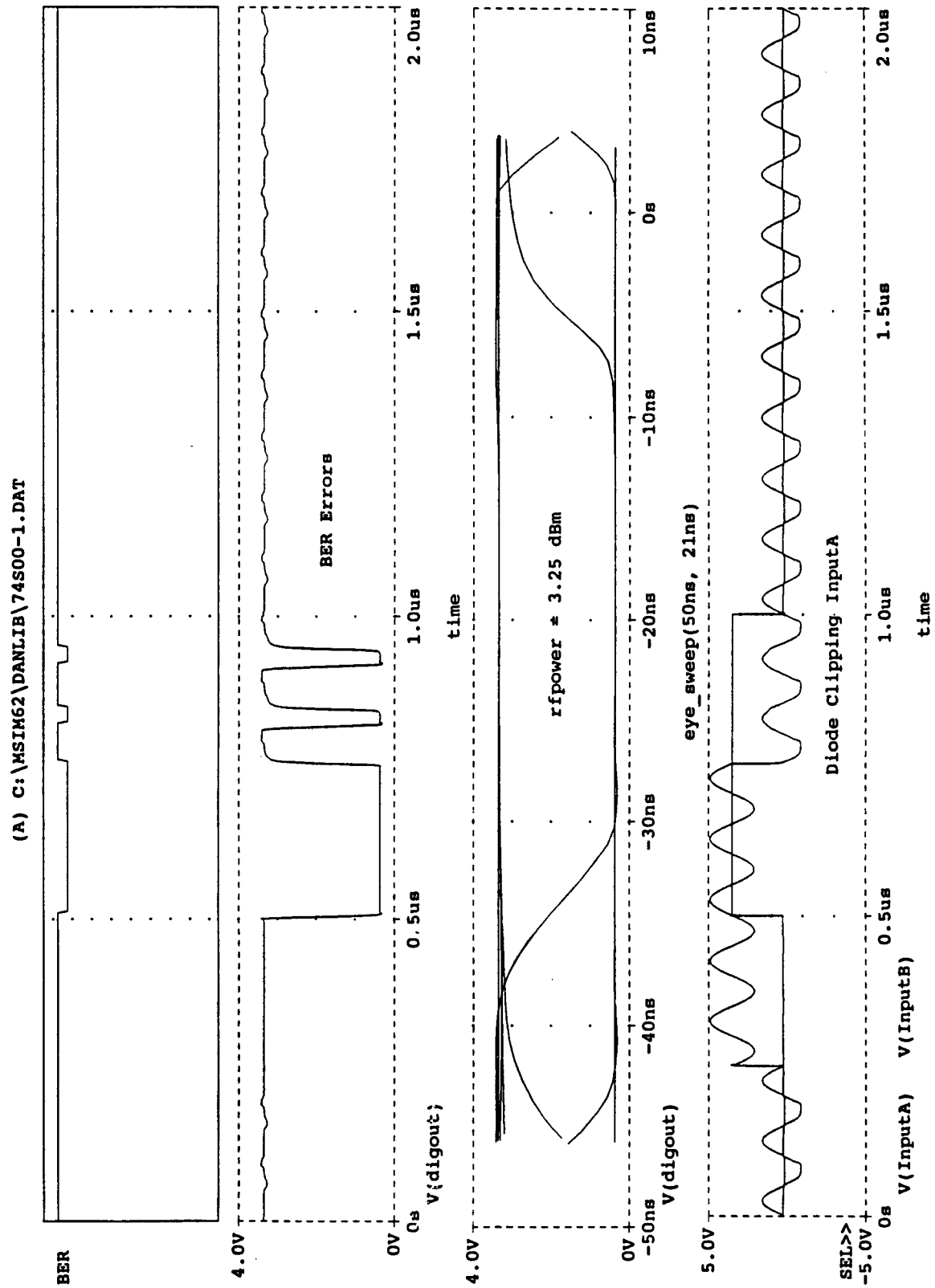


Figure 6-14 Gate Responses and Eye Pattern for 3.25 dBm Power

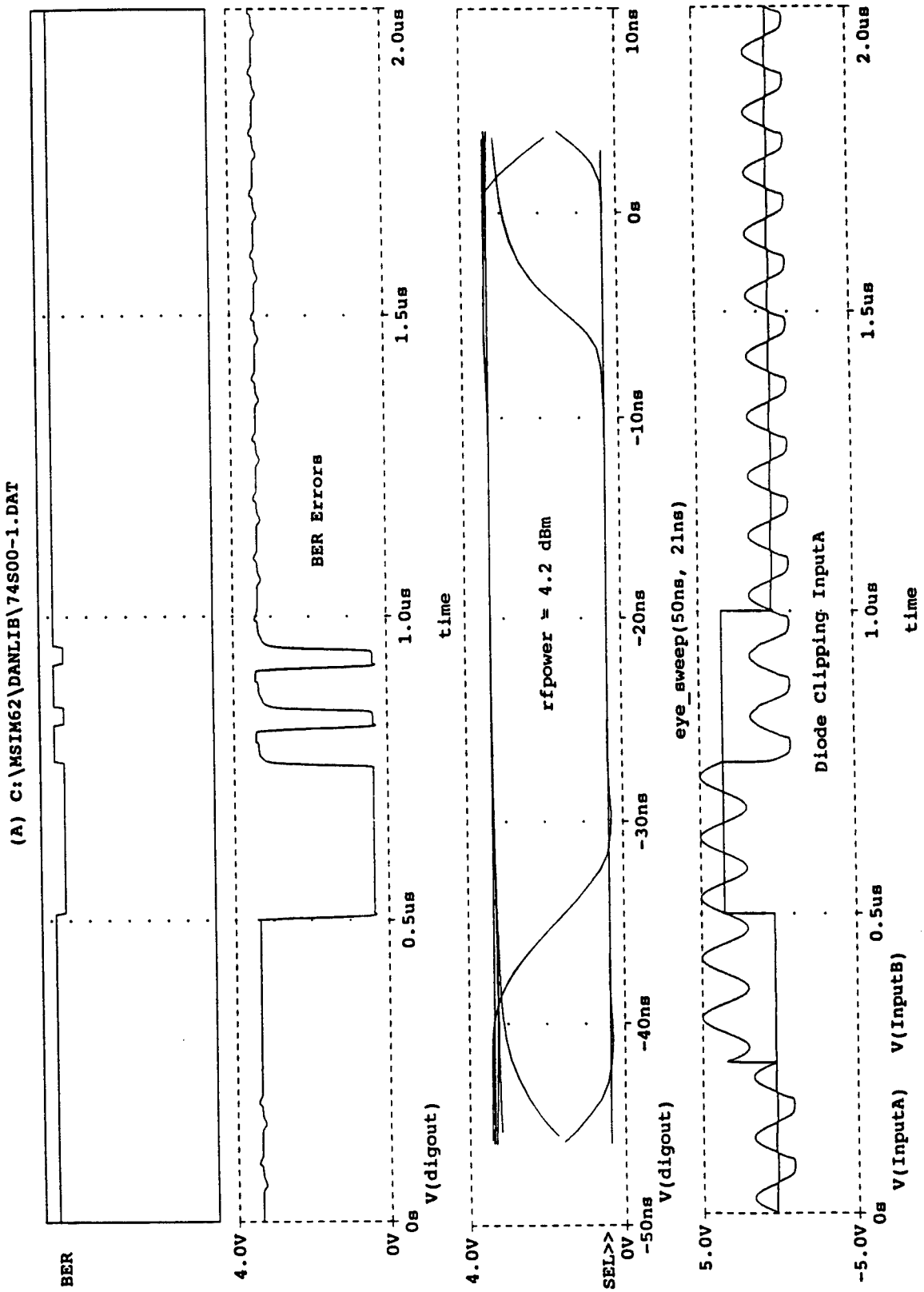


Figure 6-15 Gate Responses and Eye Pattern for 4.2 dBm Power

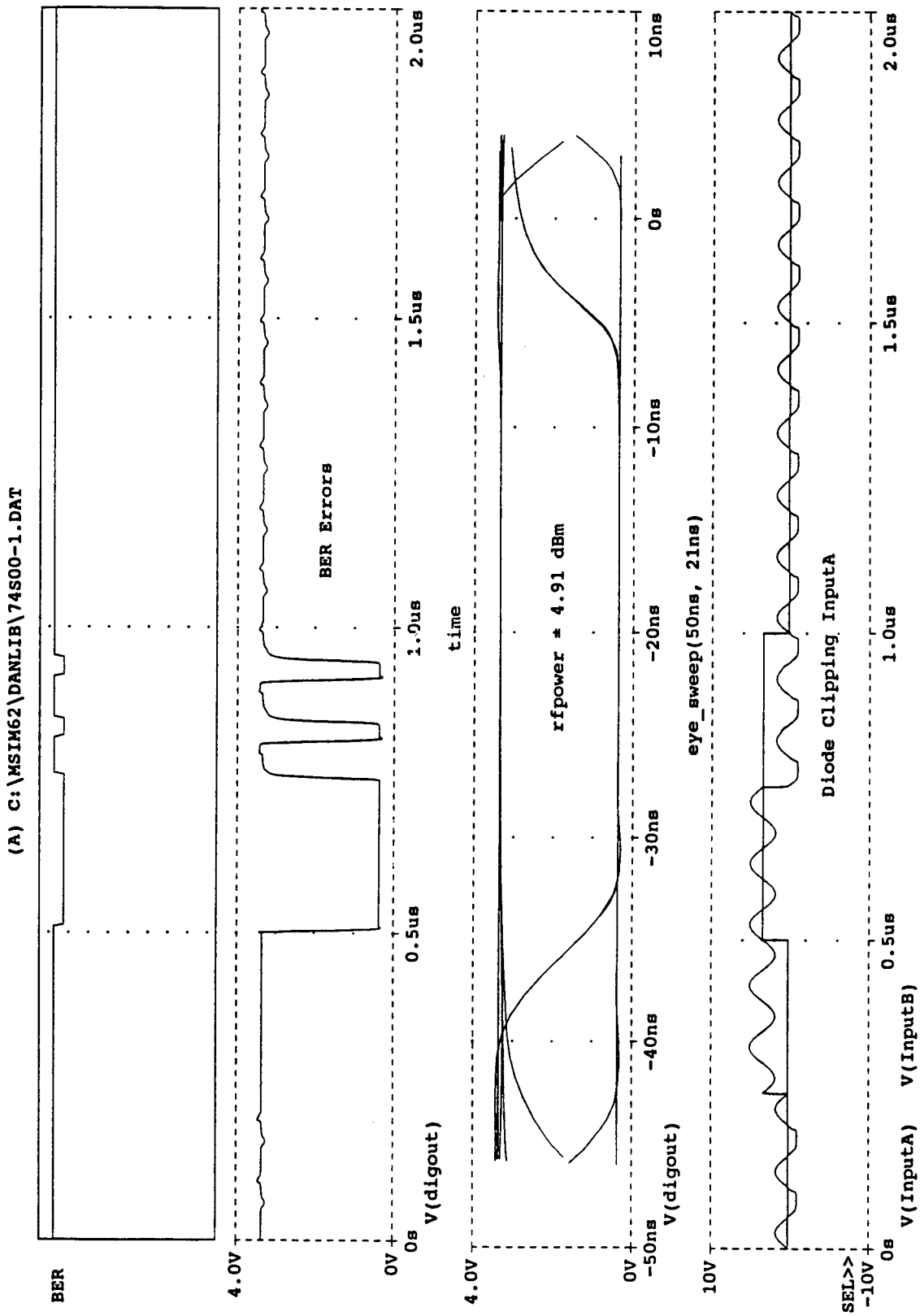


Figure 6-16 Gate Responses and Eye Pattern for 4.91 dBm Power

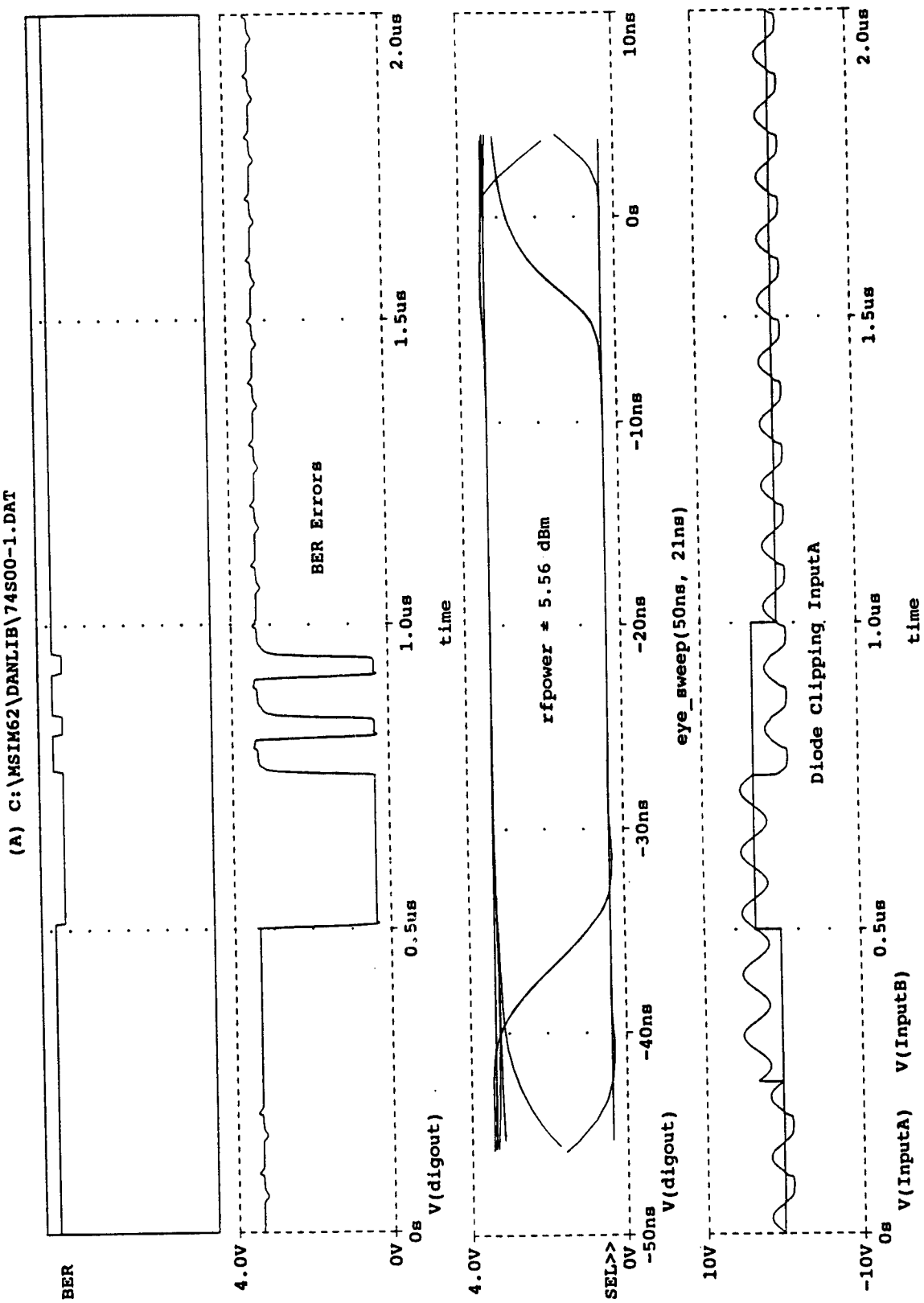


Figure 6-17 Gate Responses and Eye Pattern for 5.56 dBm Power

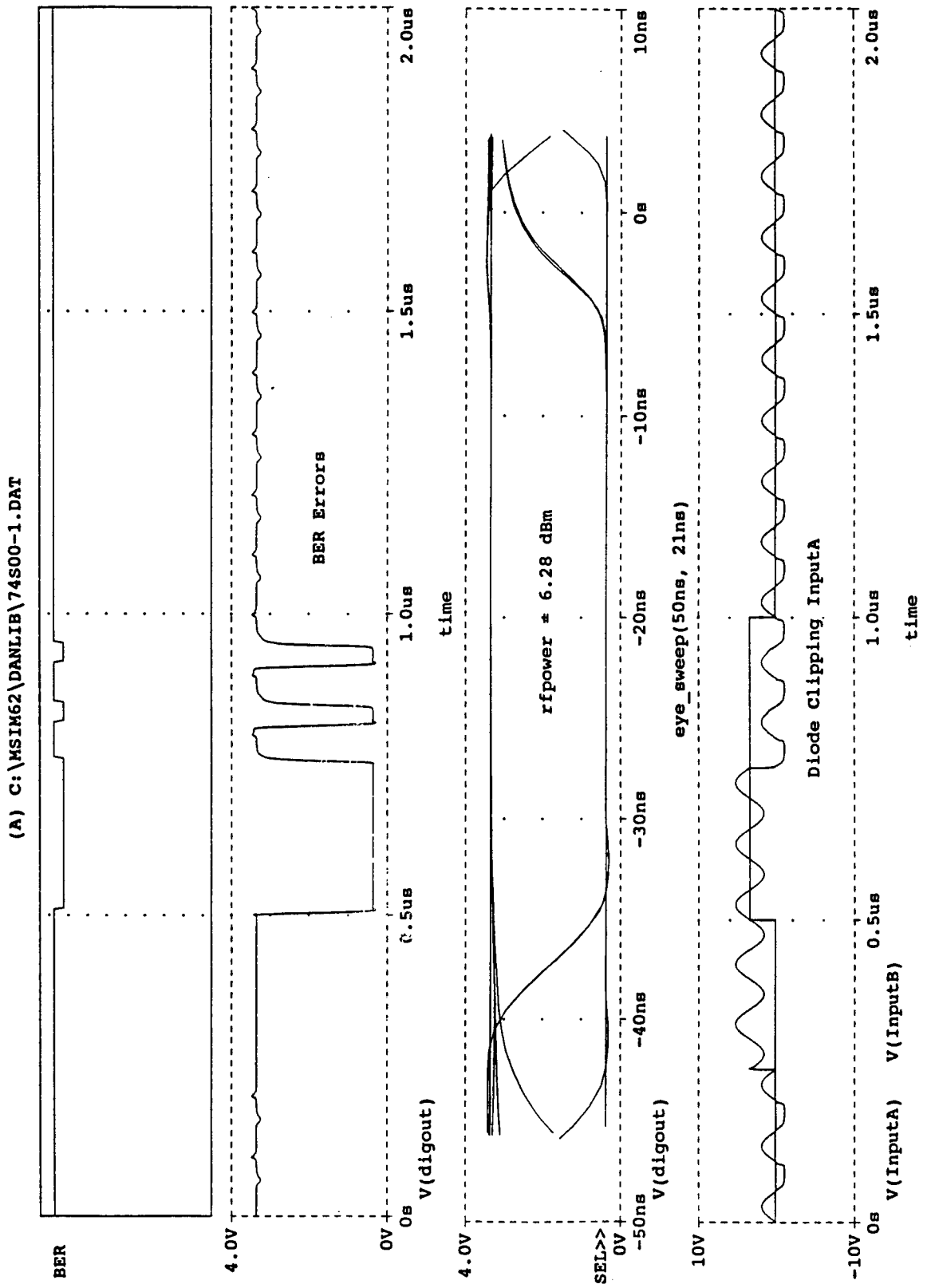


Figure 6-18 Gate Responses and Eye Pattern for 6.28 dBm Power

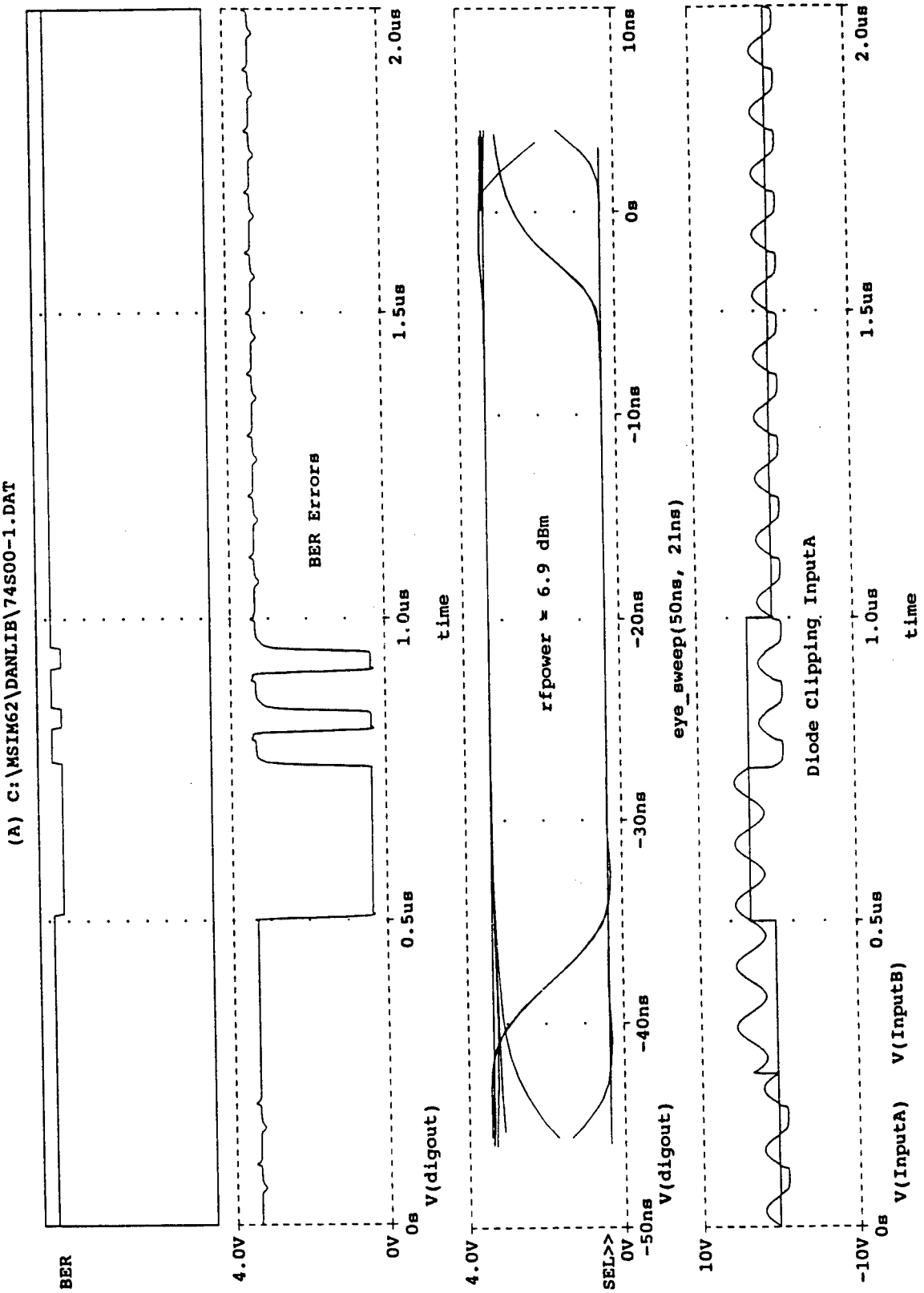


Figure 6-19 Gate Responses and Eye Pattern for 6.9 dBm Power

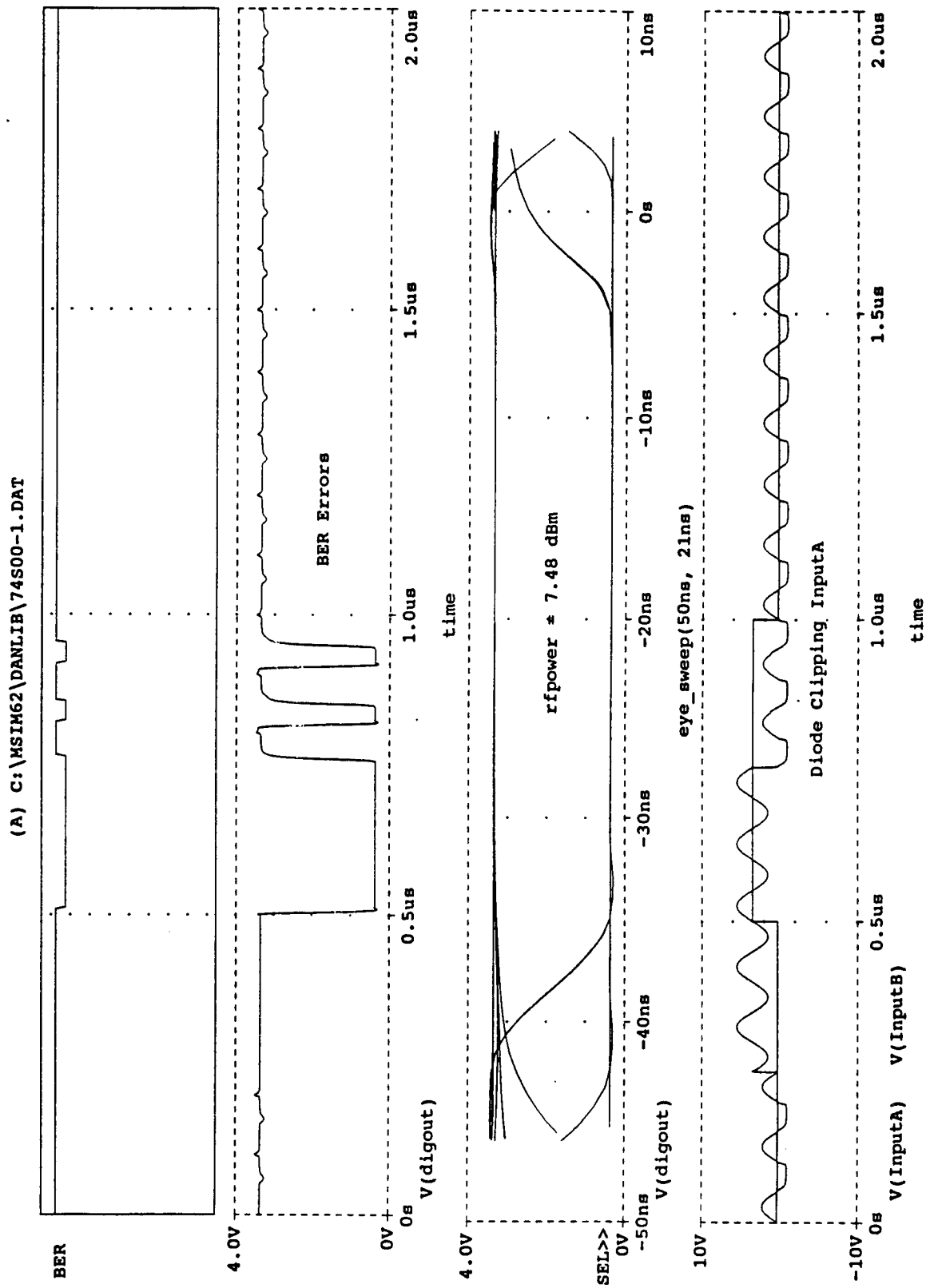


Figure 6-20 Gate Responses and Eye Pattern for 7.48 dBm Power

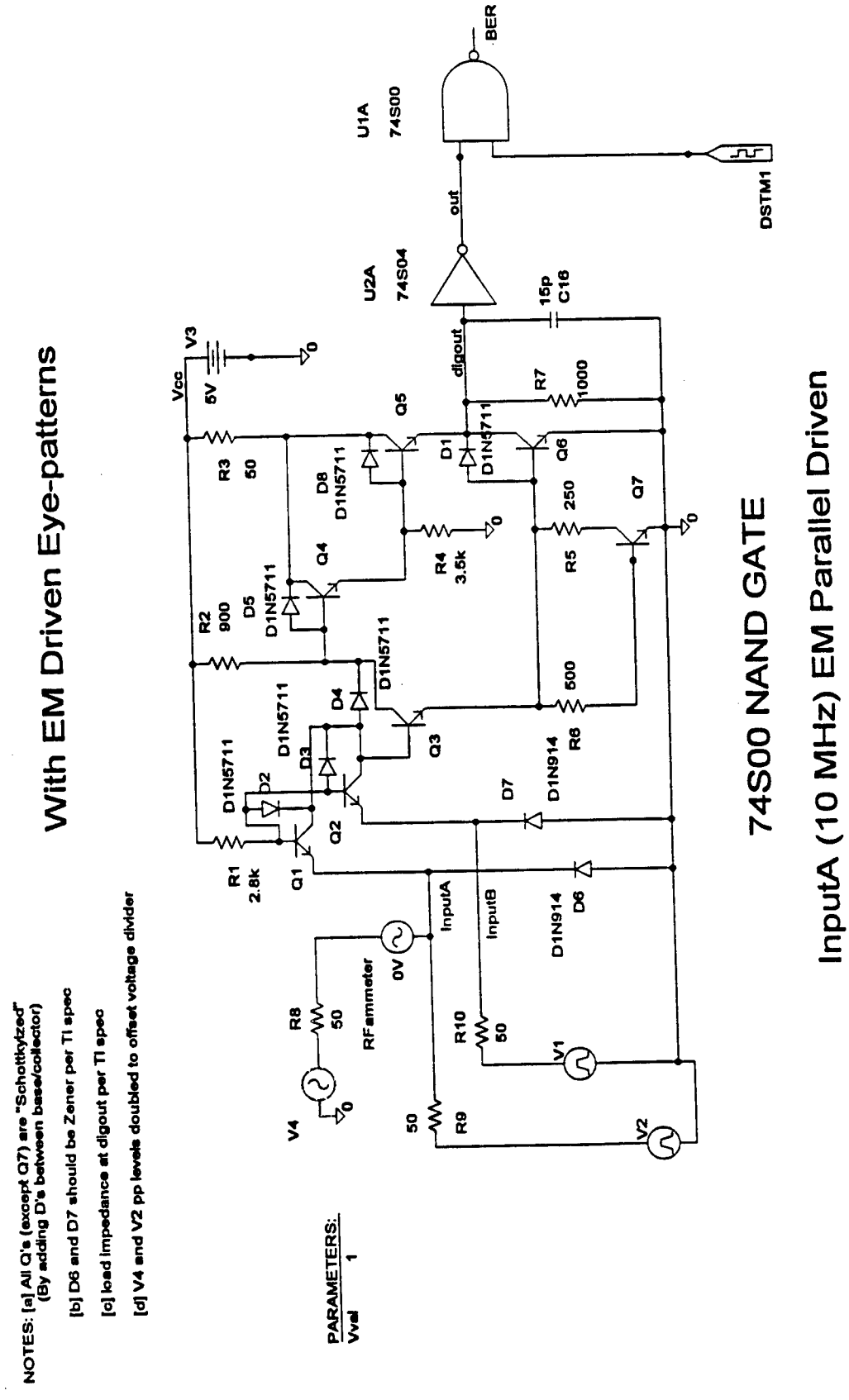


Figure 6-21 Test Gate EM Driven by 10 MHz Voltage Source in Parallel with Logic InputA

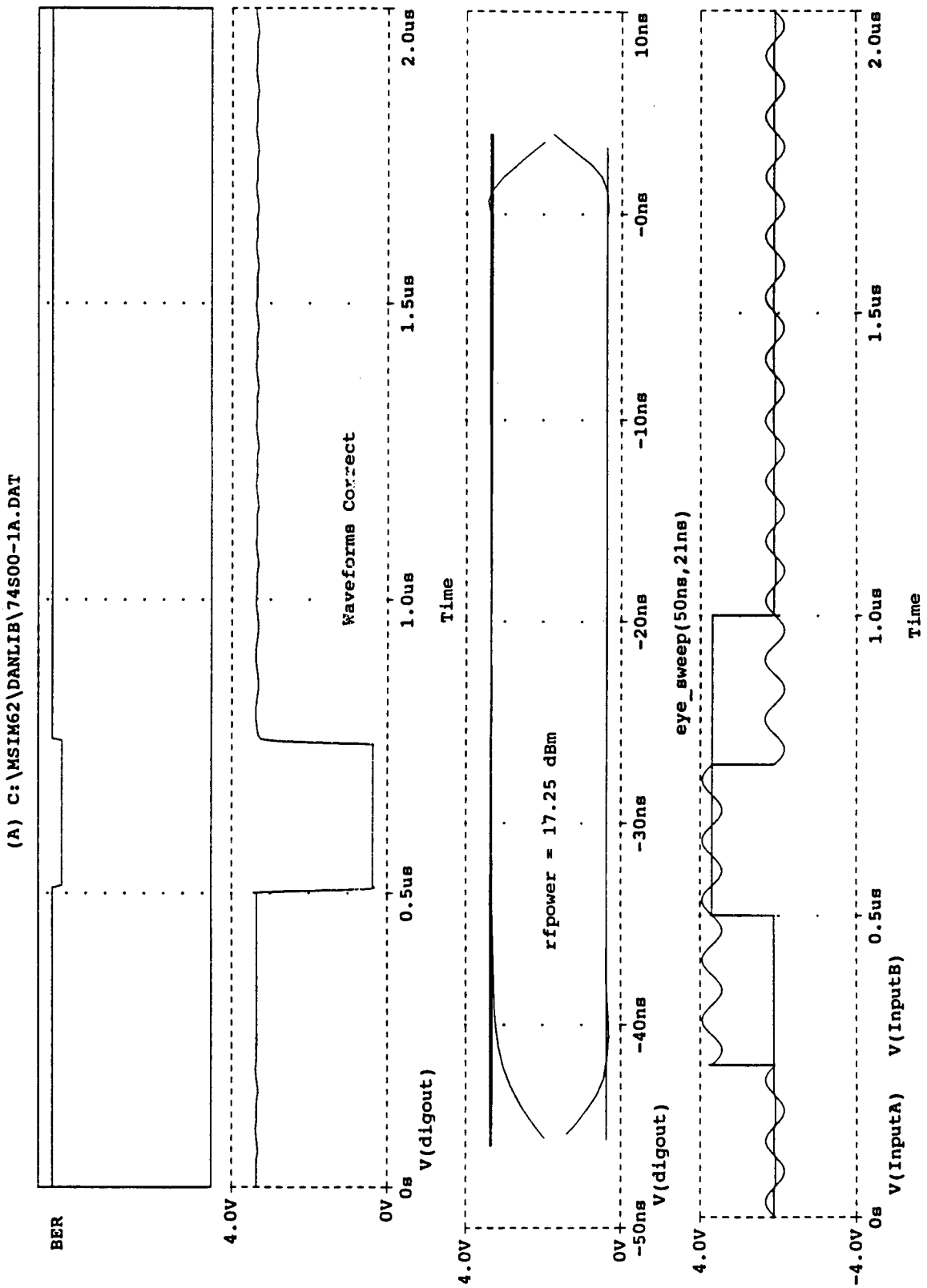


Figure 6-22 Gate Responses and Eye Pattern for 17.25 dBm Power

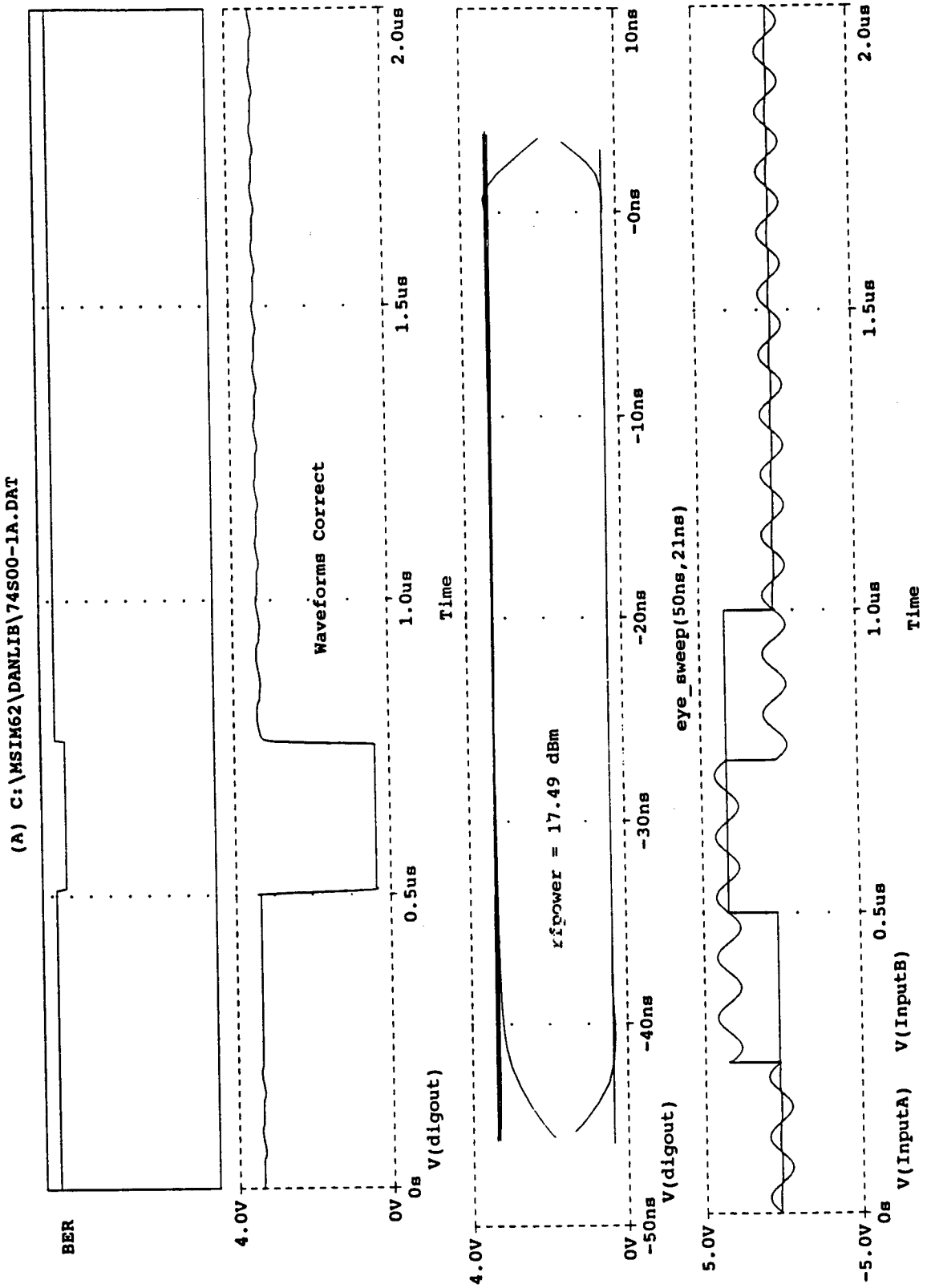


Figure 6-23 Gate Responses and Eye Pattern for 17.49 dBm Power

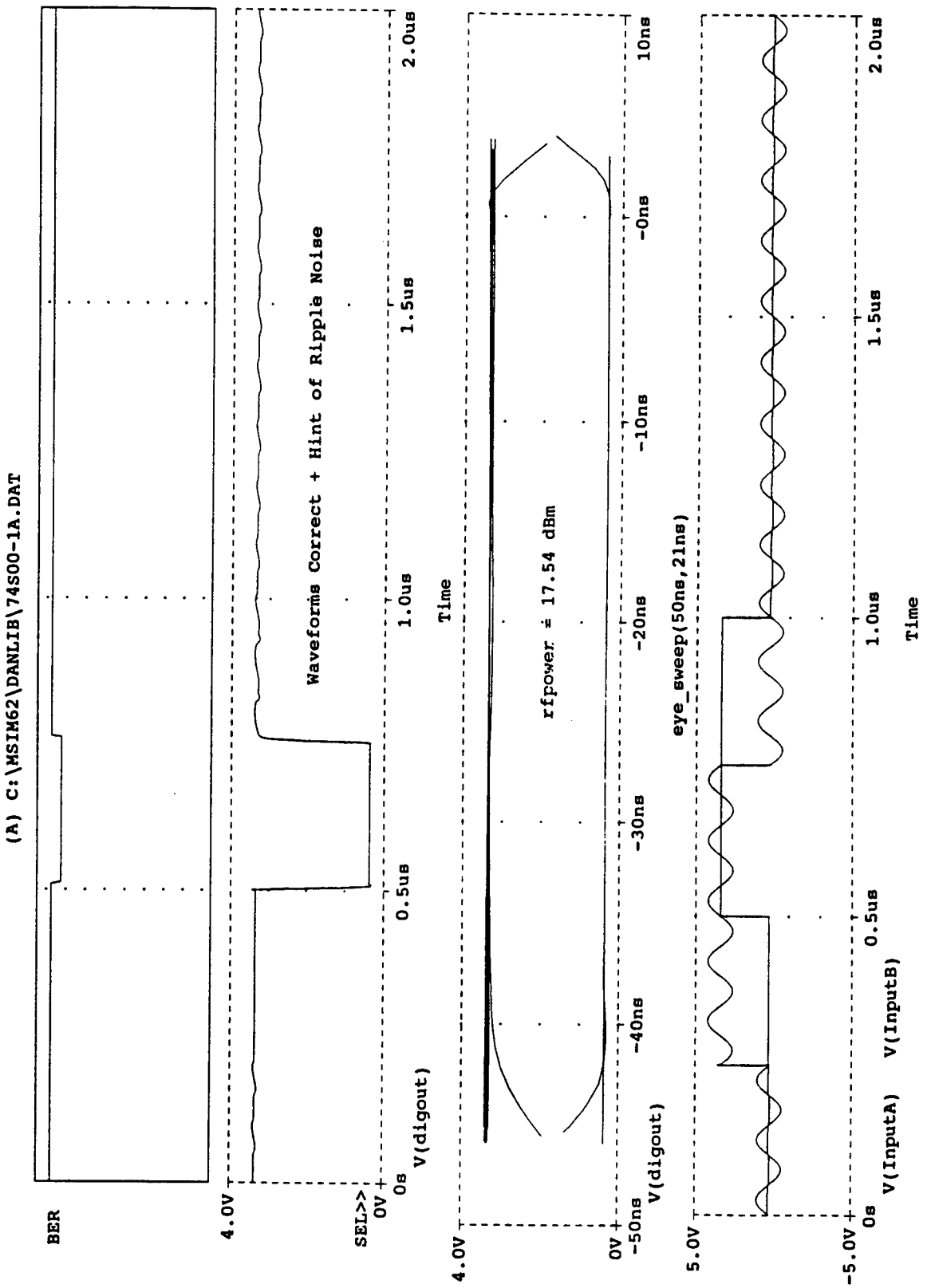


Figure 6-24 Gate Responses and Eye Pattern for 17.54 dBm Power

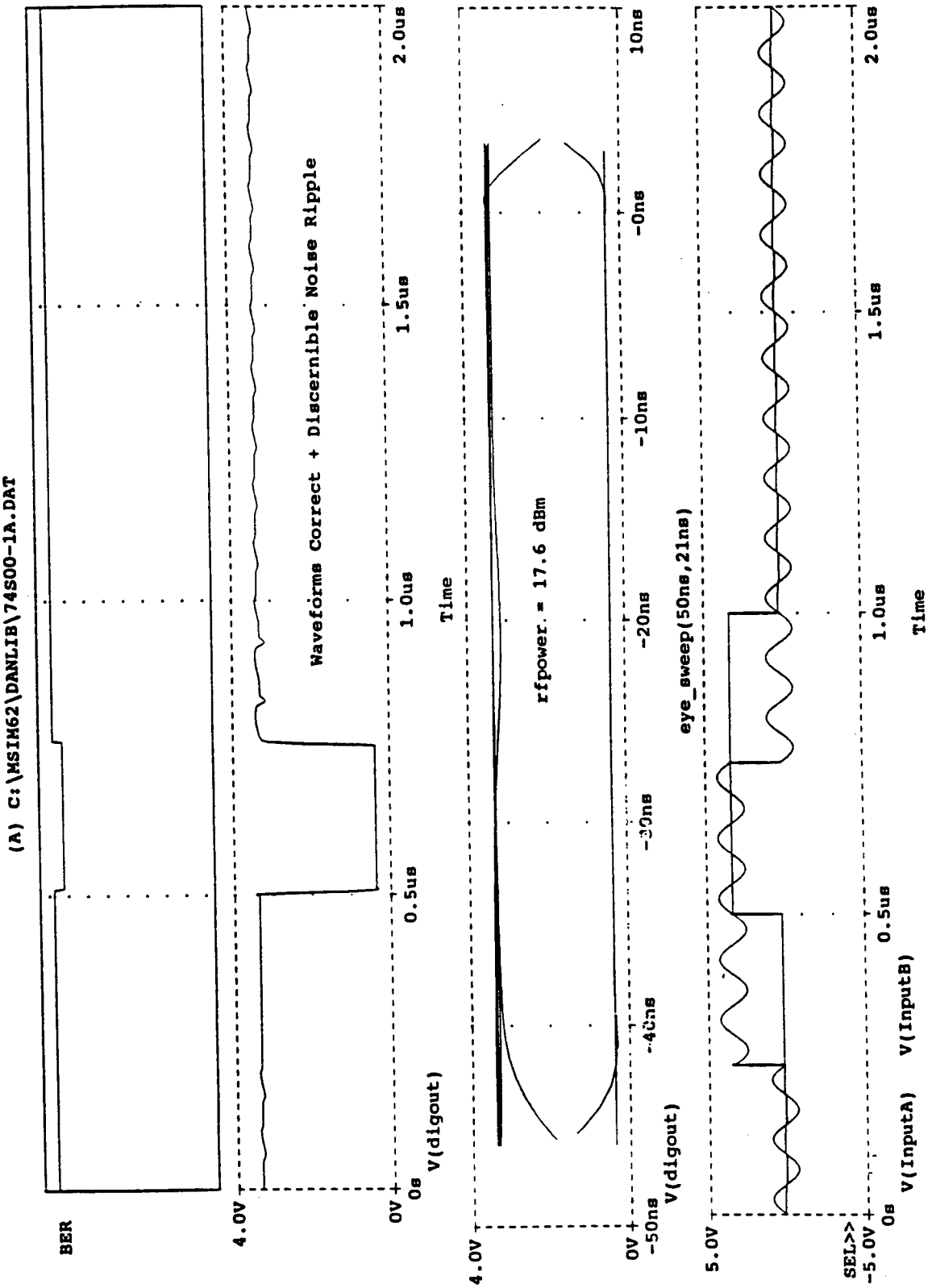


Figure 6-25 Gate Responses and Eye Pattern for 17.6 dBm Power

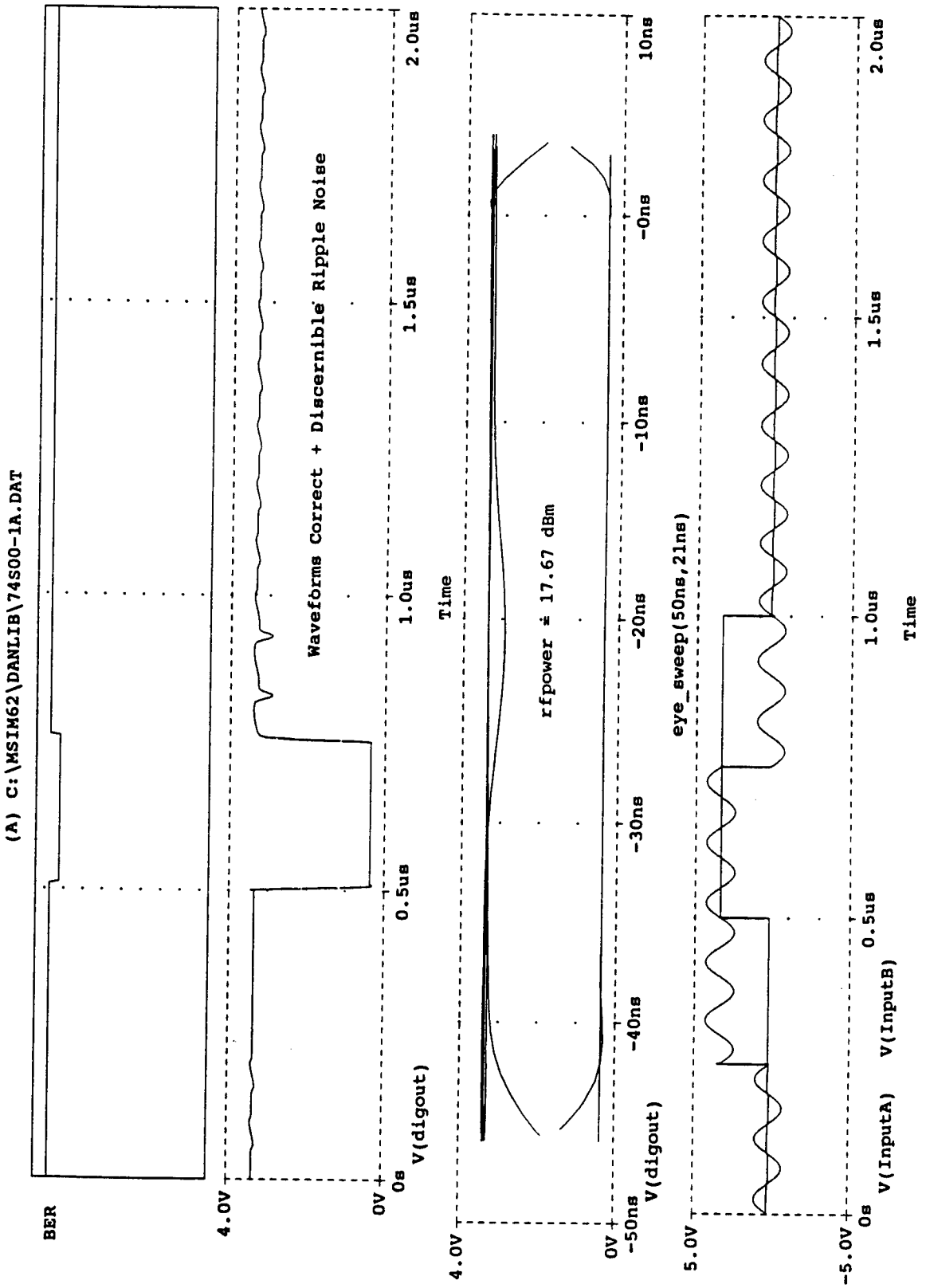


Figure 6-26 Gate Responses and Eye Pattern for 17.67 dBm Power

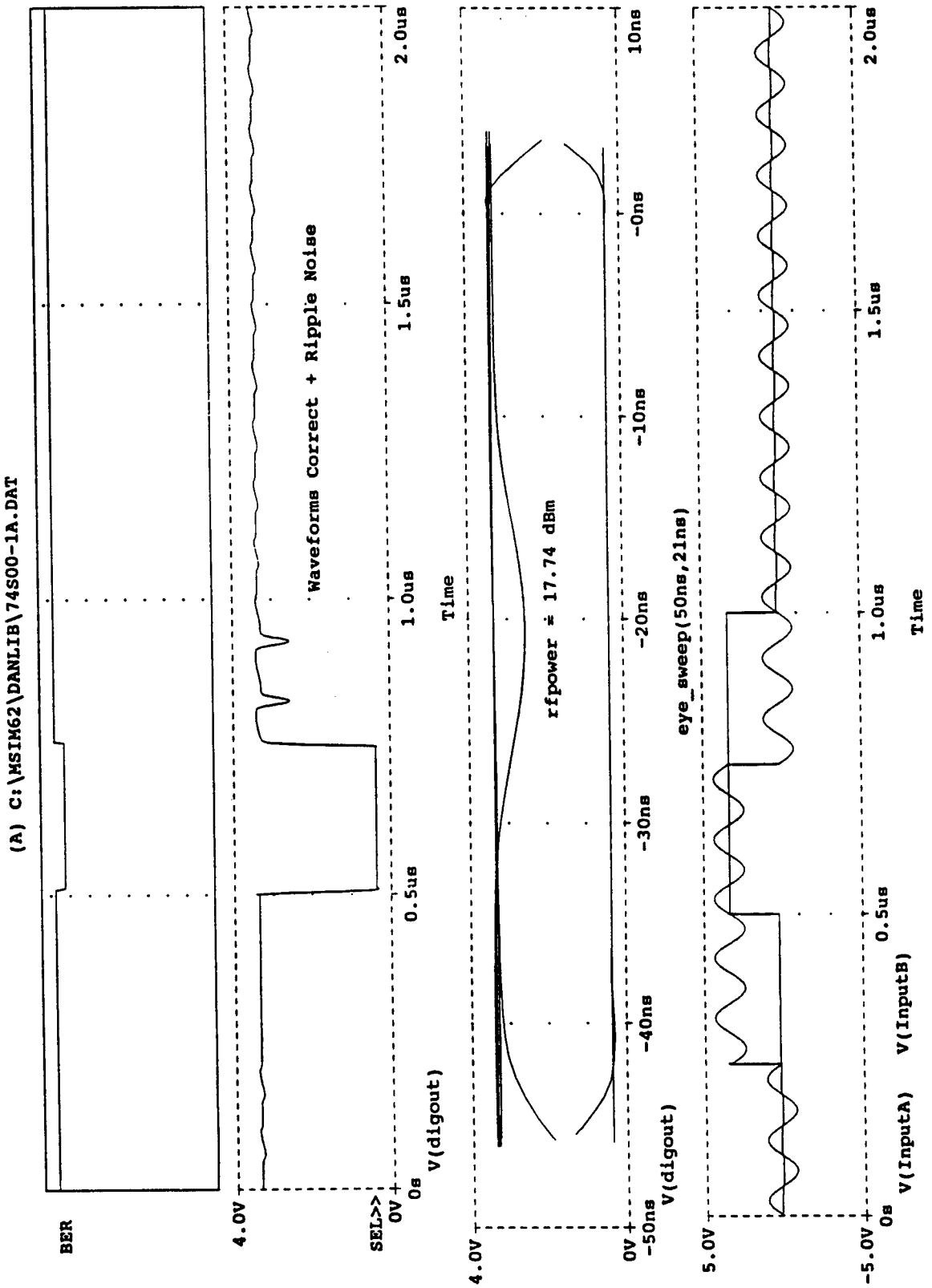


Figure 6-27 Gate Responses and Eye Pattern for 17.74 dBm Power

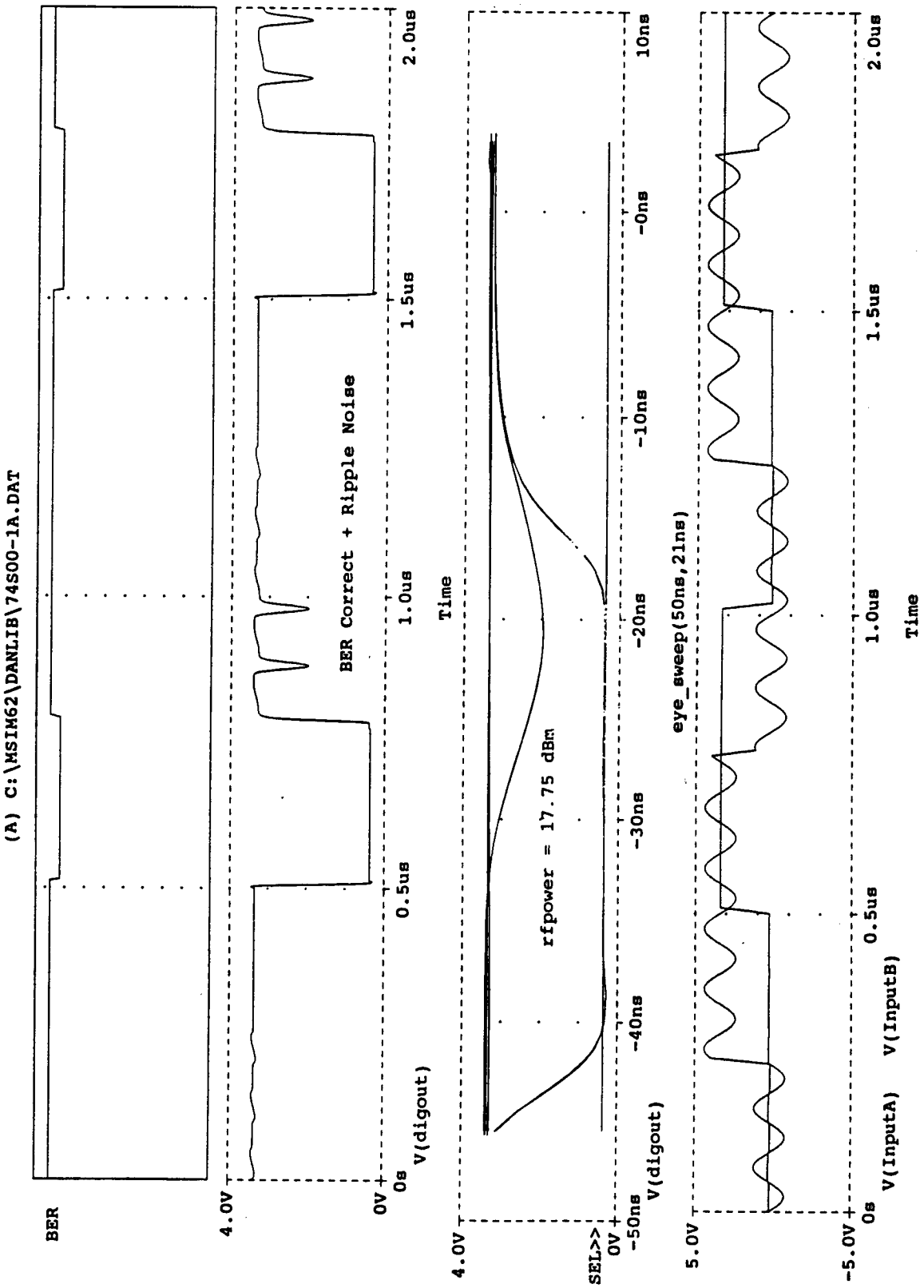


Figure 6-28 Gate Responses and Eye Pattern for 17.75 dBm Power

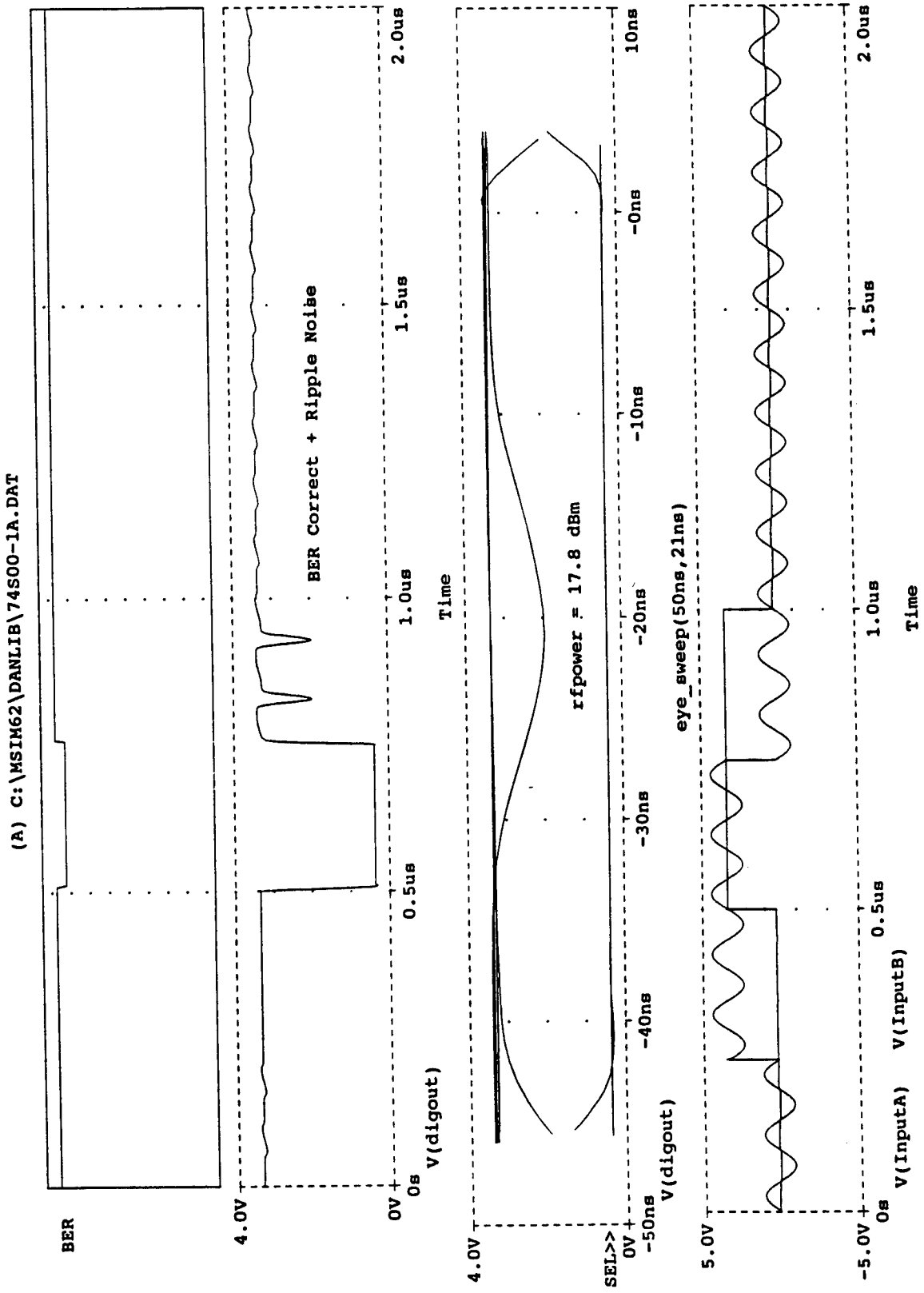


Figure 6-29 Gate Responses and Eye Pattern for 17.8 dBm Power

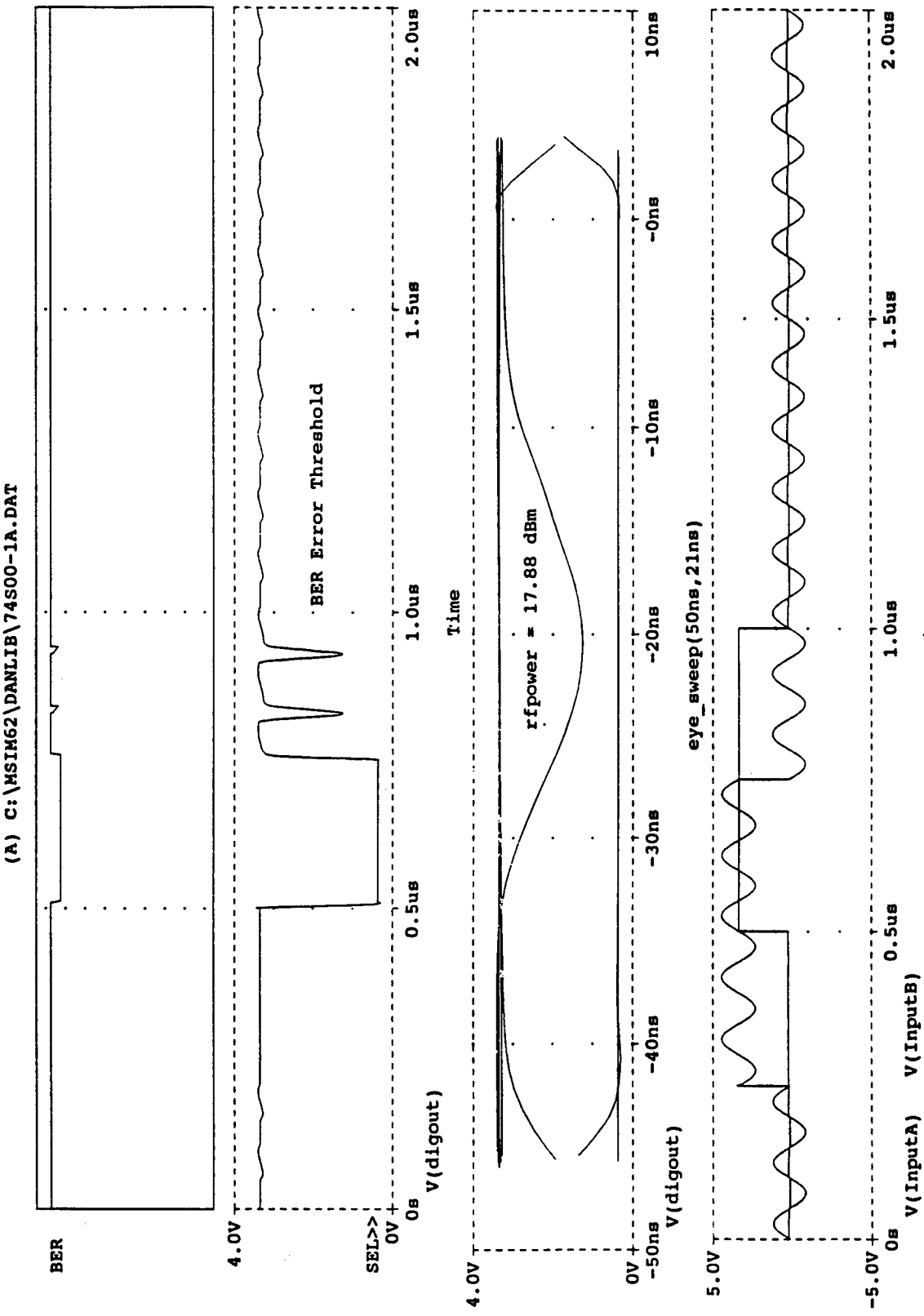


Figure 6-30 Gate Responses and Eye Pattern for 17.88 dBm Power

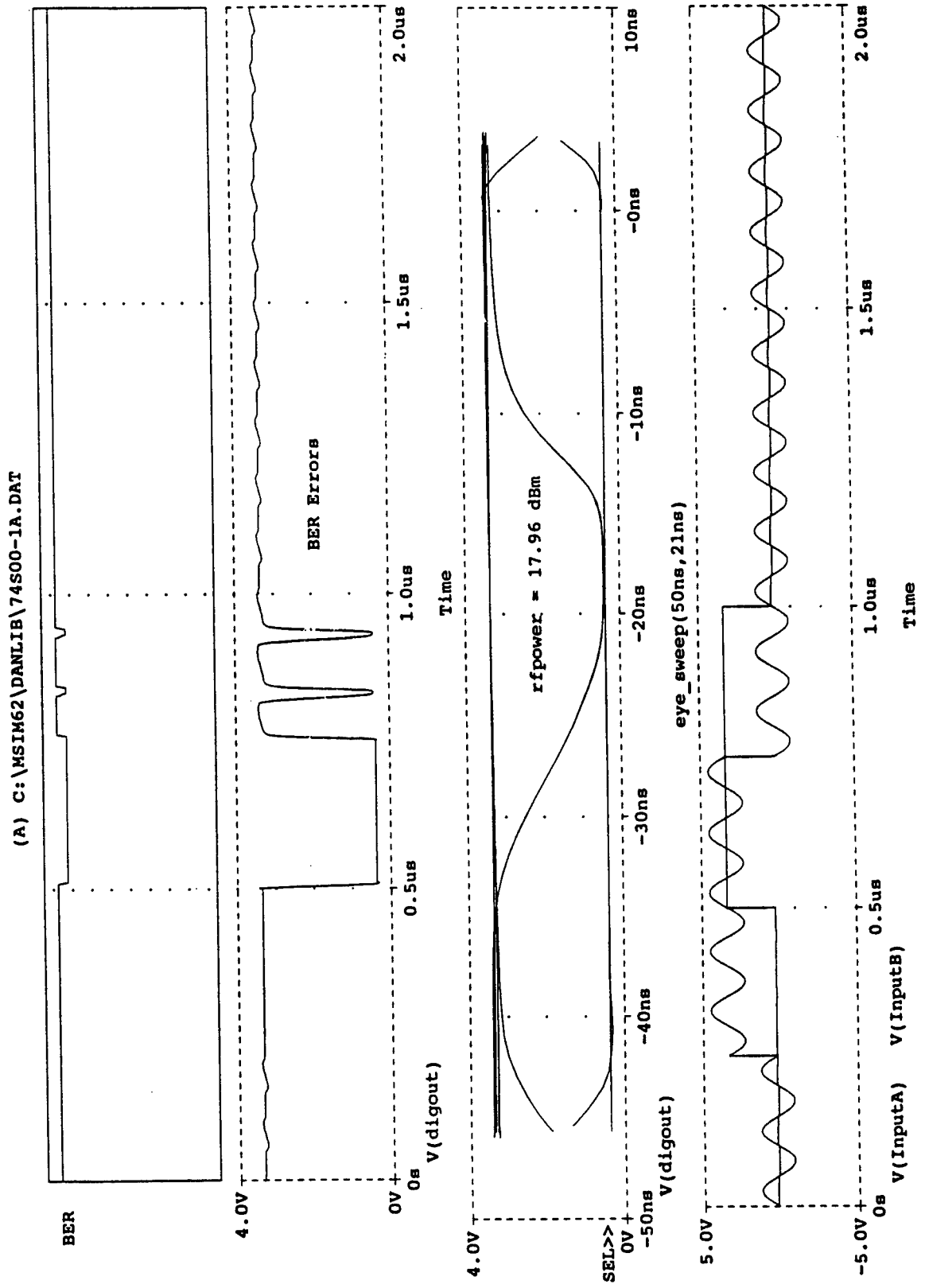


Figure 6-31 Gate Responses and Eye Pattern for 17.96 dBm Power

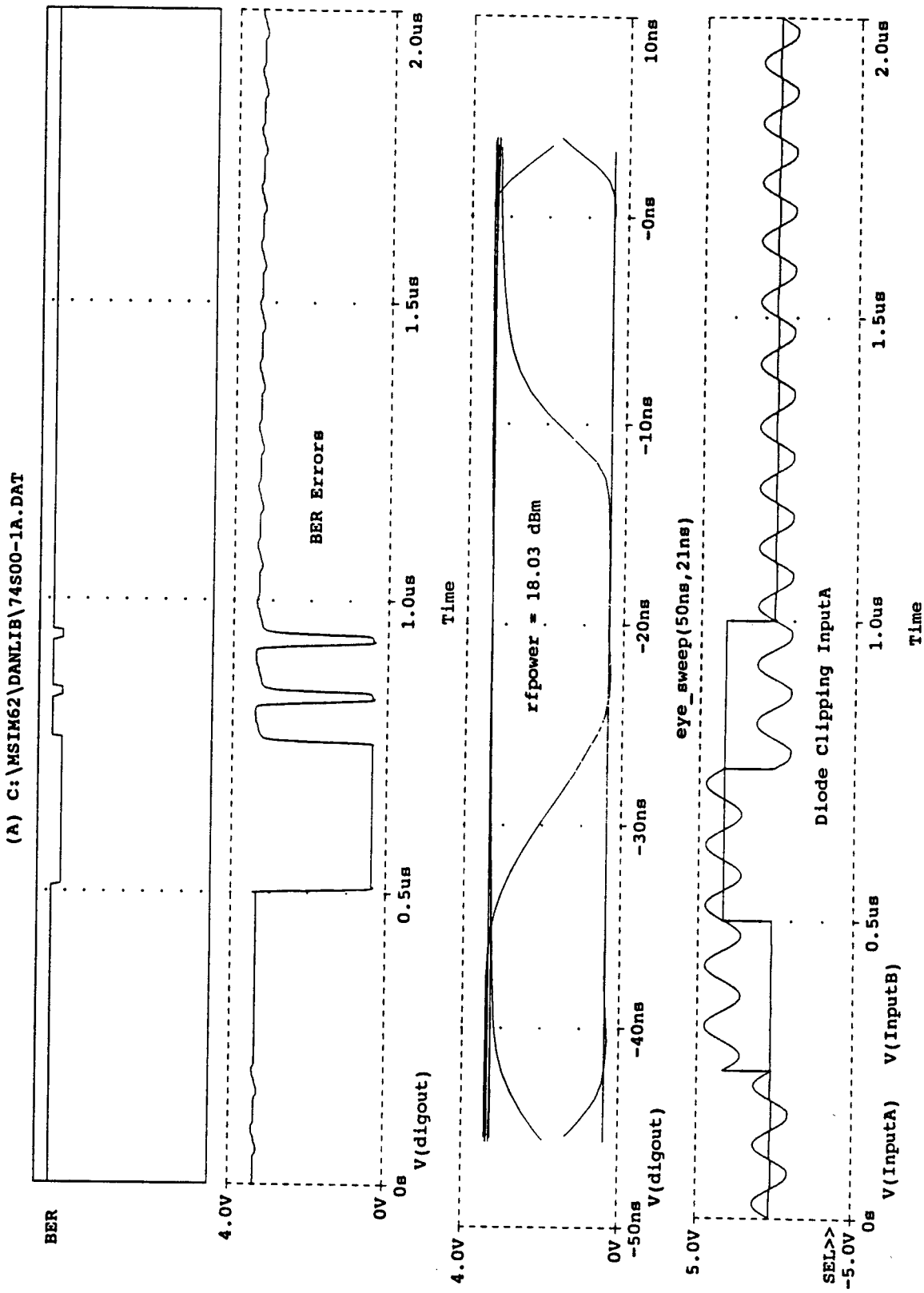


Figure 6-32 Gate Responses and Eye Pattern for 18.03 dBm Power

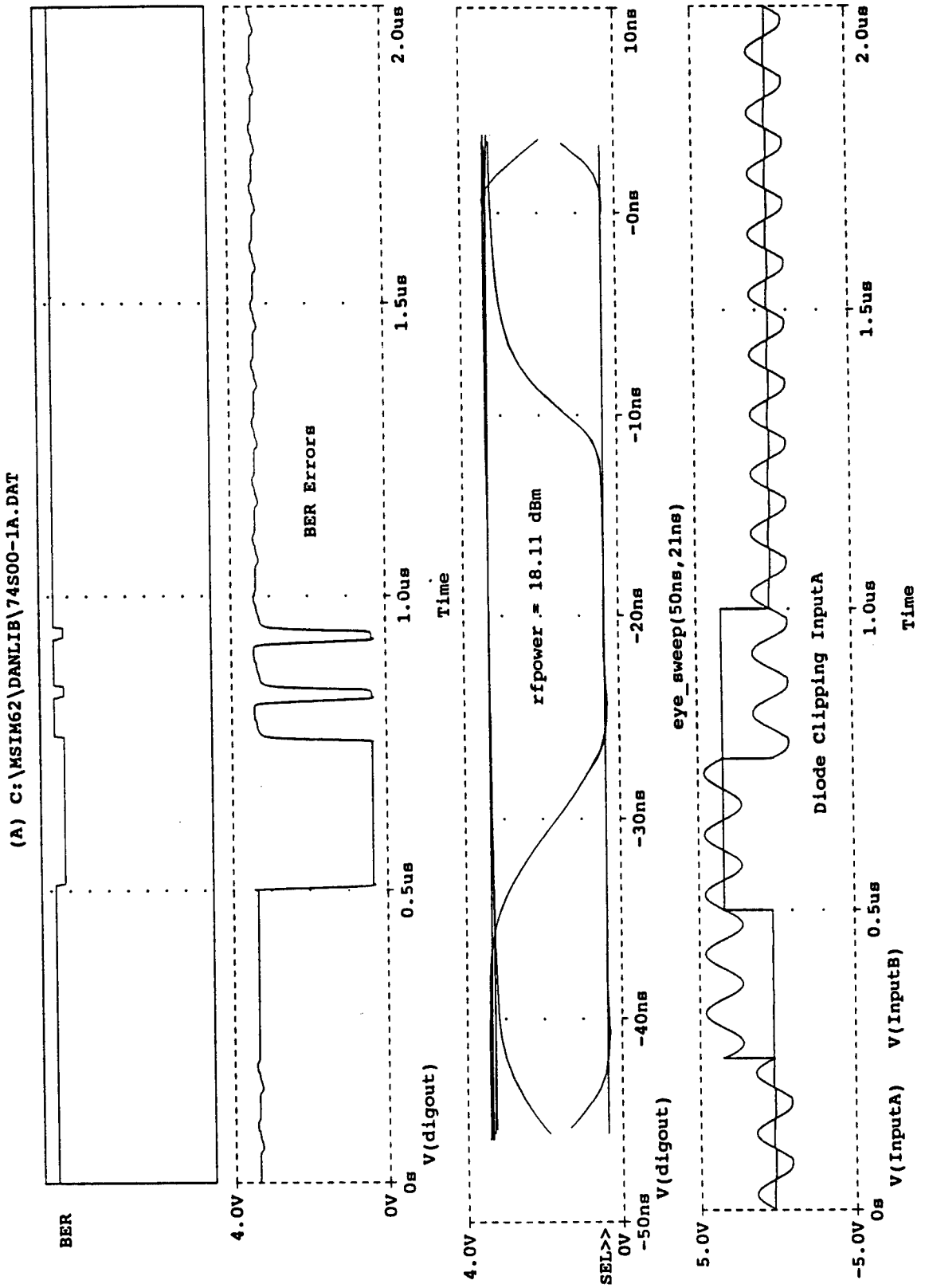


Figure 6-33 Gate Responses and Eye Pattern for 18.11 dBm Power

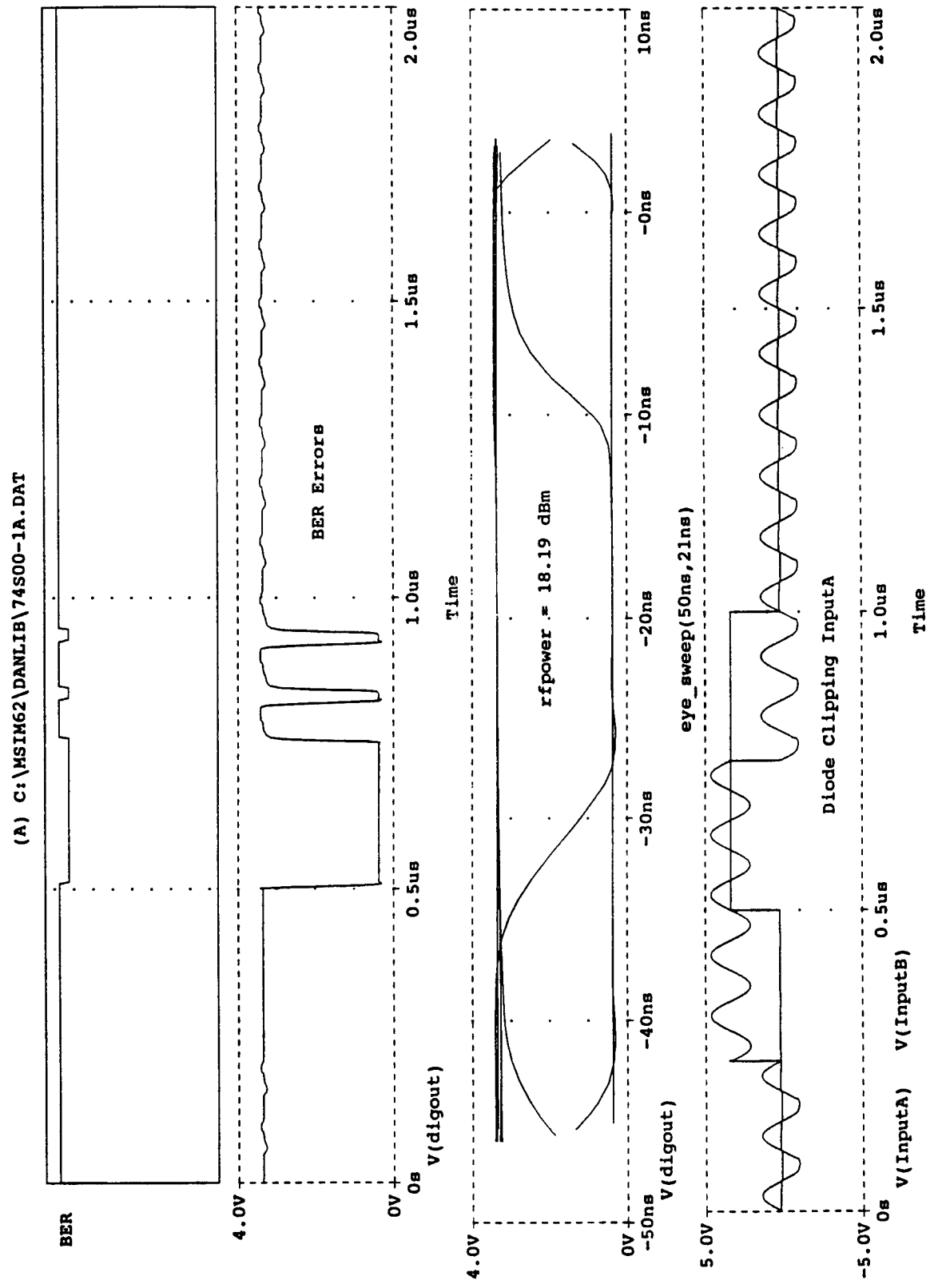


Figure 6-34 Gate Responses and Eye Pattern for 18.19 dBm Power

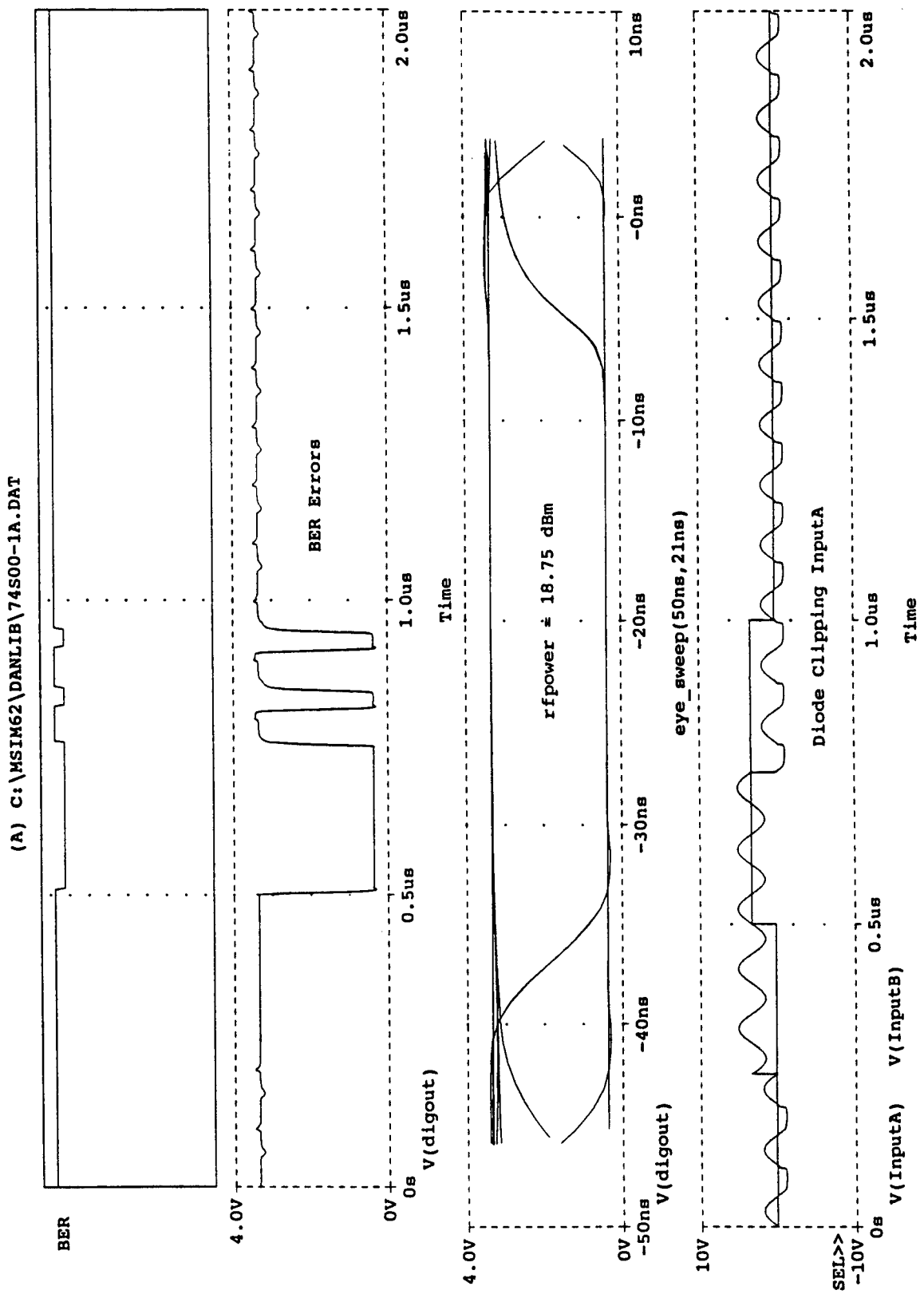


Figure 6-35 Gate Responses and Eye Pattern for 18.75 dBm Power

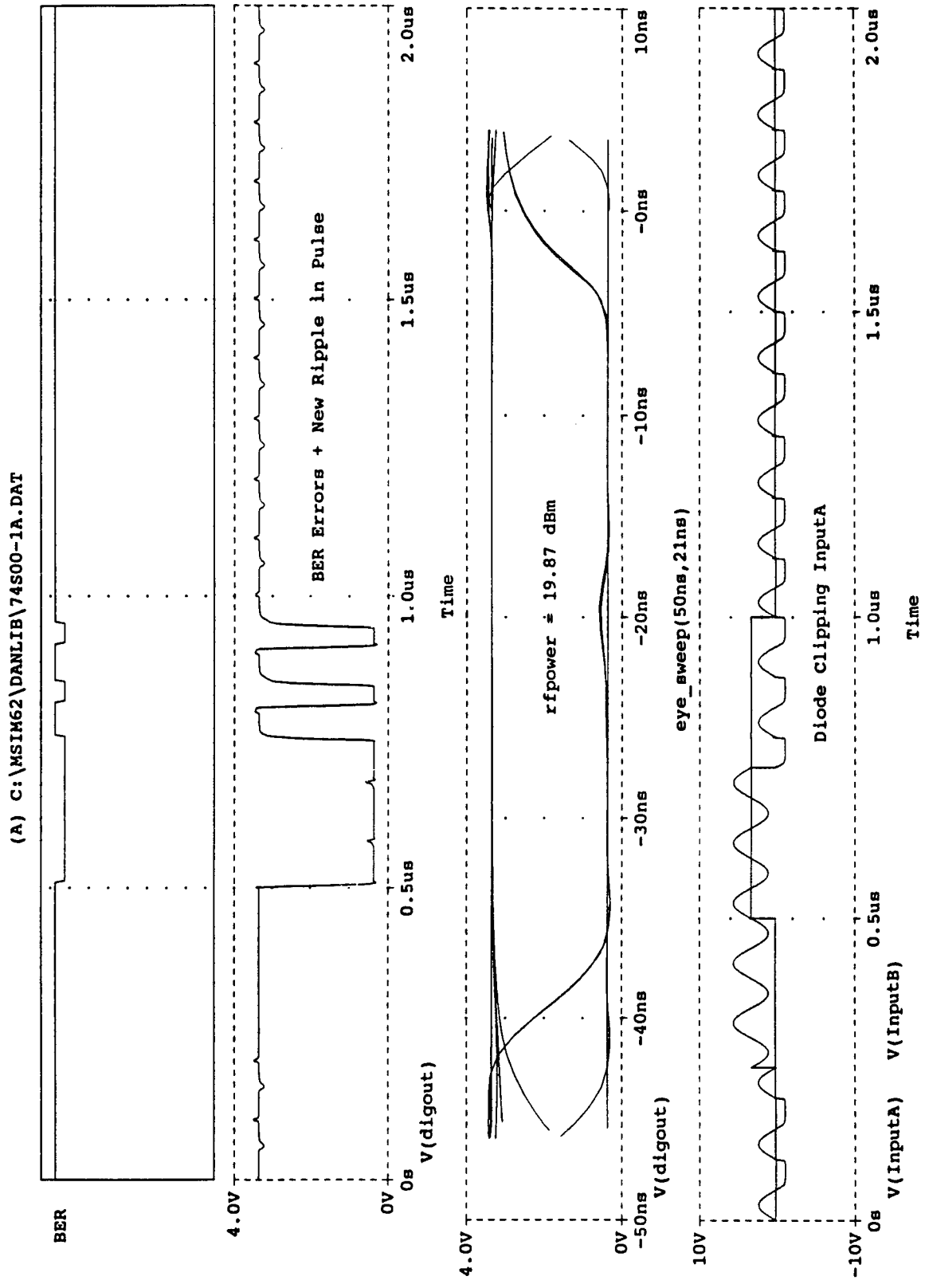


Figure 6-36 Gate Responses and Eye Pattern for 19.87 dBm Power

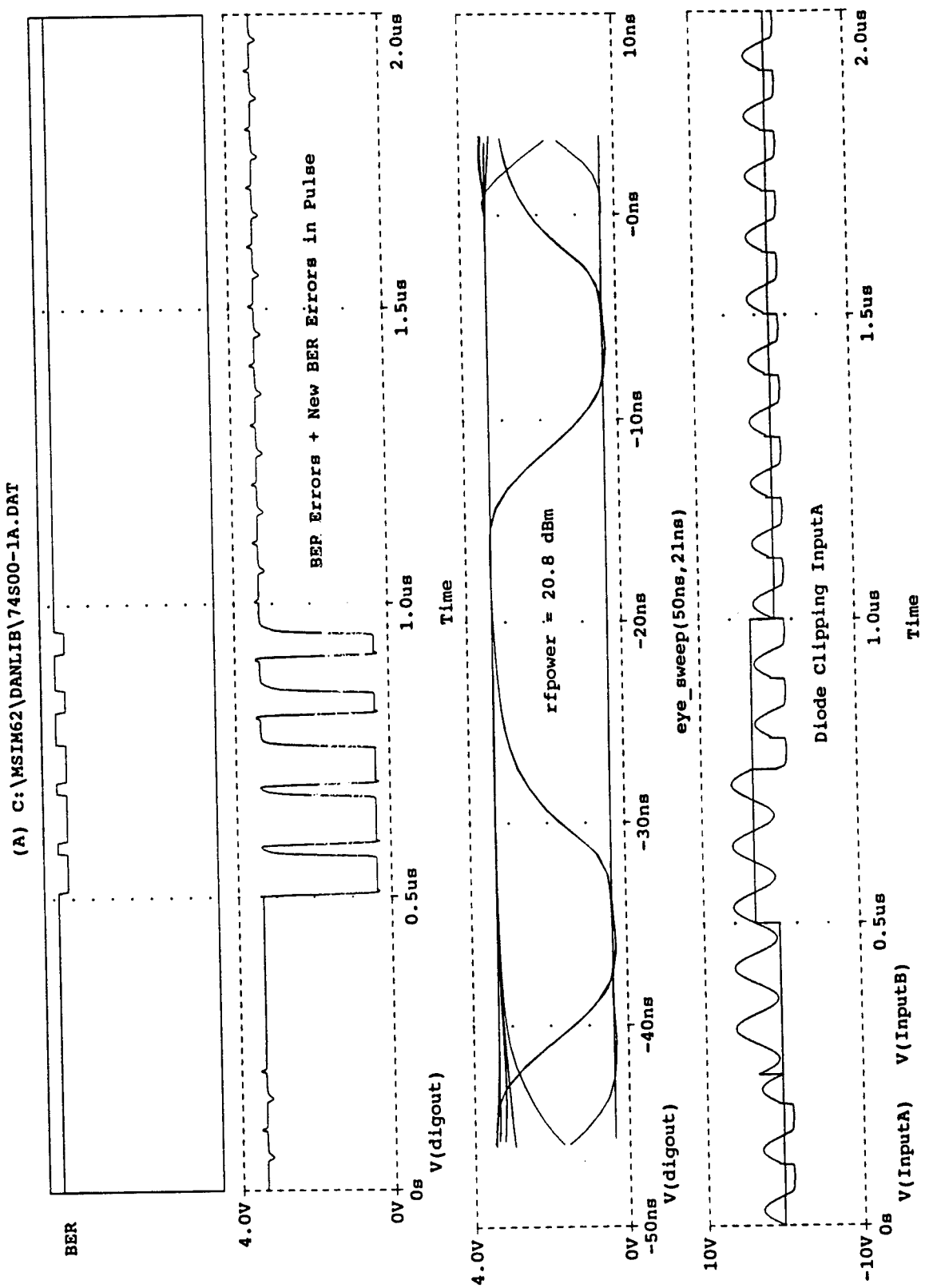


Figure 6-37 Gate Responses and Eye Pattern for 20.8 dBm Power

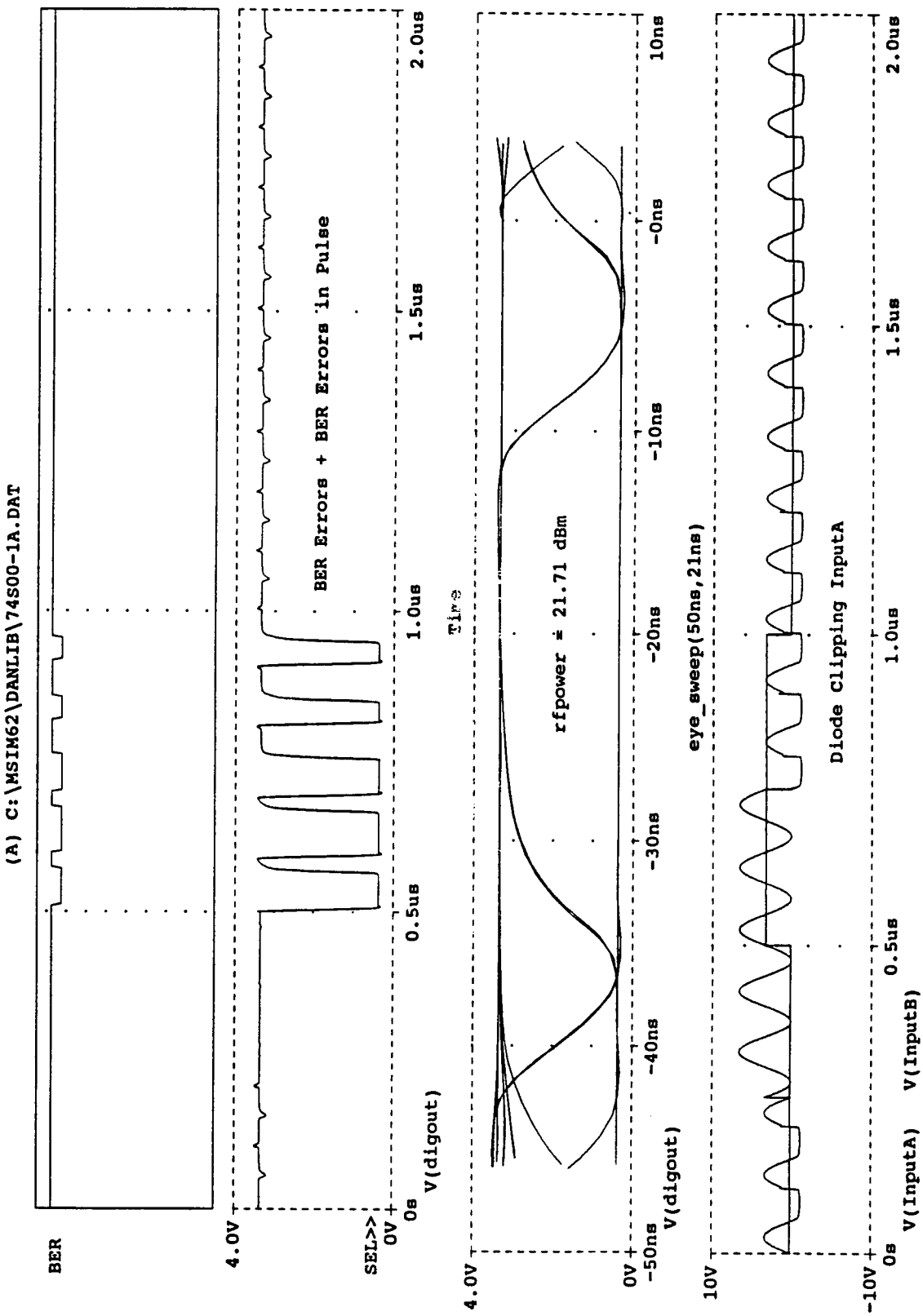


Figure 6-38 Gate Responses and Eye Pattern for 21.71 dBm Power

7. NOISE GENERATORS

In PSPICE, a noise analysis is done in conjunction with an ac sweep analysis. The most common way of computing total noise from a circuit is to first identify and characterize all the internal noise sources in the circuit, including all its active devices, and arbitrarily locate or reference them to the input of the circuit which is now assumed to be "noise free". Further, it is customarily assumed that all these noise sources are statistically independent and generate only noncorrelated, random noise. In practice, this means that although the noise sources may have signed polarity and direction attributes on schematics, voltage and current signs have no real significance. Thus, noise voltages, currents, and powers are added using root-sum-squared values or sums of rms values for each frequency specified in the ac sweep. The noise sources in the circuit may include thermal, shot, and flicker which are related to the circuit resistance values and the semiconductor device parameters extracted from whatever BJT, GaAsFET, and MOSFET models are called out in the circuit library.

In a PSPICE noise analysis, there are two nodes of interest; an arbitrary output node at which all noise powers from all the sources in the circuit are to be summed, and another arbitrary node (as an input) at which an "equivalent" noise source is to be located. The noise power at this latter node is found by taking the total summed noise (i.e., as output noise) at the output node which is customarily the circuit output and dividing it by the device gain (measured to that node) to obtain an "equivalent" noise source at the input which is customarily the circuit input. The meaning of all this is that we can now think of the "equivalent" noise source power as now driving a "noise-less" circuit. The analysis computes each noise source contribution as a voltage or current spectral noise density (i.e., volts per root hertz or Amperes per root hertz) over a one hertz bandwidth. Computational results are typically the noise spectral densities V(ONOISE) and V(INOISE) at the circuit summing node and at the reference node, respectively. The latter node is usually taken to be the input signal source. The total rms wideband noise voltages at the output and input ports are found using the

PSPICE post processor as the square roots of the integral of the squares of V(ONOISE) and V(INOISE), respectively. This is the root-mean-square value in the frequency domain where the limits of the integration are band limited to the frequency sweep used. In this version of PSPICE, using the math operator "rms" from the post processor to compute the wideband noise voltages led to an error. Apparently, "rms" seems to work only in the time domain.

Noise sources are also useful in modeling test setups used for measuring noise figure of circuits and in finding circuit responses to random input signals of various spectral distributions. This can be done using the piece-wise linear (pwl), time waveform modeling available in PSPICE. An arbitrary voltage or current waveform can be synthesized as a pwl waveform by describing it with a sequence of paired coordinates in both time and amplitude, called point pairs. At each time point of a pair, the corresponding amplitude is assigned as a "corner" of the pwl waveform. The basis of pwl randomness is the selection or generation (off line) of a sequence of random numbers with a Gaussian distribution, although the method should work for any other statistical distribution. A time sweep is selected for which the circuit transient response is of interest and is divided by the total number of random numbers selected to give a time duration for each pwl source. Then the number of pwl sources is selected. Each pwl source will be assigned a random amplitude at each time interval in its assigned duration until the entire sweep is covered.

For example, say the sweep of (circuit response) interest is 2 us or 2000 ns and the total number of random numbers available is 100; then a time interval (step) is 20 ns. If we decide to use 5 independent (pwl) sources to model the 100 random numbers, then we assign a duration of 400 ns to each source, and let each one sequentially account for a total of 20 intervals of random amplitudes over its duration of 400 ns. So, pwl source #1 will assign random numbers as voltage amplitudes in a time window from 20 ns to 380 ns at each 20 ns interval, and zero amplitudes to the outside intervals (0 and 400 ns); pwl source # 2 will assign random amplitudes in the time window from 400

ns to 780 ns at each 20 ns interval, and zero amplitudes to the outside intervals (380 ns and 800 ns); pwl source # 3 will assign random amplitudes in the time window from 800 ns to 1280 ns at each 20 ns interval, and zero to the outside intervals (780 ns and 1300 ns); and so on. In other words, each source uses a subset of random voltages (18 actually) and zero's in 20 ns step intervals for each duration of 400 ns. In our example, the 5 sources in sequence will use up 90 random number to cover 2 us and 100 random numbers to cover 2.2 us. These pwl sources are then connected in series and sequentially distributed in time until the total sweep of interest is covered. Because of the need for overlapping windows (to effectively turn on and shut off the sequential sources) and counting time epochs of zero amplitudes, more or less random numbers or pwl sources may be required to cover a given sweep. These concepts will now be demonstrated.

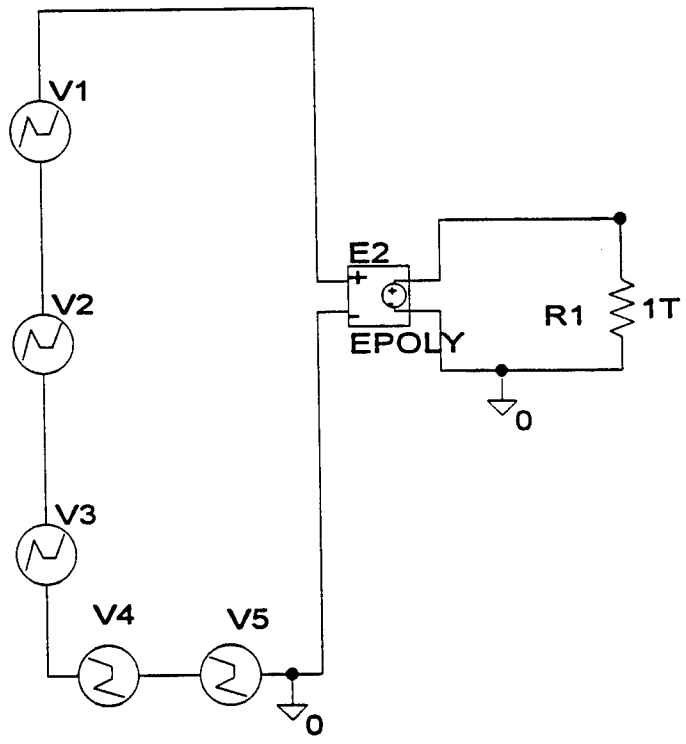
Figure 7-1 shows a low frequency noise source synthesized from piece-wise linear sources V1 to V5. Figure 7-2 shows its net list and details of the time distributions discussed above. Figure 7-3 shows the open-circuited responses to this Gaussian input: (a) shows the time domain response to 3.5 us., (b) shows its rms value of approximately 15 nV over a 3.5 us sweep, (c) shows its rms and average value of approximately zero (as it should be) over a 3.5 us sweep, and (d) shows its frequency spectrum out to 30 MHz. Figure 7-4 shows how time limited pwl sources can be expanded using voltage dependent, voltage sources to obtain time extensions or time summing the three. Figures 7-5 and 7-6 show related responses. Figure 7-7 show how two independent (i.e., no correlation) noise sources can be generated and combined. Figure 7-8 shows the netlist and time distributions needed. Figure 7-9 show the relevant responses; including the rms summed voltage in (d). Figure 7-10 shows another approach to noise generation that uses available shift registers and gates in a conventional configuration: figure 7-11 shows the net list. While this noise generator was selected from the literature as representative [1], it was not simulated in this program.

Figure 7-12 shows an attempt at a low noise UHF amplifier which turned out to be not so low

noise as wideband. Figure 7-13 shows its "final" net list after some considerable tweaking. Figure 7-14 is included to illustrate the kinds of device files that are available and easily modifiable in the PSPICE parts' library. Figure 7-15 shows the relevant results. While the gain is modest, its bandwidth is considerable, and its noise figure acceptable. The point here is not to design an amplifier but to demonstrate post analysis macros that are available to manipulate and characterize the design results. Note that the noise bandwidth computation seems strange - a noise bandwidth smaller than the design bandwidth. Further analysis indicated that there seems to be an error or code bug in using the node voltages at input and output ports to compute noise bandwidth. The error or bug seems to be in not using magnitudes (M) of the node voltages of interest. Interestingly, Motchenbacher and Connelly already alluded to this very possibility in PSPICE in their popular text [2], but this author (mistakenly) assumed the error had been corrected. Figure 7-16 shows the corrected noise bandwidth using magnitudes of the node voltages instead of just the node voltages. The noise bandwidth is correctly shown as a little more than the signal bandwidth, as is to be expected.

[1] D'Alvano, Francisco and Badra, Remy E., "A Simple Low-Cost Laboratory Hardware for Noise Generation", IEEE Transactions on Education, Vol. 39, No. 2, May 1996.

[2] Motchenbacher, C. D. and Connelly, J. Alvin, "Low Noise Electronic System Design", Wiley Interscience Publications, John Wiley & Sons, Inc., New York, NY, 1993.



LOW FREQUENCY NOISE GENERATOR

Figure 7-1 Low Frequency Noise Source Synthesis

```
* Schematics Netlist *
* Canonic Noise Generator/Created by DJK 11-23-95
* Modified 04-09-96


V_V1          $N_0001 $N_0002 DC 0 AC 0
+PWL 0 0 100n -.5059494 200n 1.25103432 300n 1.12552402 400n -1.10
173531 500n
+  -.5376212 600n 1.04056649 700n 1.53779272 800n 0 1000000n 0
V_V2          $N_0002 $N_0003 DC 0 AC 0
+PWL 700n 0 800n .19639468 900n -.0911127 1000n -.9962207 1100n .4
986145 1200n
+  -1.1072326 1300n -.6822844 1400n 0 1000000n 0
V_V3          $N_0003 $N_0004 DC 0 AC 0
+PWL 1200n 0 1300n -1.2090425 1400n -.3849866 1500n -.2828022 1600
n -.5988249
+  1700n .28696968 1800n .26043382 1900n -.1844697 2000n 0 1000000
0n 0
E_E2          $N_0005 0 POLY(1) $N_0001 0 0.0 20n
R_R1          0 $N_0005  1T
V_V4          $N_0004 $N_0006 DC 0 AC 0
+PWL 1900n 0 2000n 1.33406586 2100n .4709716 2200n -1.3384583 2300
n .31109804
+  2400n -.3693647 2500n -.1817947 2600n -.2328334 2700n 0 1000000
0n 0
V_V5          $N_0006 0 DC 0 AC 0
+PWL 2600n 0 2700n .96459691 2800n 1.20224259 2900n -1.476755 3000
n -1.7641554
+  3100n -.3685622 3200n -1.0082046 3300n .9962207 3400n 0 1000000
00n 0
```

Figure 7-2 Netlist and Time Distributions

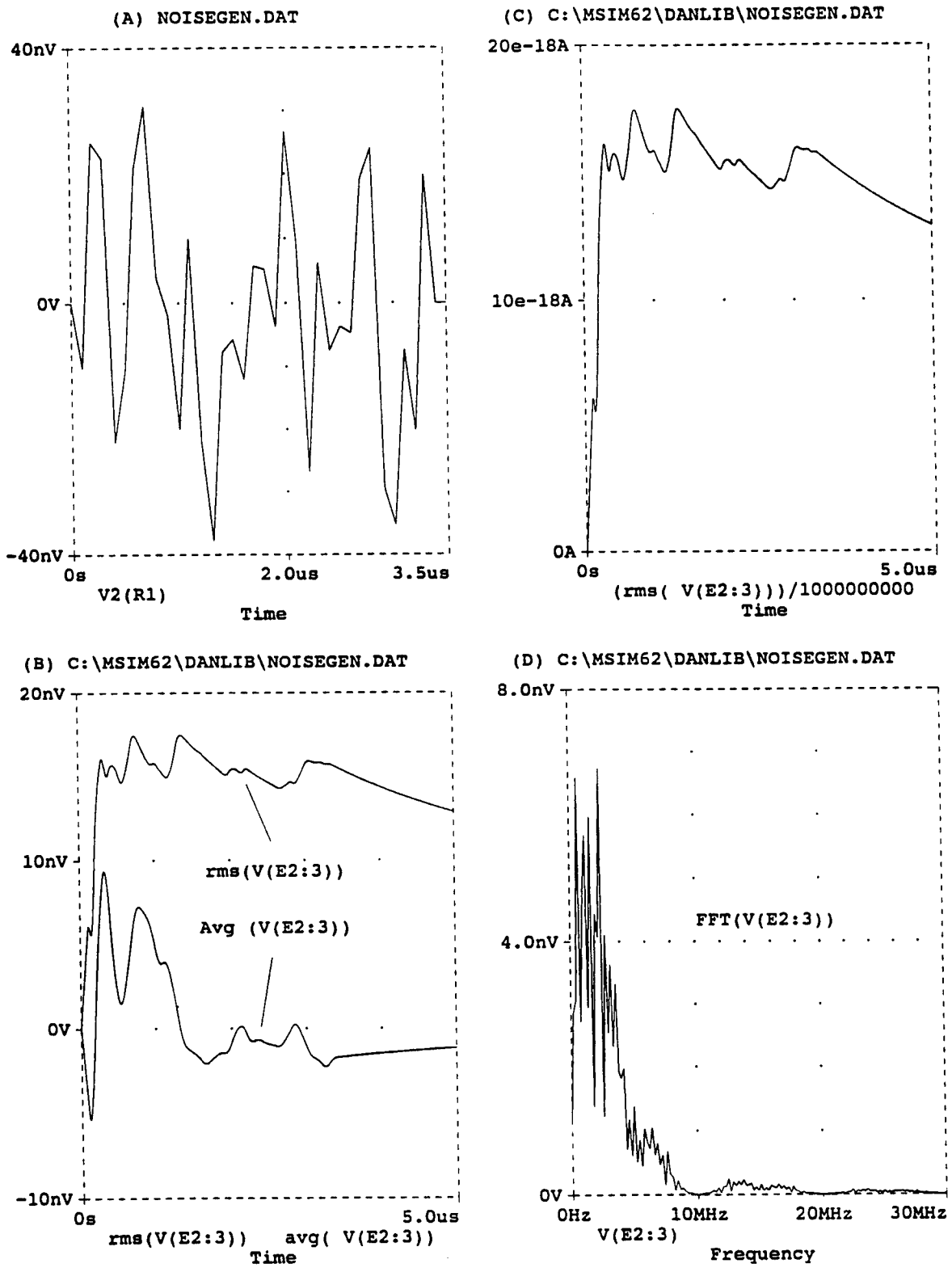


Figure 7-3 Open Circuit Responses to Gaussian Inputs

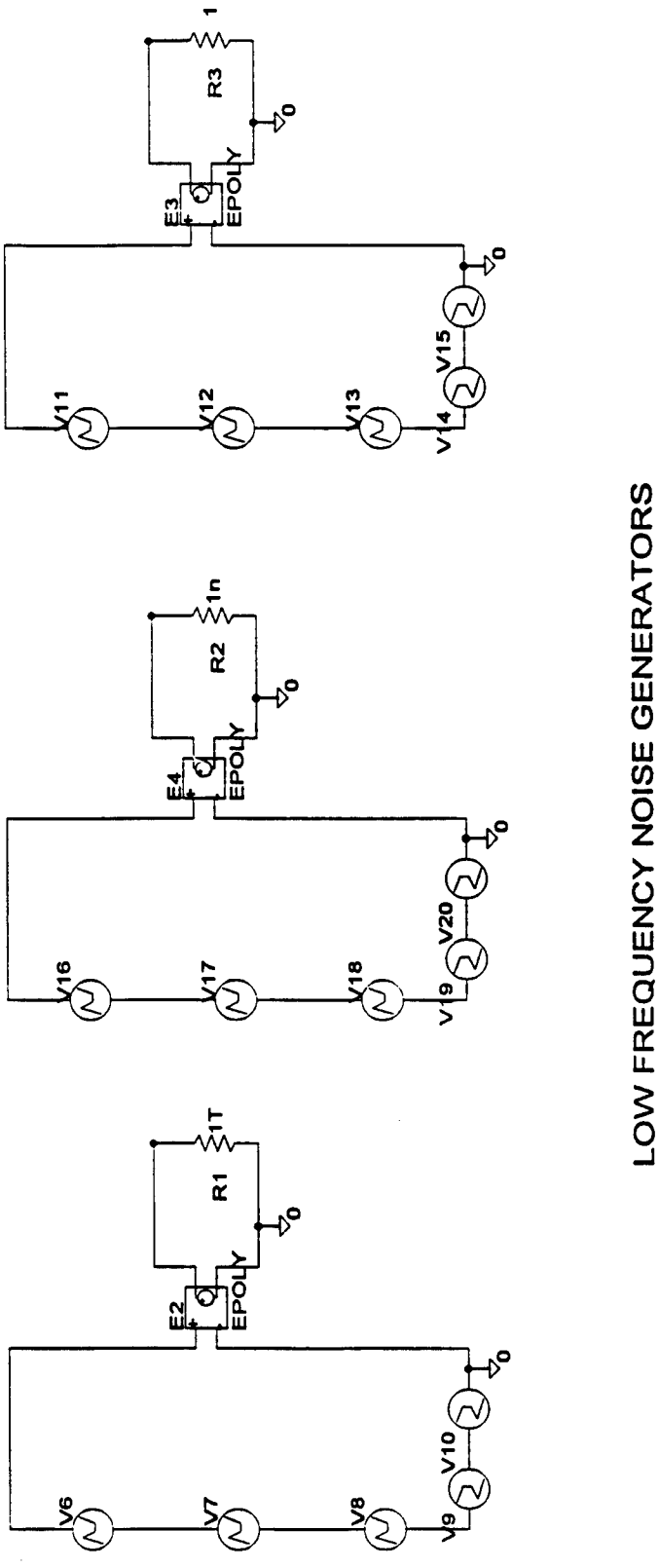


Figure 7-4 Iterated Noise Sources

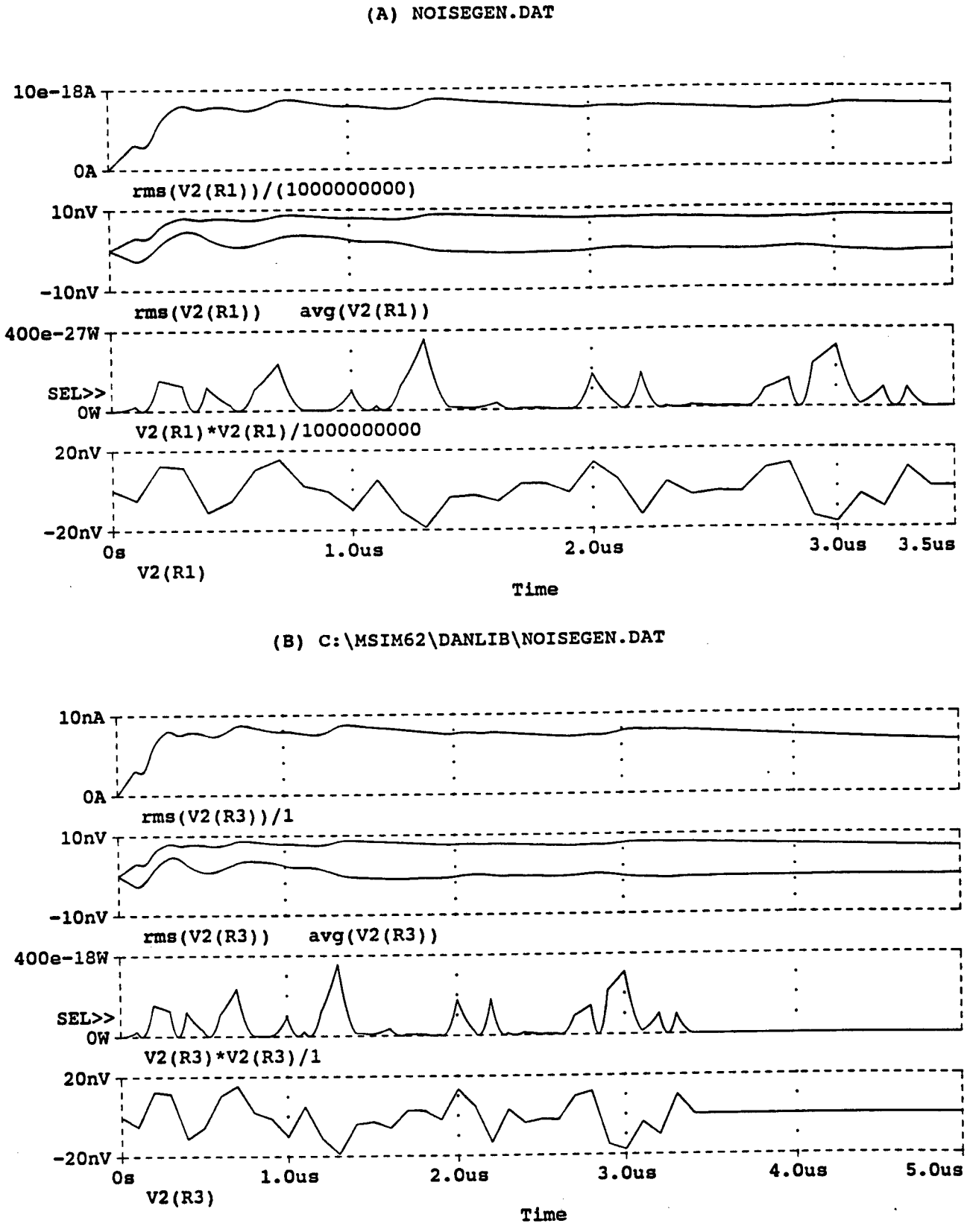
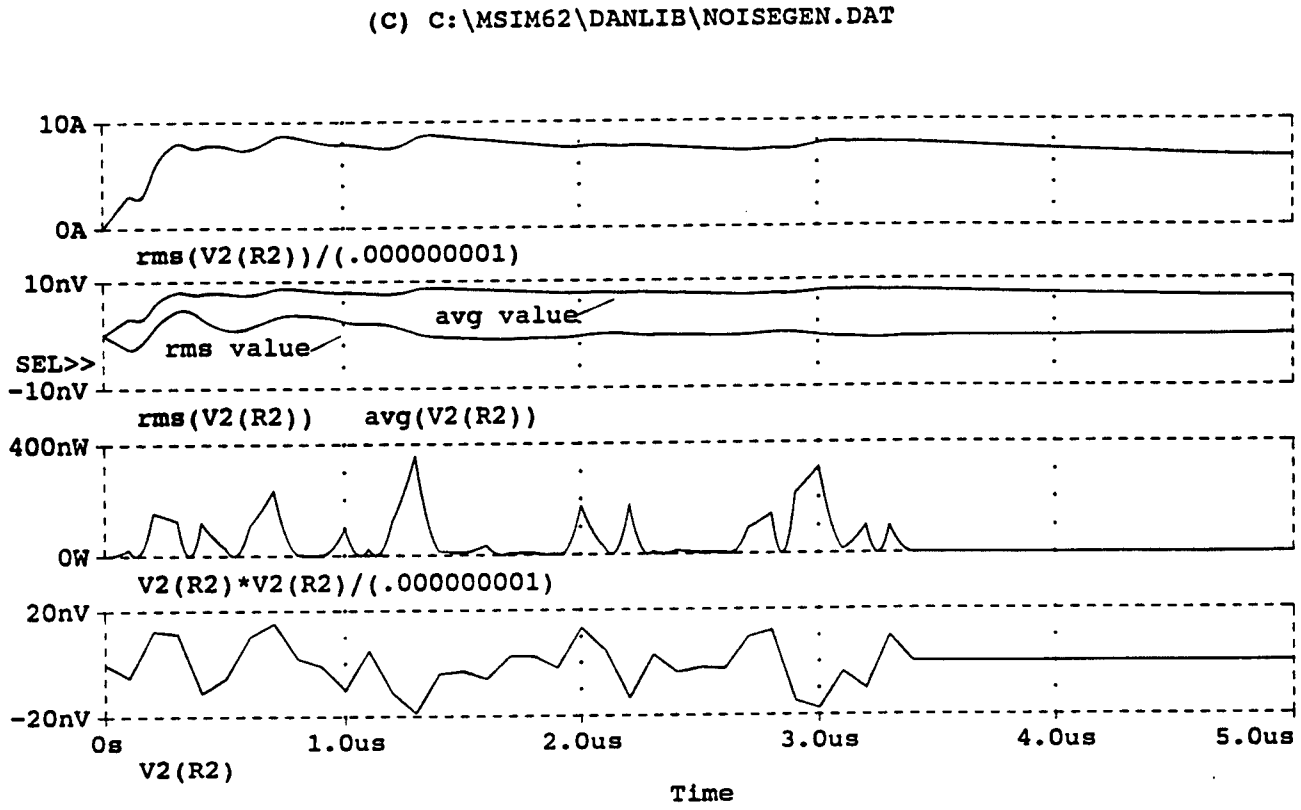


Figure 7-5 Related Noise Responses



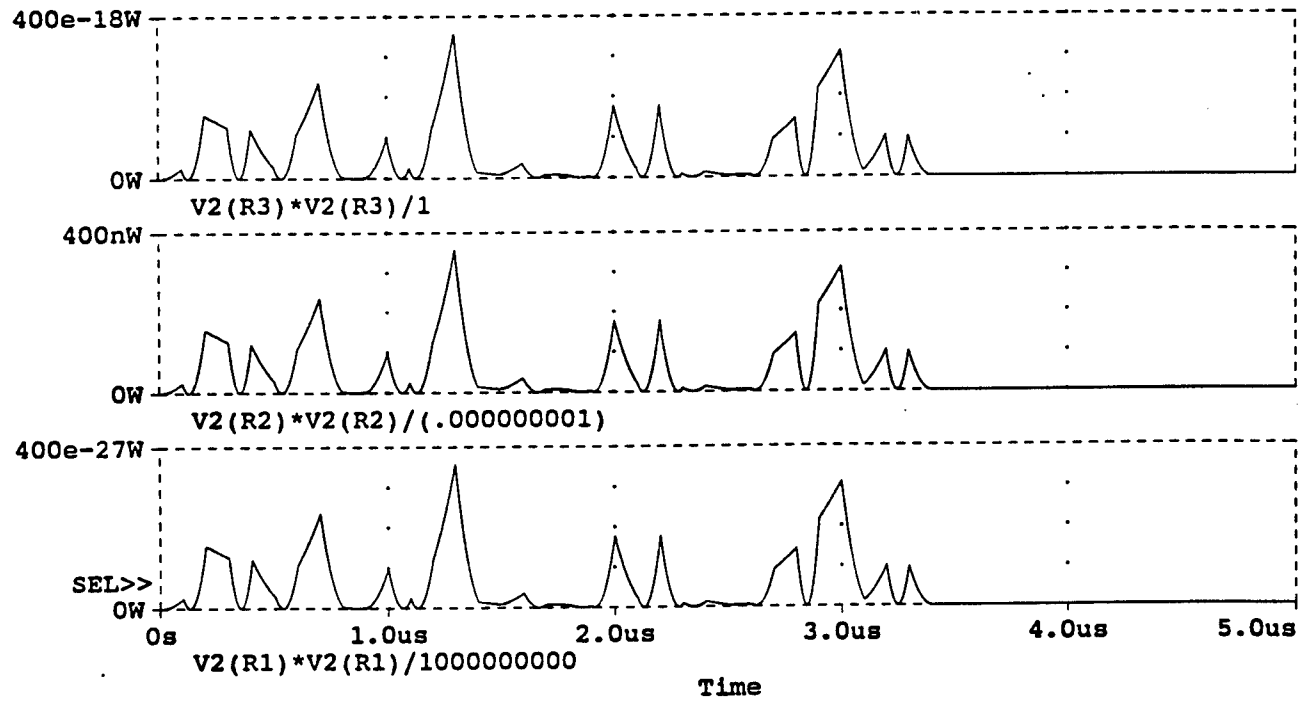


Figure 7-6 More Related Responses

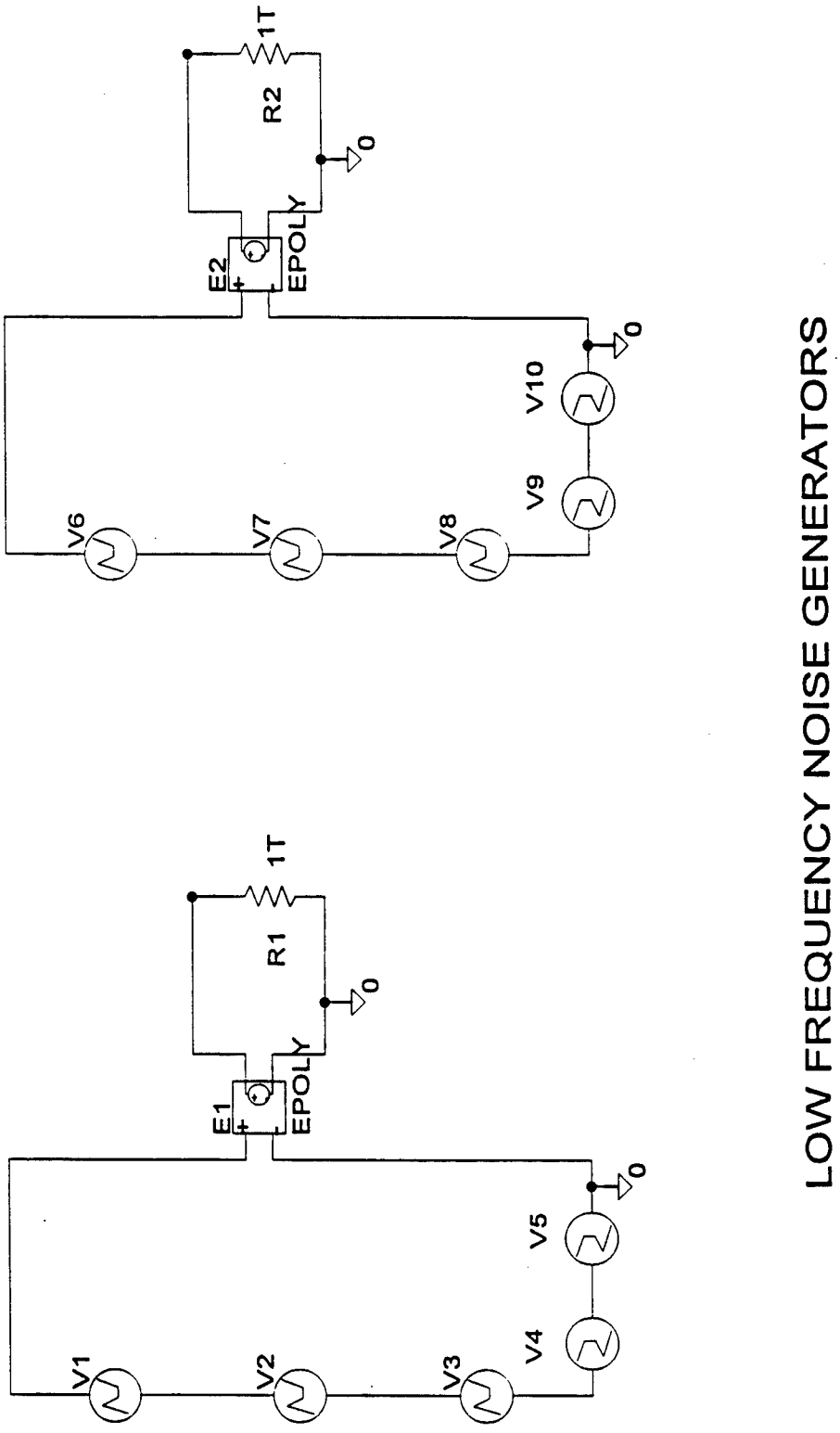


Figure 7-7 Combining Independent Noise Sources

```
* Schematics Netlist *
* Multiple Noise Generators From Randomized PWL Sources Into VCVS
E-Device
* Created by DJKenneally 10-04-95


V_V1          $N_0001 $N_0002 DC 0 AC 0
+PWL 0 0 100n -.5059494 200n 1.25103432 300n 1.12552402 400n -1.10
173531 500n
+  -.5376212 600n 1.04056649 700n 1.53779272 800n .34721034 900n -
.3457178
V_V2          $N_0002 $N_0003 DC 0 AC 0
+PWL 1000n 1.08154726 1100n .19639468 1200n -.0911127 1300n -.9962
207 1400n
+  .4986145 1500n -1.1072326 1600n -.6822844 1700n -.7236932 1800n
 1.652121590
V_V3          $N_0003 $N_0004 DC 0 AC 0
+PWL 1900n .31232854 2000n -1.2090425 2100n -.3849866 2200n -.2828
022 2300n
+  -.5988249 2400n .28696968 2500n .26043382 2600n -.1844697 2700n
 .87739239
+  2800n .79259537
E_E1          $N_0005 0 POLY(1) $N_0001 0 0.0 10n
R_R1          0 $N_0005  1T
V_V4          $N_0004 $N_0006 DC 0 AC 0
+PWL 2900n -.2760077 3000n 1.33406586 3100n .4709716 3200n -1.3384
583 3300n
+  .31109804 3400n -.3693647 3500n -.1817947 3600n -.2328334 3700n
 1.5594066
+  3800n -1.3422033
V_V5          $N_0005 0 DC 0 AC 0
+PWL 3900n -1.4945704 4000n .96459691 4100n 1.20224259 4200n -1.47
6755 4300n
+  -1.7641554 4400n -.3685622 4500n -1.0082046 4600n .9962207 4700
n -.0651654
+  4800n .84267109
V_V6          $N_0007 $N_0008 DC 0 AC 0
+PWL 0 0 100n -.5059494 200n 1.25103432 300n 1.12552402 400n -1.10
173531 500n
+  -.5376212 600n 1.04056649 700n 1.53779272 800n 0 1000000n 0
V_V7          $N_0008 $N_0009 DC 0 AC 0
+PWL 700n 0 800n .19639468 900n -.0911127 1000n -.9962207 1100n .4
986145 1200n
+  -1.1072326 1300n -.6822844 1400n 0 1000000n 0
V_V8          $N_0009 $N_0010 DC 0 AC 0
+PWL 1200n 0 1300n -1.2090425 1400n -.3849866 1500n -.2828022 1600
n -.5988249
+  1700n .28696968 1800n .26043382 1900n -.1844697 2000n 0 1000000
0n 0
E_E2          $N_0011 0 POLY(1) $N_0007 0 0.0 20n
R_R2          0 $N_0011  1T
V_V9          $N_0010 $N_0012 DC 0 AC 0
+PWL 1900n 0 2000n 1.33406586 2100n .4709716 2200n -1.3384583 2300
n .31109804
+  2400n -.3693647 2500n -.1817947 2600n -.2328334 2700n 0 1000000
0n 0
V_V10          $N_0012 0 DC 0 AC 0
+PWL 2600n 0 2700n .96459691 2800n 1.20224259 2900n -1.476755 3000
n -1.7641554
+  3100n -.3685622 3200n -1.0082046 3300n .9962207 3400n 0 1000000
00n 0
```

Figure 7-8 Netlist and Time Distributions for Combination Sources

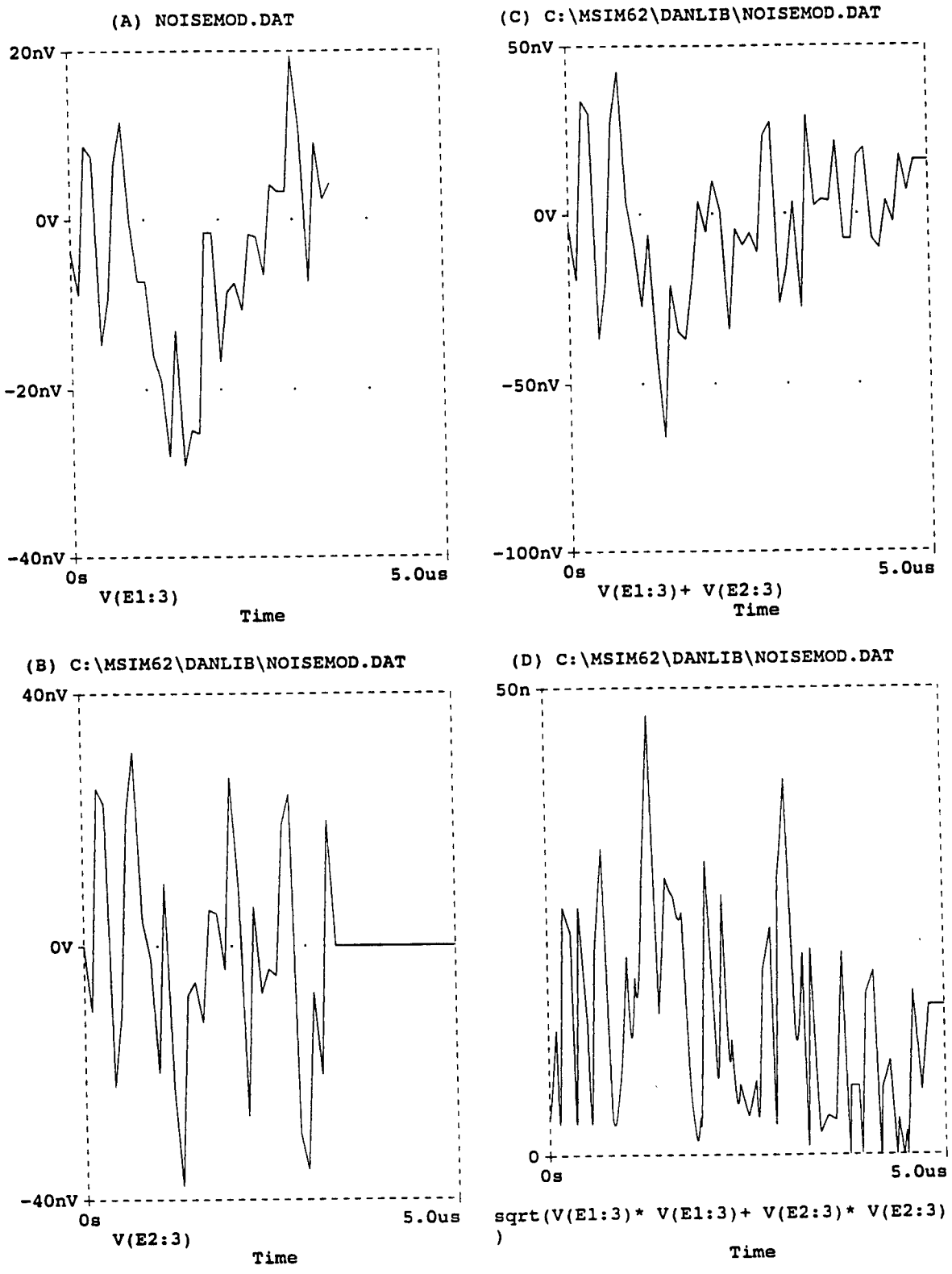


Figure 7-9 Responses of Combined Sources

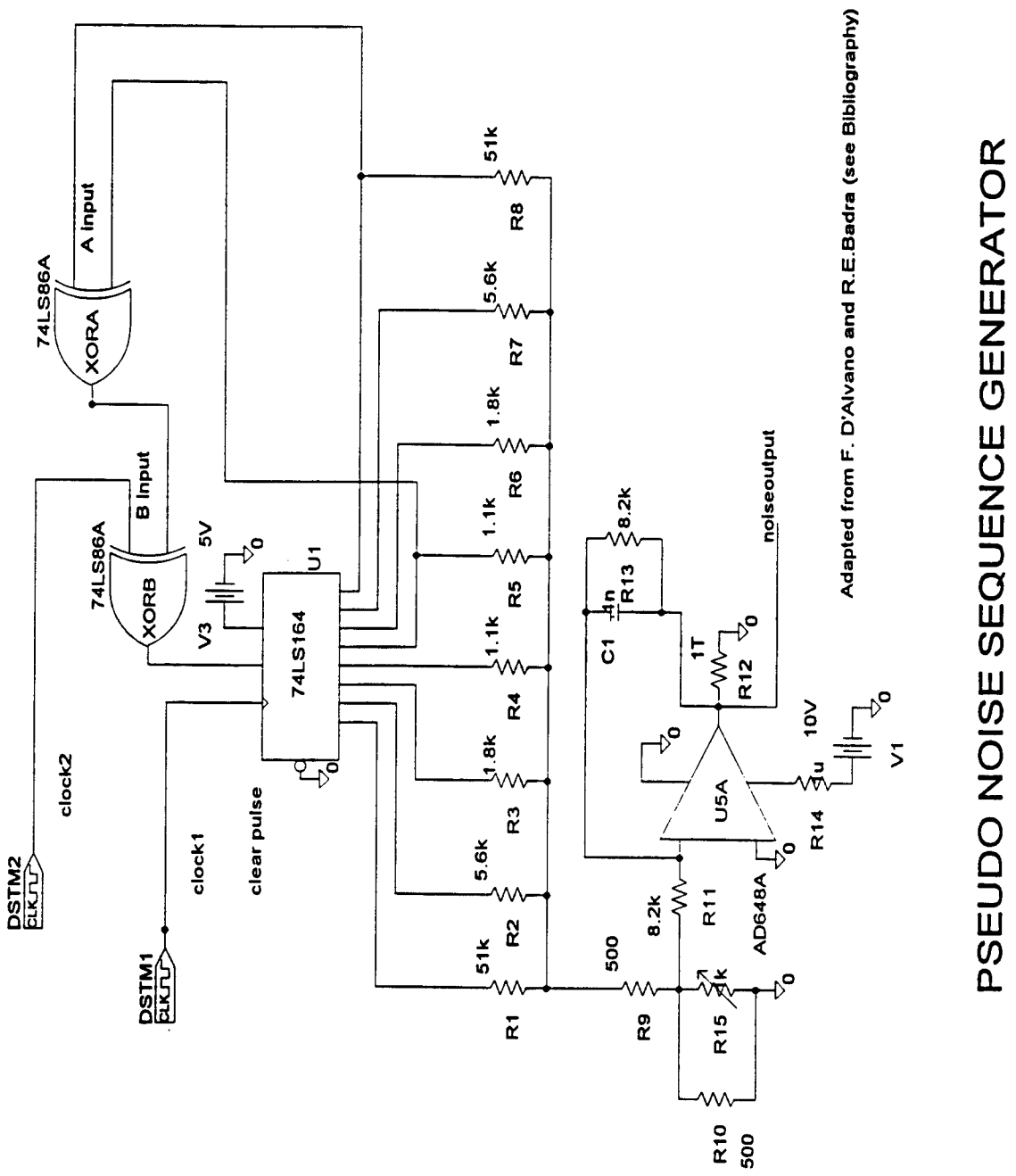


Figure 7-10 Pseudo Noise Generator with Shift Registers

```
* Schematics Netlist *
* PN Noise Generator(from D'Alvano&Badra)/DJK Modified 05-30-96*


X_U1          0 $N_0003 $N_0001 $N_0002 $N_0004 $N_0005 $N_0006 $N_
0007 $N_0008
+  $N_0009 $N_0010 $N_0011 $G_DPWR $G_DGND 74LS164 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_XORB          $N_0012 $N_0013 $N_0002 $G_DPWR $G_DGND 74LS86A PAR
AMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_XORA          $N_0007 $N_0004 $N_0012 $G_DPWR $G_DGND 74LS86A PAR
AMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R1          $N_0014 $N_0011  51k
R_R2          $N_0014 $N_0010  5.6k
R_R3          $N_0014 $N_0009  1.8k
R_R4          $N_0014 $N_0008  1.1k
R_R5          $N_0014 $N_0007  1.1k
R_R6          $N_0014 $N_0006  1.8k
R_R7          $N_0014 $N_0005  5.6k
R_R8          $N_0014 $N_0004  51k
R_R9          $N_0015 $N_0014  500
R_R10          0 $N_0015  500
R_R11          $N_0016 $N_0015  8.2k
X_U5A          0 $N_0016 $N_0017 0 output AD648A-X
R_R12          0 output  1T
V_V1          $N_0018 0 10V
U_DSTM1          STIM(1,1) $G_DPWR $G_DGND $N_0003 IO_STM IO_LEVEL=
0
+ 0 1
+ LABEL=START
+ +0 0
+ +.5uS 1
+ +.5uS goto START -1 times
U_DSTM2          STIM(1,1) $G_DPWR $G_DGND $N_0013 IO_STM IO_LEVEL=
0
+ 0 0
+ LABEL=START
+ +100ns 1
+ +.333uS 0
+ +.333uS goto START -1 times
R_R13          output $N_0016  8.2k
C_C1          output $N_0016  .1n
R_R14          $N_0018 $N_0017  1u
V_V3          $N_0001 0 5V
```

Figure 7-11 Netlist for Pseudo Noise Generator

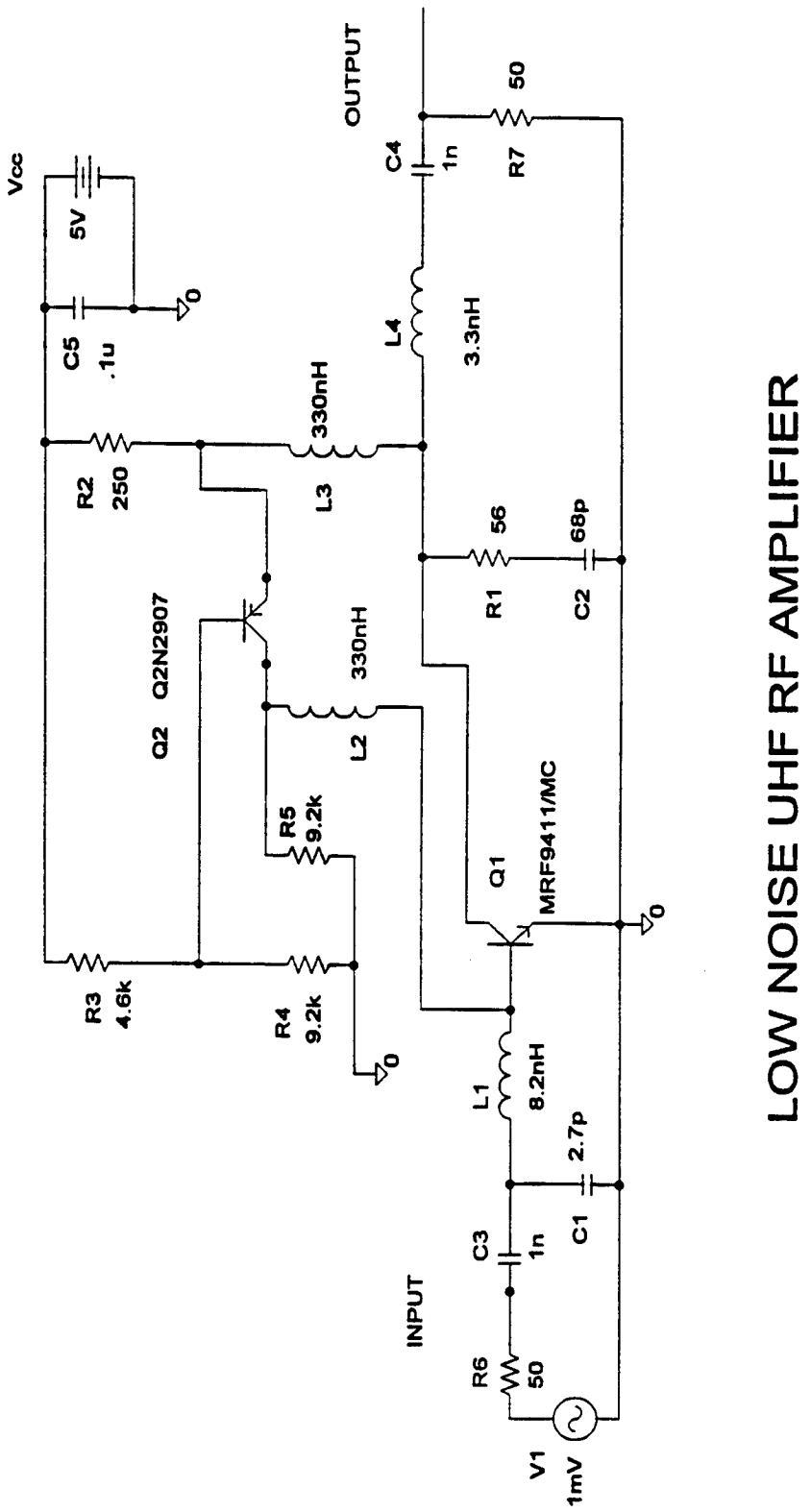


Figure 7-12 Low Noise, Wideband UHF RF Amplifier

```
* Schematics Netlist *
* LOW NOISE UHF RF AMPLIFIER (created 05-04-95/DJK)*
* Modified and Tuned Often*
* Design Settled (12-29-95)*

Q_Q1          $N_0002 $N_0001 0 MRF9411/MC
Q_Q2          $N_0004 $N_0003 $N_0005 Q2N2907
L_L1          $N_0006 $N_0001  8.2nH
L_L2          $N_0001 $N_0004  330nH
L_L3          $N_0002 $N_0005  330nH
L_L4          $N_0002 $N_0007  3.3nH
C_C1          0 $N_0006  2.7p
C_C2          0 $N_0008  68p
C_C3          INPUT $N_0006  1n
C_C4          $N_0007 OUTPUT  1n
C_C5          0 $N_0009  .1u
R_R1          $N_0008 $N_0002  56
R_R2          $N_0005 $N_0009  250
R_R3          $N_0003 $N_0009  4.6k
R_R4          0 $N_0003  9.2k
R_R5          0 $N_0004  9.2k
V_V1          $N_0010 0 DC 0V AC 1mV
R_R6          $N_0010 INPUT  50
R_R7          0 OUTPUT  50
V_V2          $N_0009 0 5V
```

Figure 7-13 Netlist for UHF Amplifier

Bipolar Transistor - Junction Voltage

Device data:

Vbe	base-emitter voltage @ Ib (device in saturation)
Vce	collector-emitter voltage (device in saturation)
Ib	base current for Vbe and Vce
%Ib	fraction of Ib (not a data sheet value)

Model parameters:

IS	saturation current
XTI	temperature coefficient for IS
EG	activation energy

This screen estimates the parameter IS from the saturation characteristics of the transistor. IS is a semiconductor junction parameter and should not be confused with the collector current in saturation. The data sheet will have values or curves for Vbe and Vce in a "forced beta" (where the ratio Ic/Ib is much lower than the normal current gain) or "saturated" condition. Enter values of Vbe and Vce for the same Ib.

The value of %Ib is a "fudge" value and is not critical. It factors how much of the base current will be shunted through the ideal diode of the Gummel-Poon transistor model. We have set it to a "normal" amount.

Obtaining an accurate value for IS is not critical, since other parameters will be set relative to IS, and only the ratio between values will be important. It is necessary, though, to not have a wildly inaccurate value. The last two model parameters, XTI and EG, may be changed. We have set them to be normal values for silicon transistors.

The display graphs for this screen are not too useful. However, they do let you know something is happening.

Figure 7-14 Device File for BJT's in UHF Amplifier

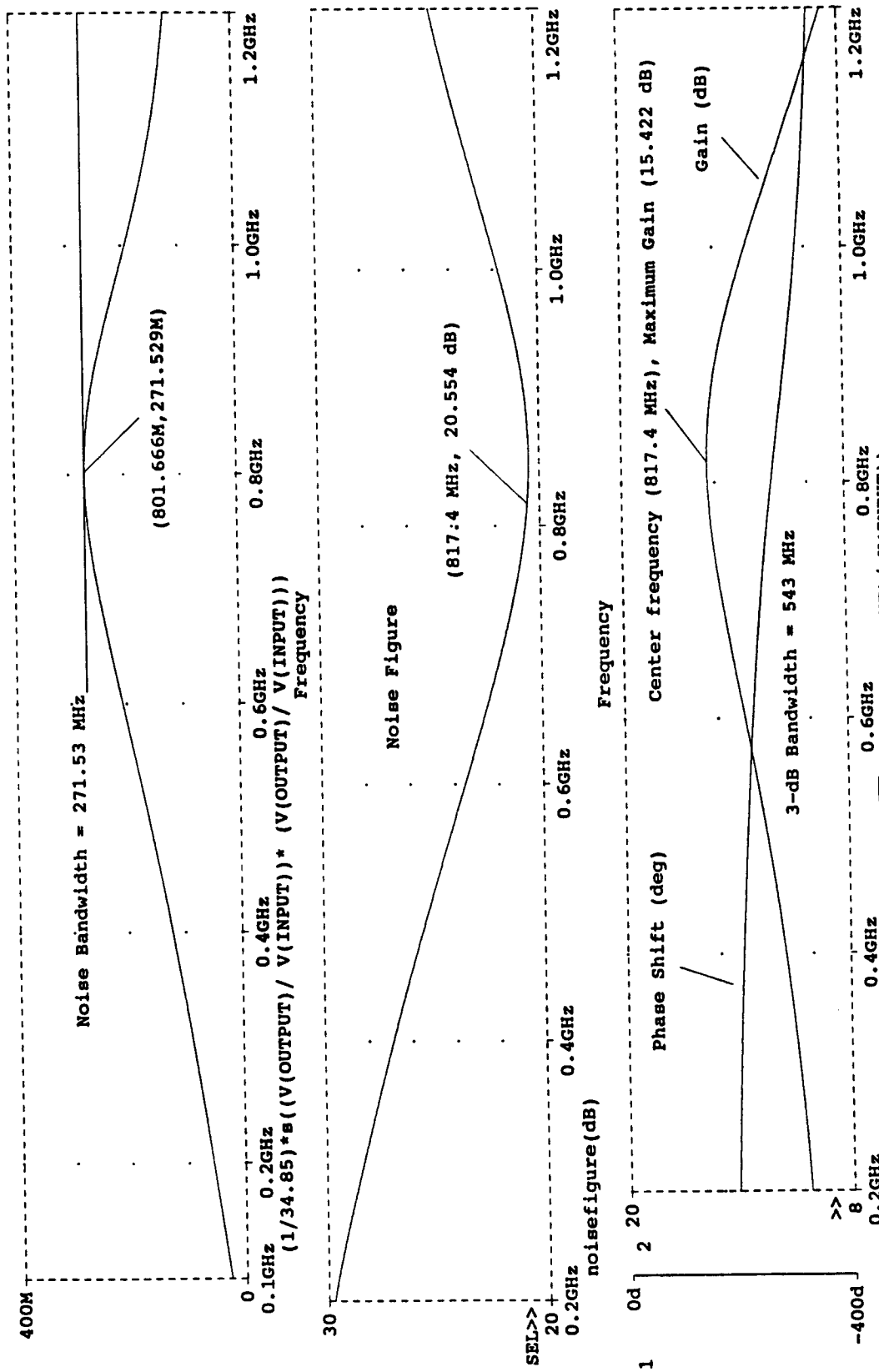


Figure 7-15 UHF Design Results

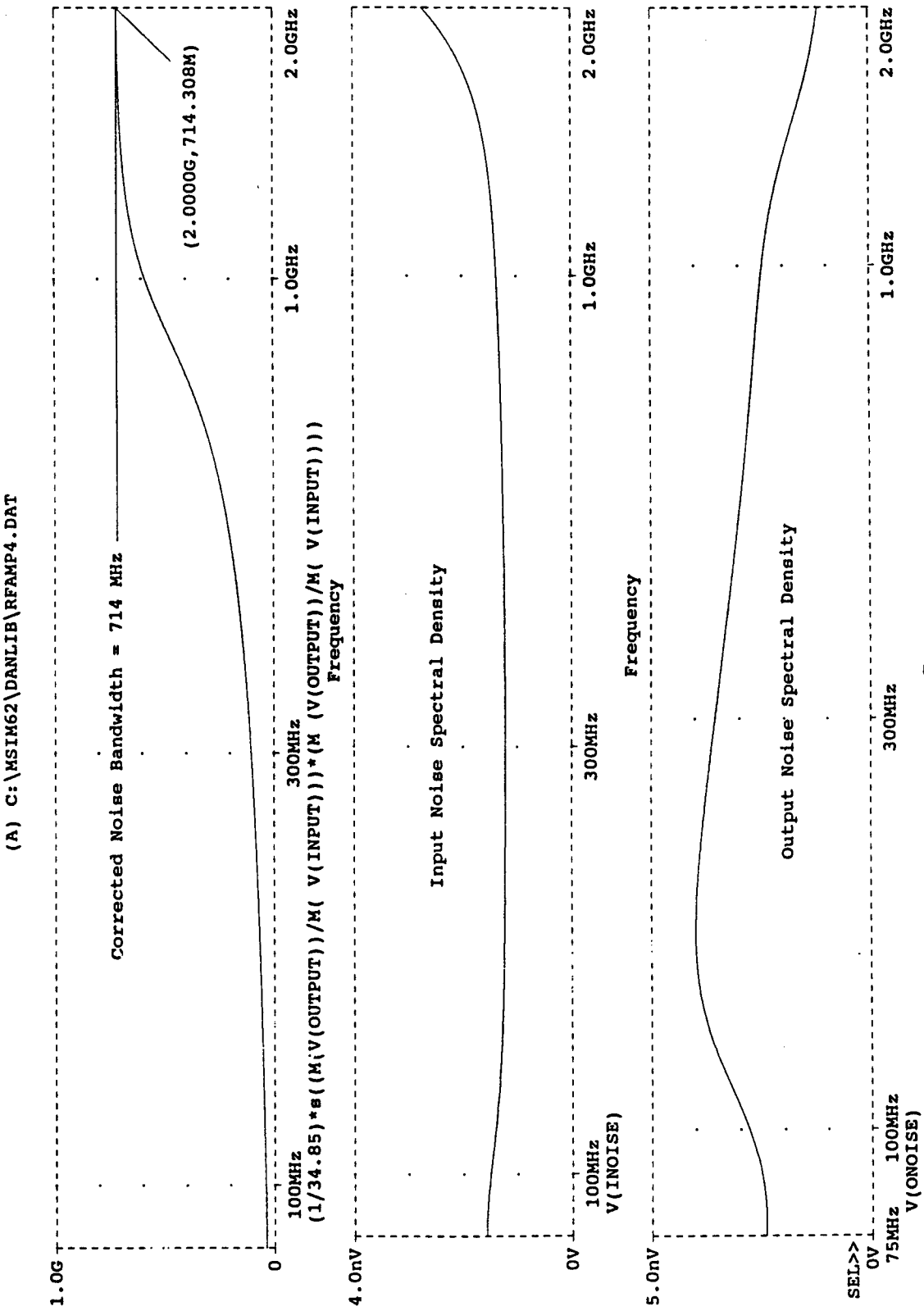


Figure 7-16 Corrected Noise Bandwidth Results

8. RF POWER COMBINERS

Power combiners are essential to doing EM susceptibility assessments either in the lab or by CAD modeling. The ideal combiner is a lossless, three port that additively combines a desired functional signal with an rf signal that is suspect of causing digital upset or linear distortion in the desired performance of the device or circuit under test. In other words, if port 3 of the three port combiner is taken as output port where combined signals are desired, and ports 1 and 2 are taken as input ports (for functional and rf signals), then over the band of interest: combiner input reflection coefficients s11, s22, and s33 should be zero; transmission coefficients s12 and s21 should be zero; and, transmission coefficients s13, s31, s23, and s32 should be ≥ 1.0. In other words, this ideal prescription requires: ports 1 and 2 to be matched to their respective sources; zero cross coupling between ports 1 and 2; and, unity coupling (or transmission gain) from ports 1 and 2, respectively, to output port 3.

For some time, OpAmp's (OA's) have been of considerable interest to designers of signal and rf combiners for EM assessments. Recently, attention has focused on using current mode feedback instead of the conventional voltage feedback in these OpAmp's. The rationale is that voltage mode feedback in conventional OpAmp's is more prone to parasitic capacitative effects between output and input nodes of high gain, inverting stages. This can be especially degrading at higher frequencies where the Miller effect kicks in to effectively multiply parasitic capacitative effects with stage gain. Current feedback using BJT's, on the other hand, offers faster switching times, wider bandwidths, and takes advantage of the reality that in most commercial (IC) circuits and board layouts, parasitic inductances are much less of a problem than stray capacitances.

Conventional voltage driven Opamp's usually have a high input impedance between their inverting and non-inverting pins and voltage feedback from the output pin to the inverting pin is easily accomplished. On the other hand, current feedback requires a low impedance path to at least one

input pin, preferably the inverting pin. The design challenge is to obtain a high impedance at the non-inverting input port of the OpAmp to accommodate the voltage signal drivers and, at the same time, obtain a low impedance at the inverting input port of the OpAmp to accommodate current feedback. With advanced manufacturing technologies for high speed, bipolar complementary device processing, a first practical solution was found and implemented by Elantec in 1986 [1]. This was soon followed by improved and diverse product lines of current feedback OpAmp's now commercially available from Comlinear Corporation, Linear Technologies, Burr-Brown, Harris, National Semiconductor, and others.

The conventional wisdom is to add an internal buffer at the non-inverting pin that provides a high input impedance to the external port, but now provides a low output impedance (internal) to the inverting pin. The voltage controlled, voltage source normally modeled (internally) between non-inverting and inverting pins of a conventional (voltage feedback) OpAmp, is now a current controlled, voltage source. The non-inverting, high impedance pin of the modified OpAmp can (still) be driven by a voltage source, but its inverting pin now has a low impedance path for the current feedback. An OpAmp using current feedback is really a transimpedance amplifier that senses signal current flowing from the internal input buffer to the external feedback load connected to the inverting pin. This buffer current controls the output voltage through the device transimpedance gain, and which generates an amplified voltage at the output port.

Many detailed device models of Opamp's use both current controlled and voltage controlled dependent sources. These dependent sources are used: to model the transfer function for the input buffer that is connected (device internal) between the non-inverting and inverting pins; to sense the current into the inverting node and set the transimpedance gain; to model dominant and higher order poles in the transimpedance gain; and to model parasitic admittances at input and output ports of the OpAmp. Small signal model parameters in most cases are extracted from rf measurements of steady

state responses for various input and output impedance loading. Parameter extraction involve extensive lab testing, and subsequent tweaking of computer simulated performance of candidate models to obtain a best performance fit with measured S-parameter data.

Detailed models of current feedback mode OpAmp's make use of PSPICE "E", "F", "G", and "H" controlled sources (i.e., voltage-controlled voltage source, current-controlled current source, voltage-controlled current source, and current-controlled current source, respectively). Using these sources in some models may cause a convergence problem. For example, using E and F sources with gains higher than 10, we found convergence problems that seemed to be associated with instability in the high frequency, high gain poles used to model the OpAmp transimpedance transfer gain. Limiting time step ceiling to 1 ps for frequency sweeps above 100 MHz seemed to help. Some other models and dc bias sources also seem to contribute to the instability. Using very small series resistors with some dc sources may allow a dc bias point convergence which, otherwise, might prevent the simulation from even running.

When using OpAmp's (and other models) from the parts library, it is sometimes not obvious which pins are the non-inverting and inverting pins, which are the bias supply pins, etc. An easy way to sort out pin assignments and polarities of devices on a schematic is to purposely remove strategic wires to suspect pins and simply run ERC (electrical rule check). ERC will then fail but will identify all the nodes with missing connections and provide an arrow "go to" pointer to the pin(s) in question.

In the following data figures, we show several configurations of rf signal combiners that make use of current feedback Opamp's and their simulated performance characteristics. Some designs are original: others are modified (and hopefully, improved) versions of rf combiners previously developed and tested elsewhere [2-3]. References and sources for imported original designs are indicated; if we missed proper credit, it is unintentional. In most figures, we make extensive use of EM macros developed and described elsewhere in this report without further comment.

Figures 8-1 and 8-2 show detailed OpAmp combiners, designed and modified from ones previously developed and tested by Rohrbaugh, et al. While the original combiner designs also used CLC 220 Opamp's manufactured by Comlinear Corporation, detailed OpAmp model parameters in the rf power combiner configurations were not available in the literature. RF combiner models shown here use the CLC 220 Opamp with a hybrid transistor tee for the input buffer. They are based on extracted device data provided by Comlinear [4], and modified here for the specific applications. Figure 8-3 show baseline, frequency domain results achieved. Baseline simulations were run with the functional source V5 removed by shorting it to ground. The amplitude of rf source V5 was then doubled to account for the effective voltage divider at pin 6. The gain curves shown are considerable improvements over previous work. While the pole at 158.7 MHz might be a problem, the roll off seems very consistent with known current feedback behavior. This OpAmp is "good" to 100 MHz. Figure 8-4 shows detail responses in the vicinity of the high band, high gain pole; figure 8-4 also shows the results of gain parameter variation with the feedback resistor R22VAL.

Figures 8-5 and 8-6 show the OpAmp results for transient behavior with both functional and rf sources present. Figure 8-7 shows the combined, small signal waveforms at the OpAmp output port (pin 9 of the Elantec EL2009/EL buffer). Figure 8-8 shows the combined, large signal waveforms. Figure 8-9 shows another OpAmp configuration to approximate an L-band, low pass filter that uses models of Burr-Brown OpAmp OPA 643. Figure 8-10 shows the modest results achieved. Figure 8-11 shows another configuration of an rf combiner using models of Elantec Opamp's EL2073/EL and Apex Microtechnology's OpAmp WB05. Figure 8-12 shows the baseline, frequency domain results. While the gain here is comparable to results in figure 8-3, this combiner exhibits more bandwidth and more phase shift. Figure 8-13 shows maximum values of combiner gain changes with feedback capacitance C1 (c1val). Figures 8-14 and 8-15 show the Elantec combiner used for transient testing with both rf and functional signals. Figure 8-16 shows the results obtained.

Beginning with figure 8-17, we now introduce a new approach to rf power combiners based on the contemporary Wilkinson power divider. Shown is a baseline Wilkinson power divider and its time domain performance out to 2 ns. Transmission line models T6 and T7 are lossless, each with characteristic impedances of 70.71 ohms, zero time delays, center frequencies of 6.0 GHz, and are 1/4 wavelengths long. Calibrations of power coupling at ports 1, 2, and 3 confirm expected Wilkinson behavior. Figure 8-18 shows a baseline Wilkinson power divider and also its frequency domain performance in the range from 1 GHz to 12 GHz. These calibration results shown are consistent with the time domain responses. Figure 8-19 shows a synthesized "dual" of a Wilkinson power divider - a Wilkinson rf power combiner. Port 1 is now a load port instead of an rf source port as in the Wilkinson power divider: ports 1 and 2 are now rf driven ports instead of load ports as in the Wilkinson power divider. Shown also in figure 8-19 is an extended time domain to 10 ns to allow time for the transient ripple to attenuate. This longer sweep allows better time resolution for macros to compute power. Figure 8-20 shows the frequency domain performance of the Wilkinson combiner out to 12 GHz.

[1] Lande, Tor Sverre and Toumazou, Chris, "Current Feedback Opamp's: A Blessing in Disguise?", IEEE Circuits and Devices Magazine, Vol. 10, No. 1, January 1991, pp. 34-37.

[2] Rohrbaugh, John and Pursley, Randall H., "X-Band T/R Module Conducted Interference Simulation and Measurements", Georgia Institute of Technology Final Report, Summer Research Program, Rome Laboratory, June 1992.

[3] Rohrbaugh, John and Levin, Rick J., "Conducted Interference Measurements and Simulation Results for a General Electric Soft Part Analogous Module (SPAM)", Georgia Institute of Technology Final Report, Summer Research Program, Rome Laboratory, July 1993.

[4] Corporate Author, "Fast Settling, Wideband Operational Amplifiers", Applications Note for CLC 220, Comlinear Corporation, Fort Collins, CO 80525, January 1993.

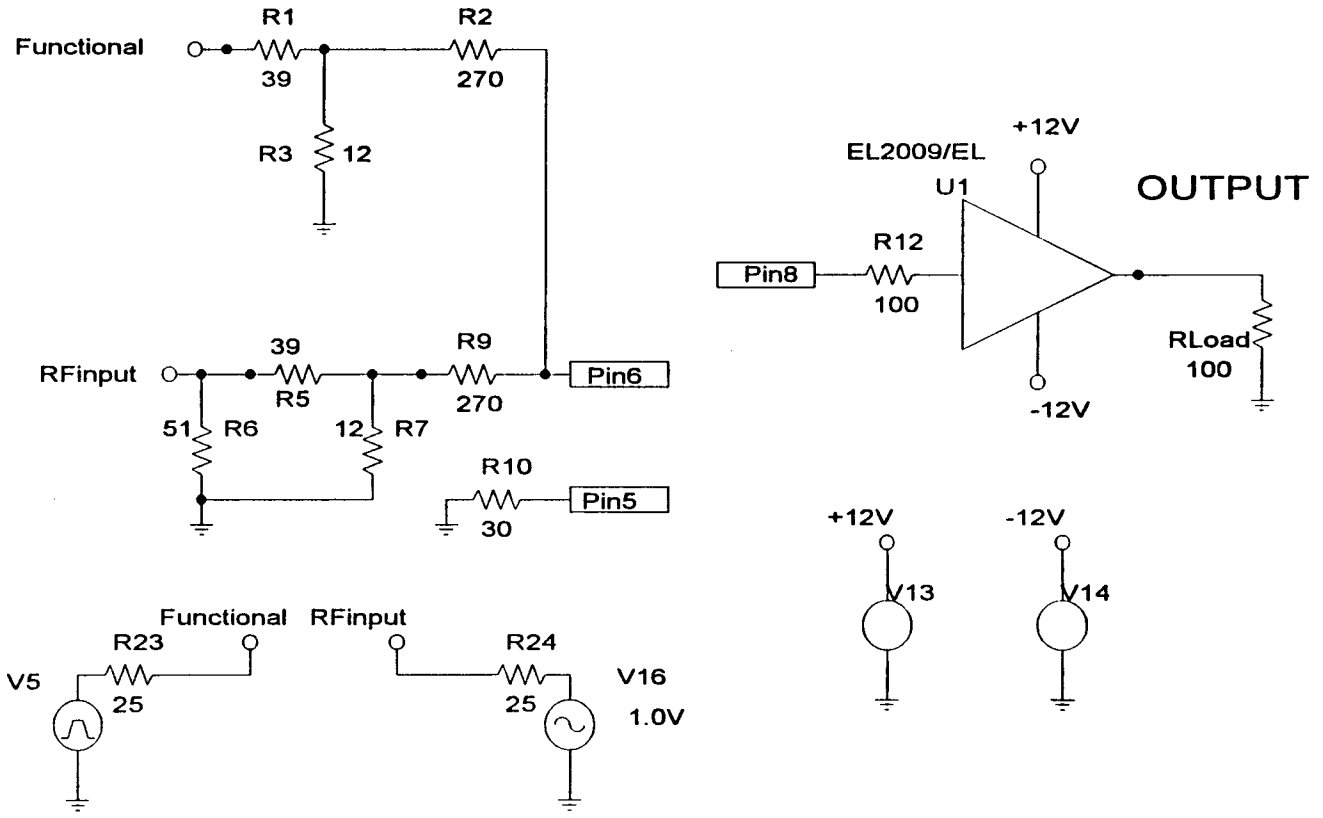


Figure 8-1 OpAmp Combiner (page 1 of 2)

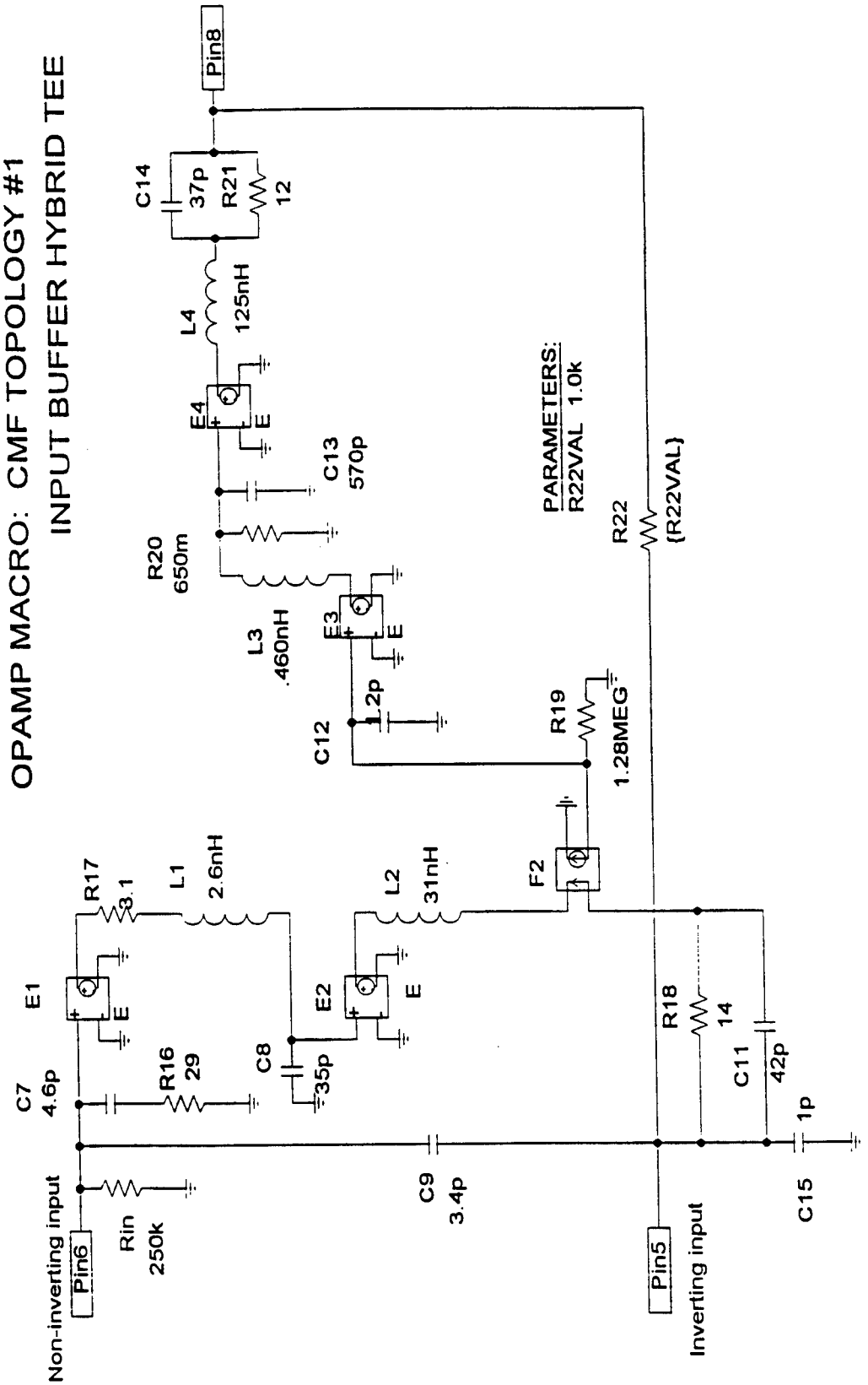


Figure 8-2 OpAmp Combiner (page 2 of 2)

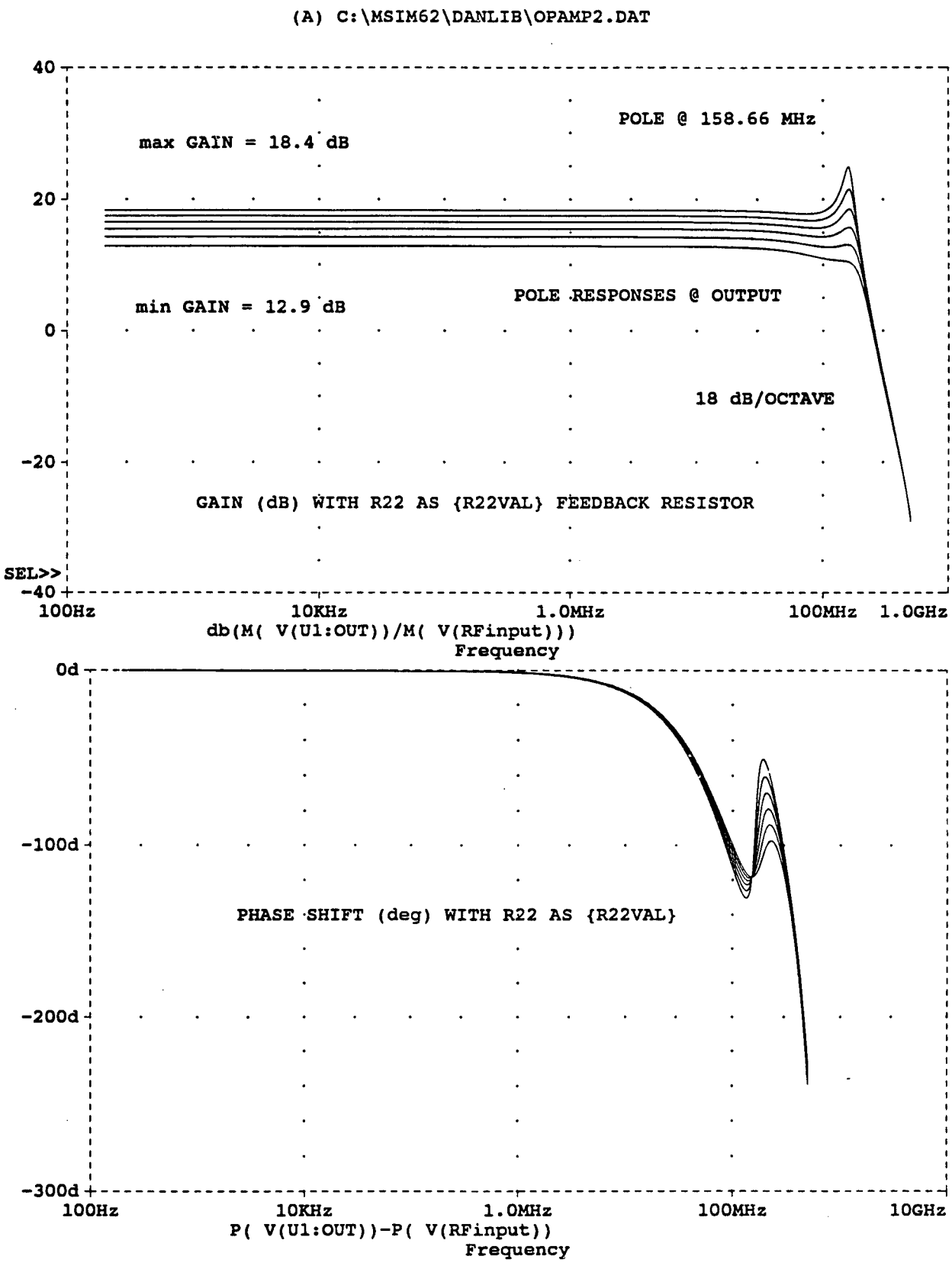


Figure 8-3 Baseline Frequency Responses

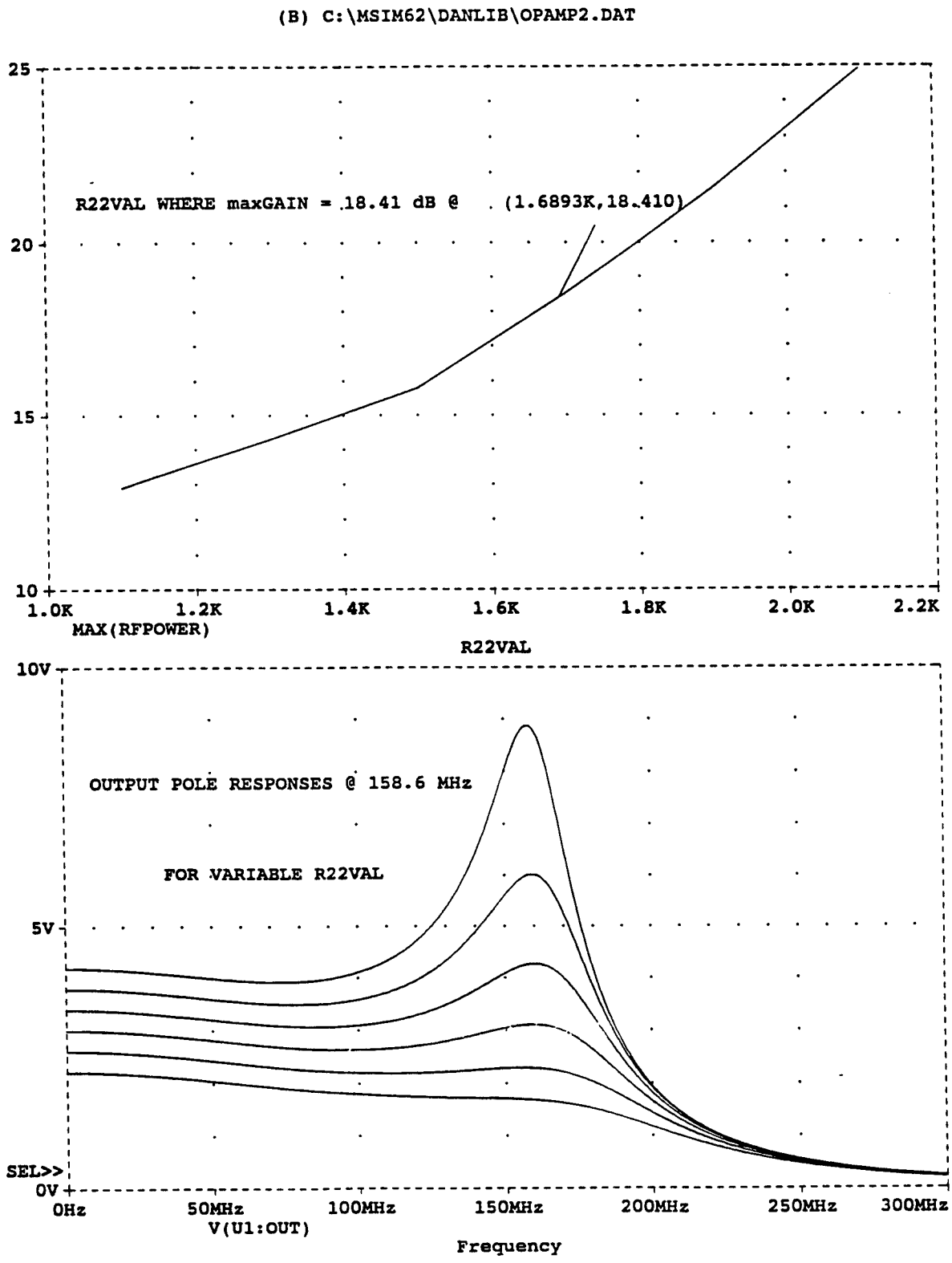


Figure 8-4 Feedback Parameter and Related Pole Responses

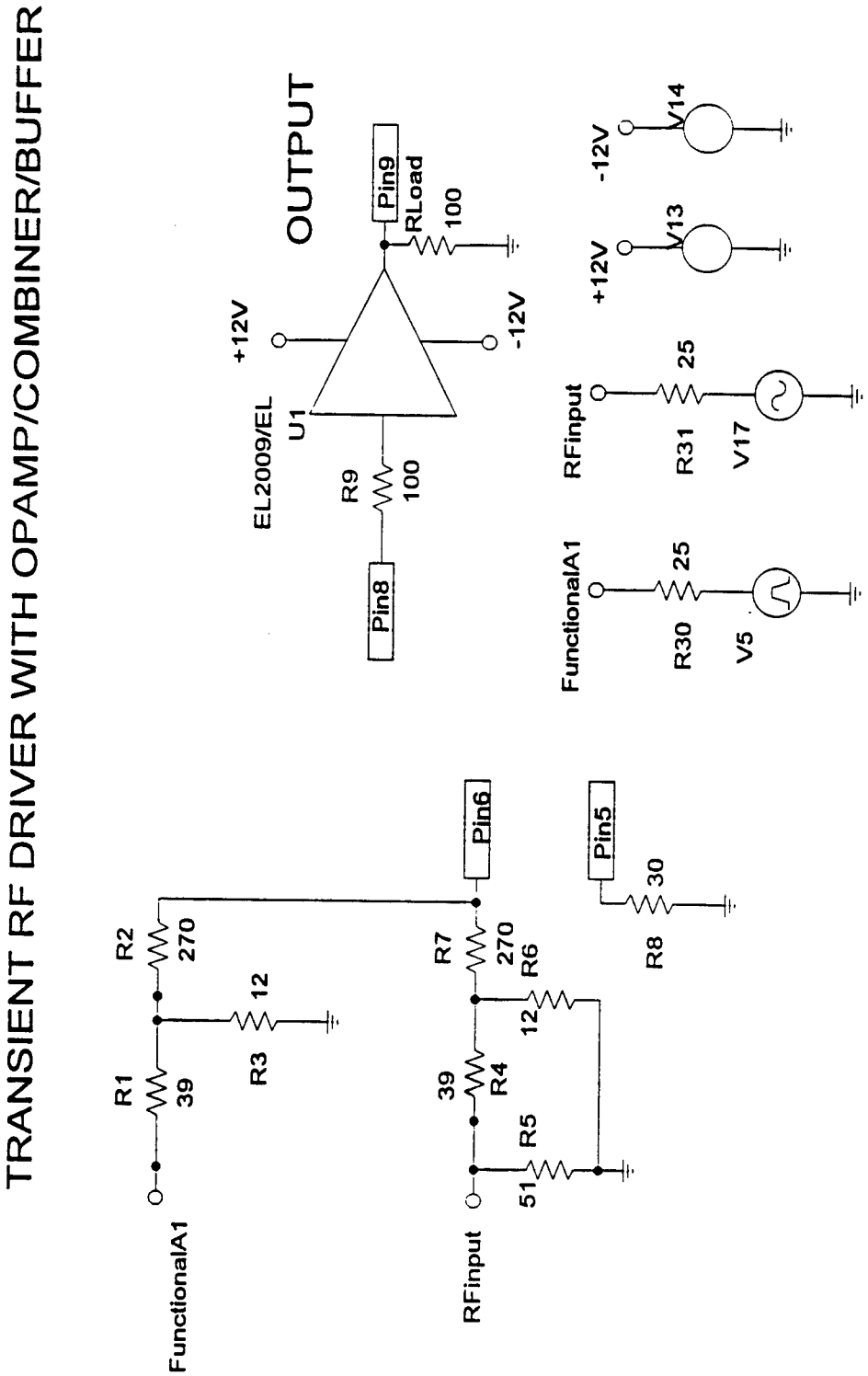


Figure 8-5 OpAmp Combiner with Functional and RF Sources (page 1 of 2)

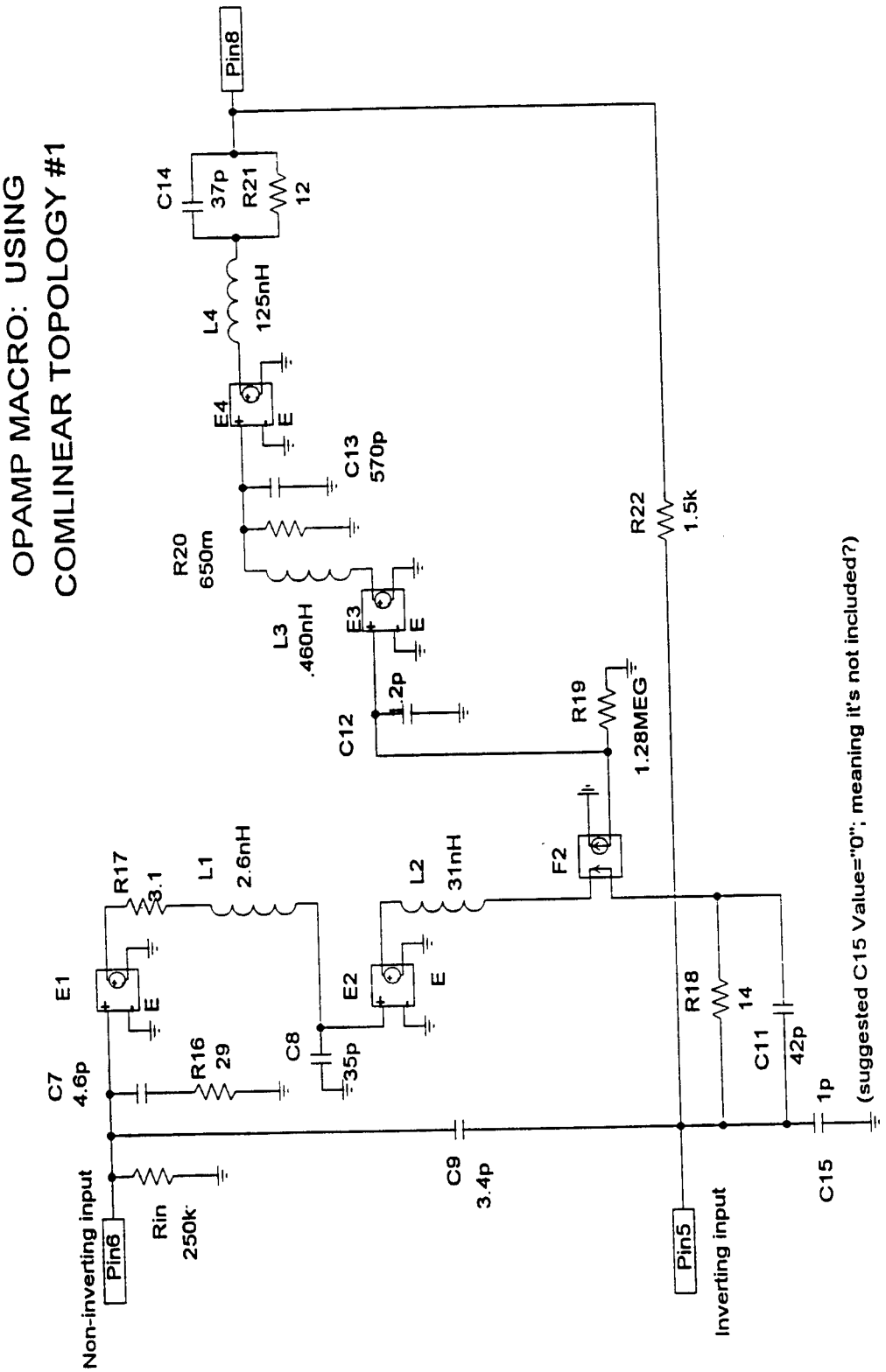


Figure 8-6 OpAmp Combiner with Functional and RF Sources (page 2 of 2)

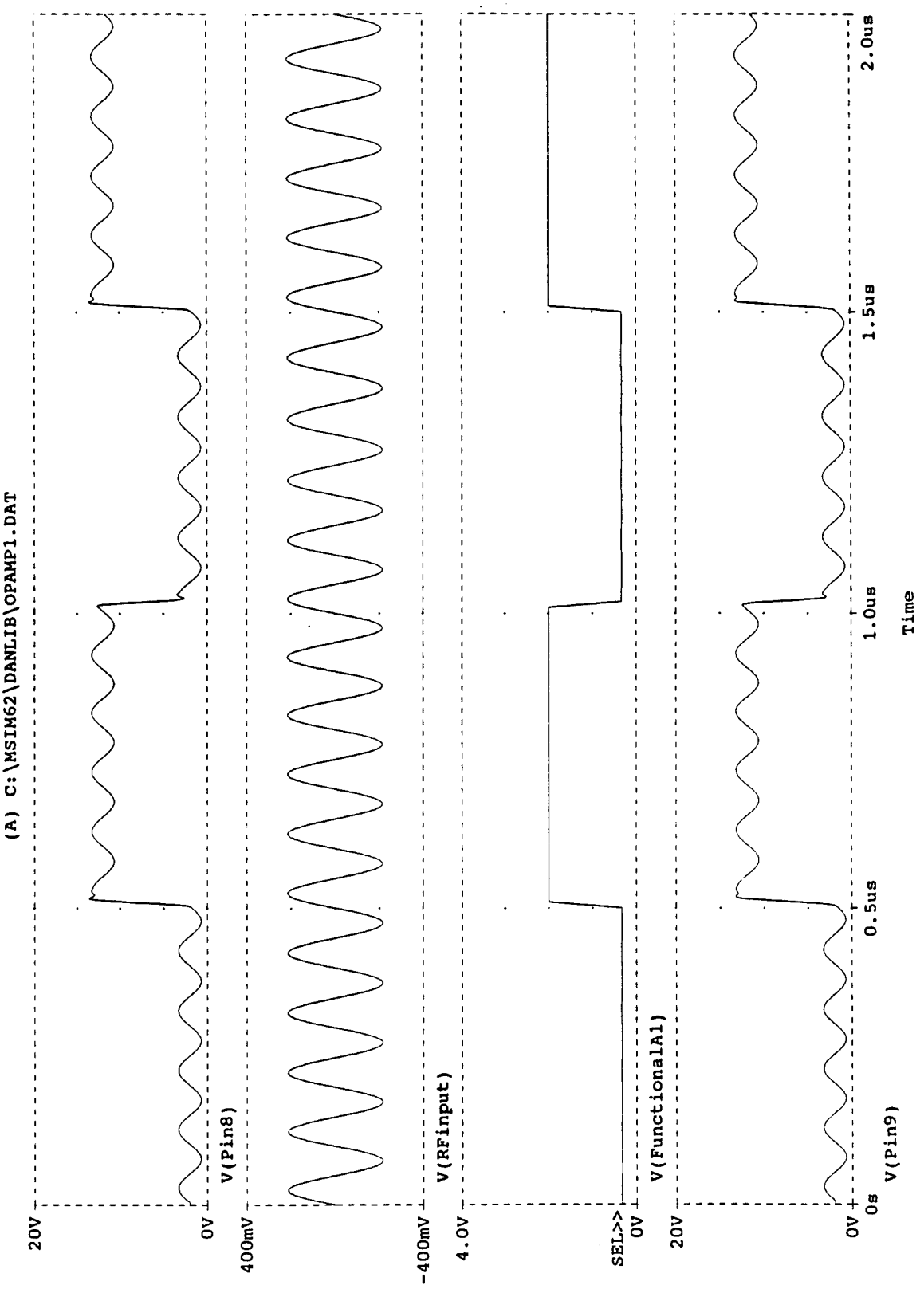


Figure 8-7 Small Signal Time Domain Responses

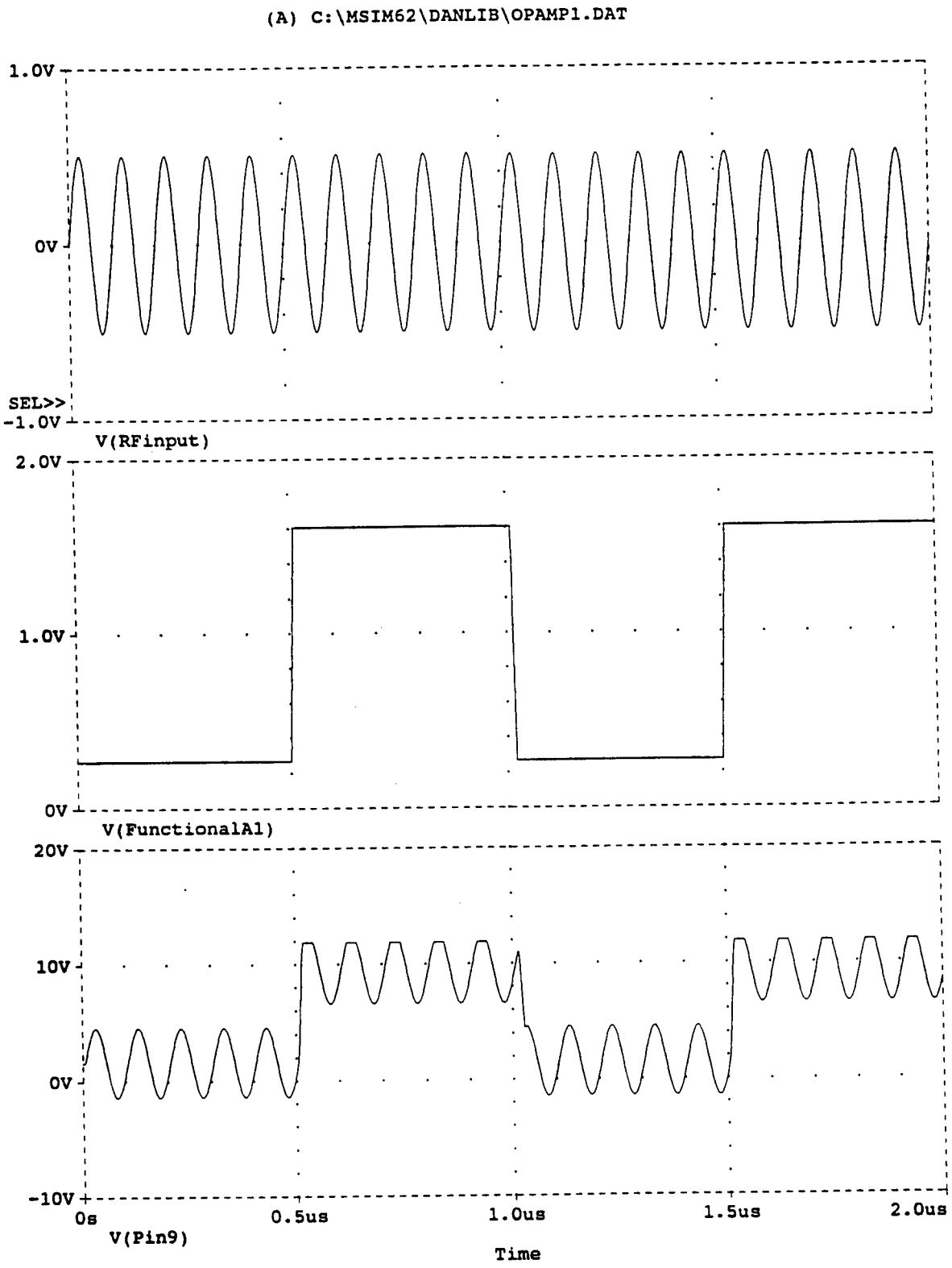


Figure 8-8. Large Signal Time Domain Responses

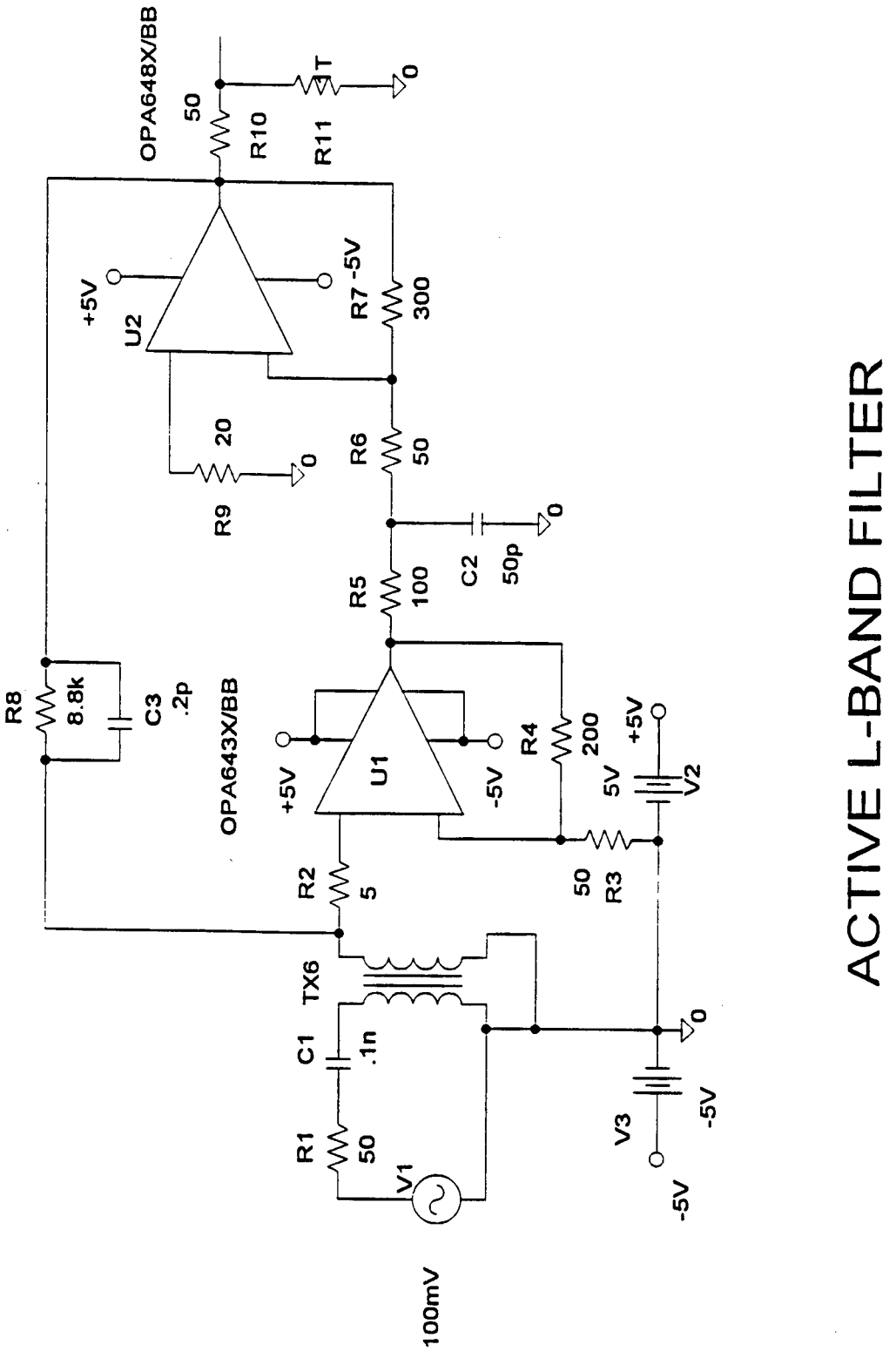


Figure 8-9 OpAmp L-Band Filter

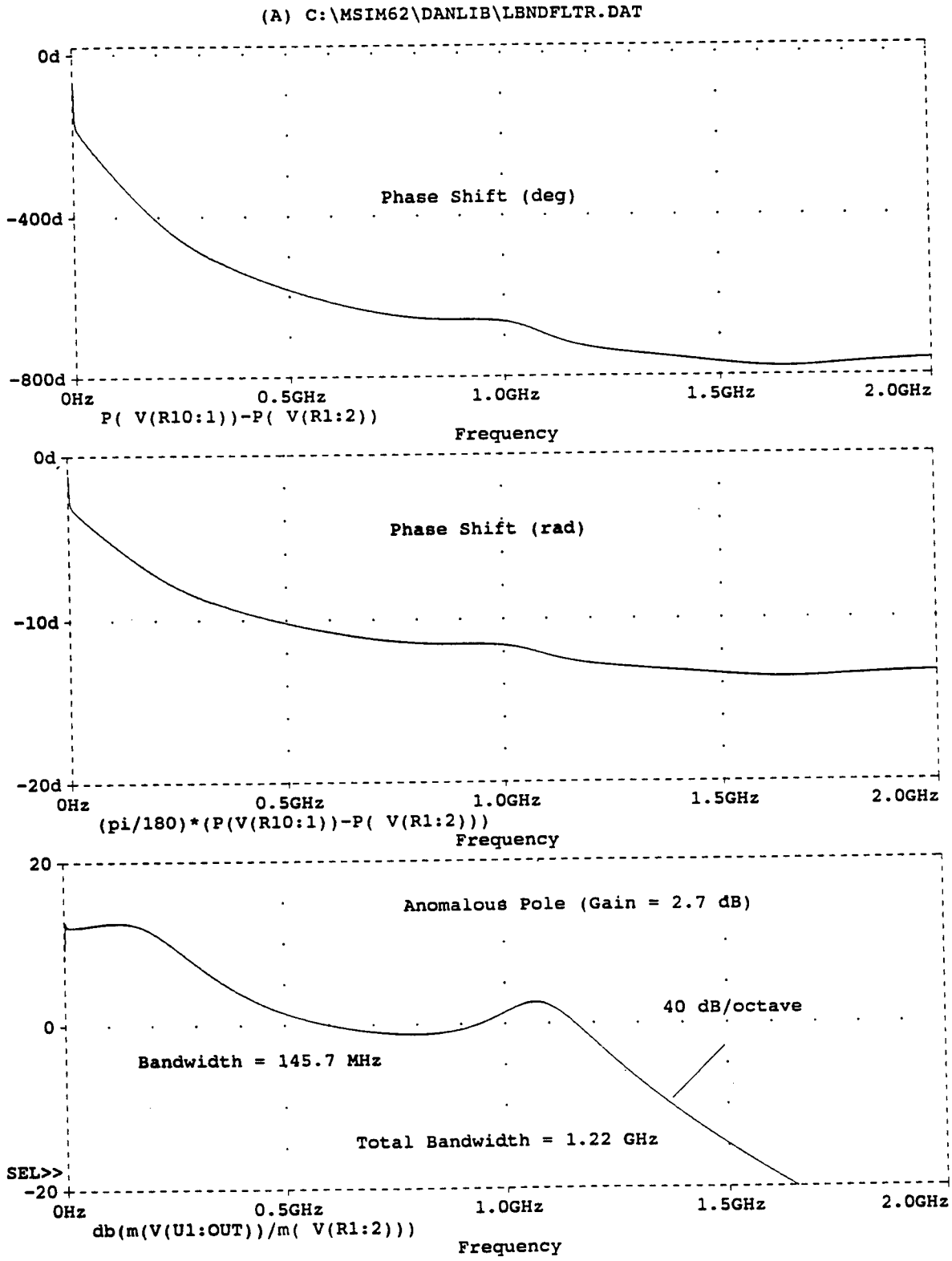


Figure 8-10 Filter Characteristics

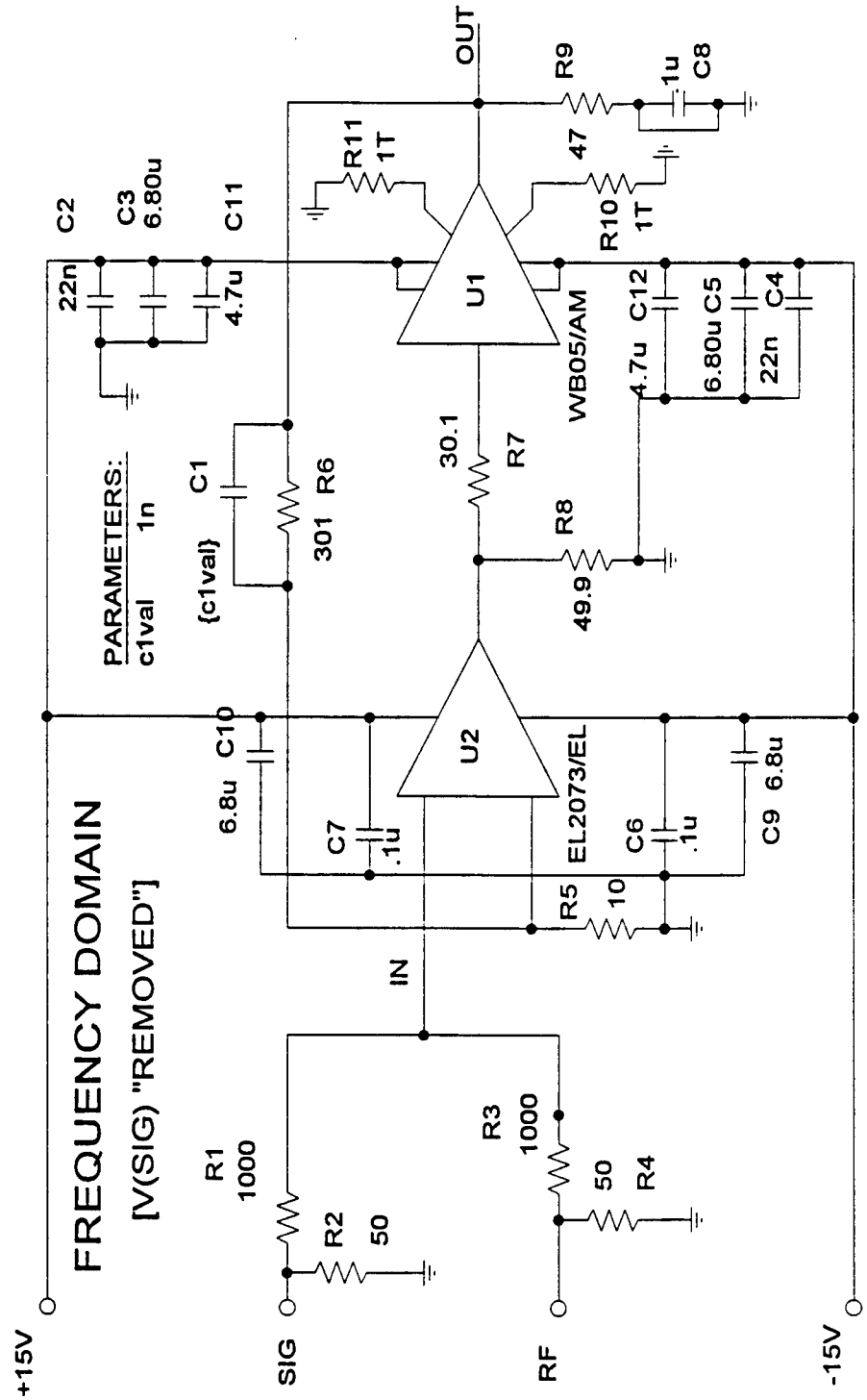


Figure 8-11 OpAmp Combiner using Elantec Devices

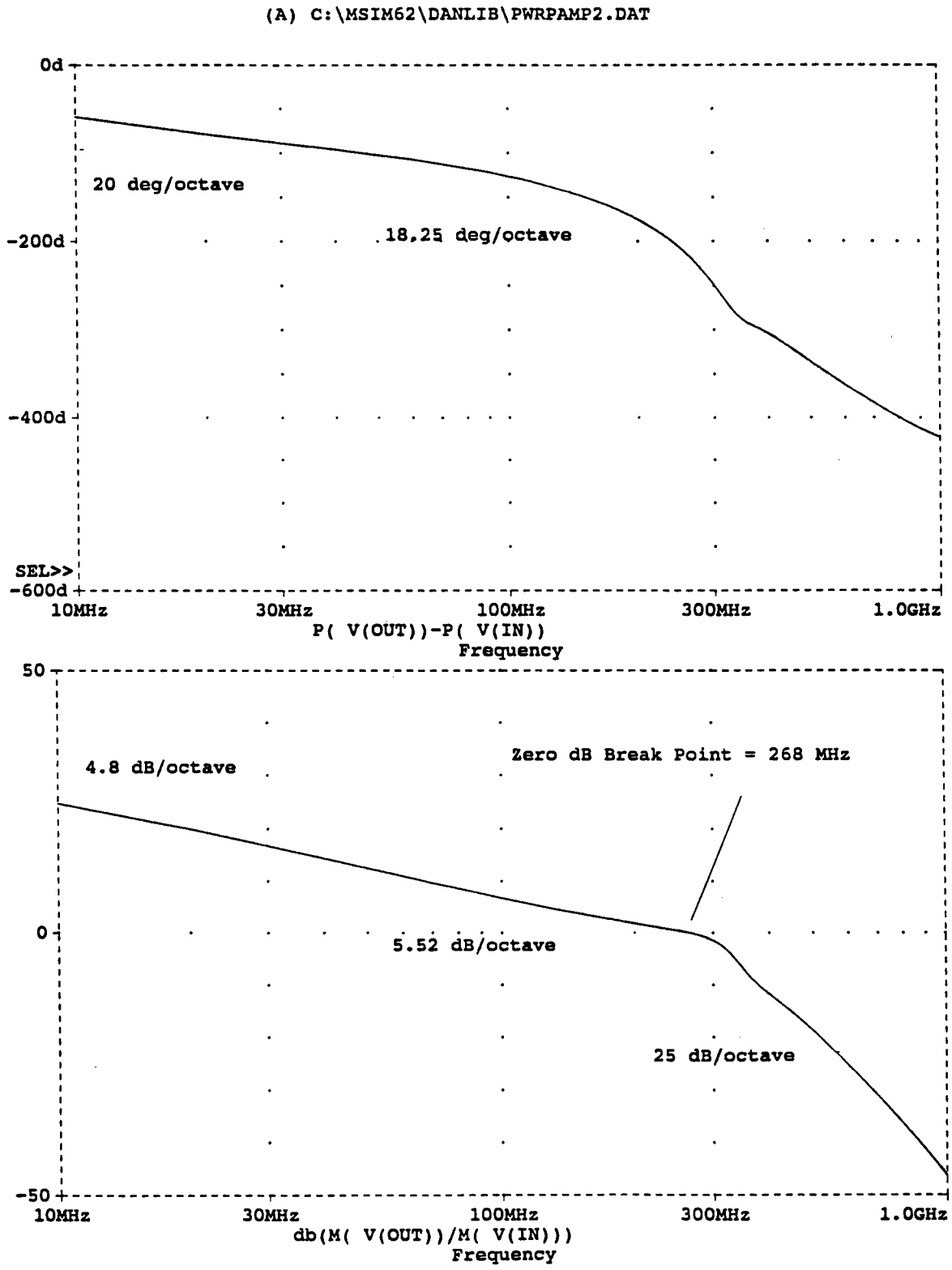


Figure 8-12 Frequency Domain Responses

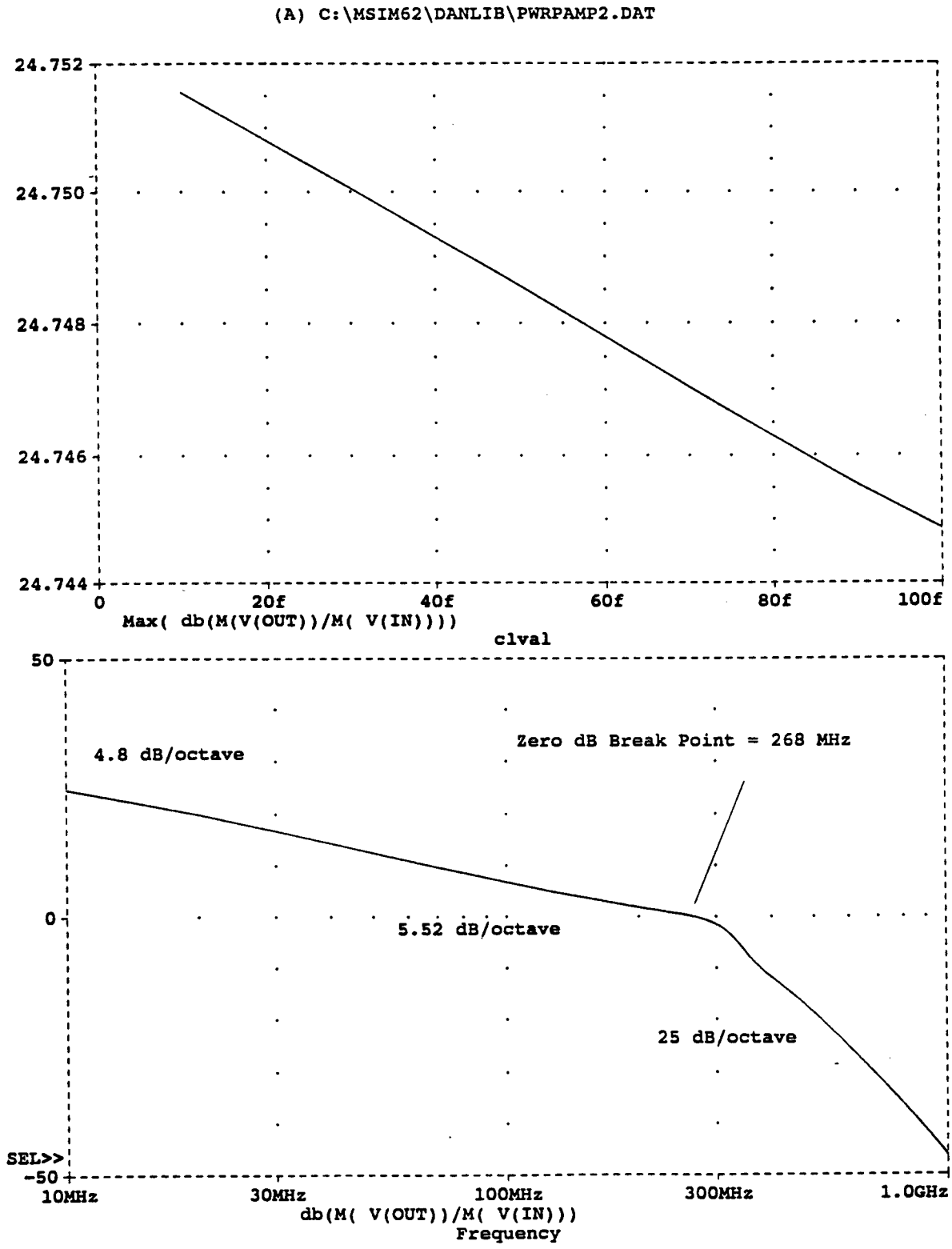


Figure 8-13 Gain Characteristics

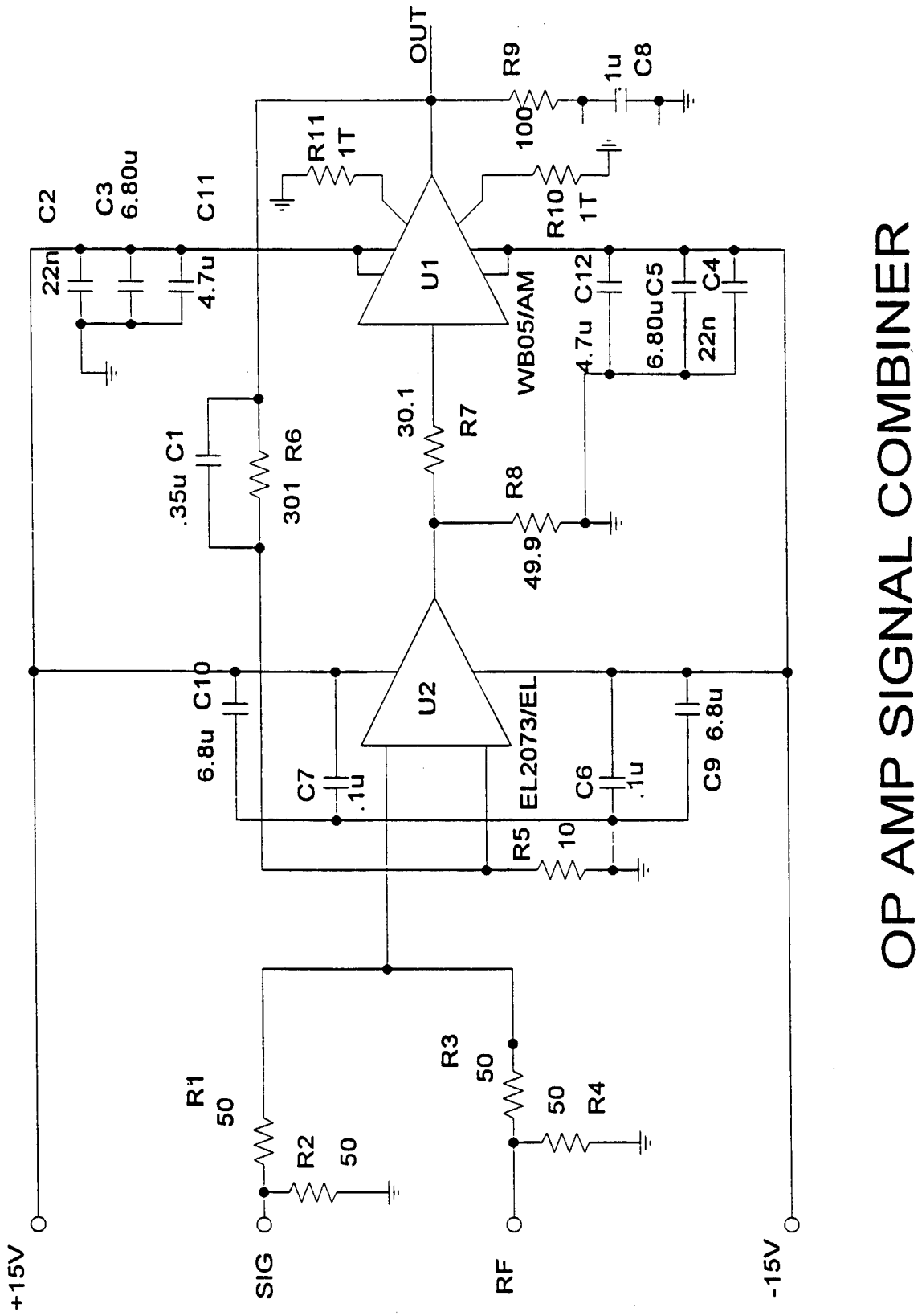


Figure 8-14 Elantec Configuration for Combined Sources (page 1 of 2)

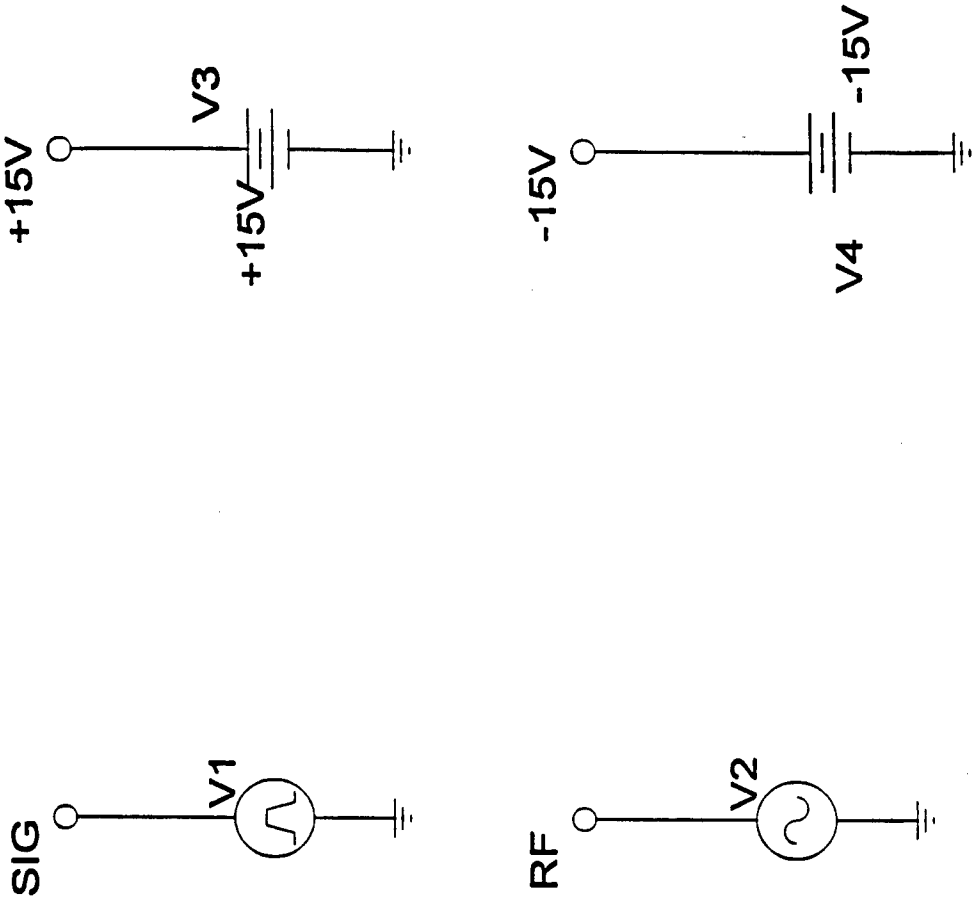


Figure 8-15 Elantec Configuration for Combined Sources (page 2 of 2)

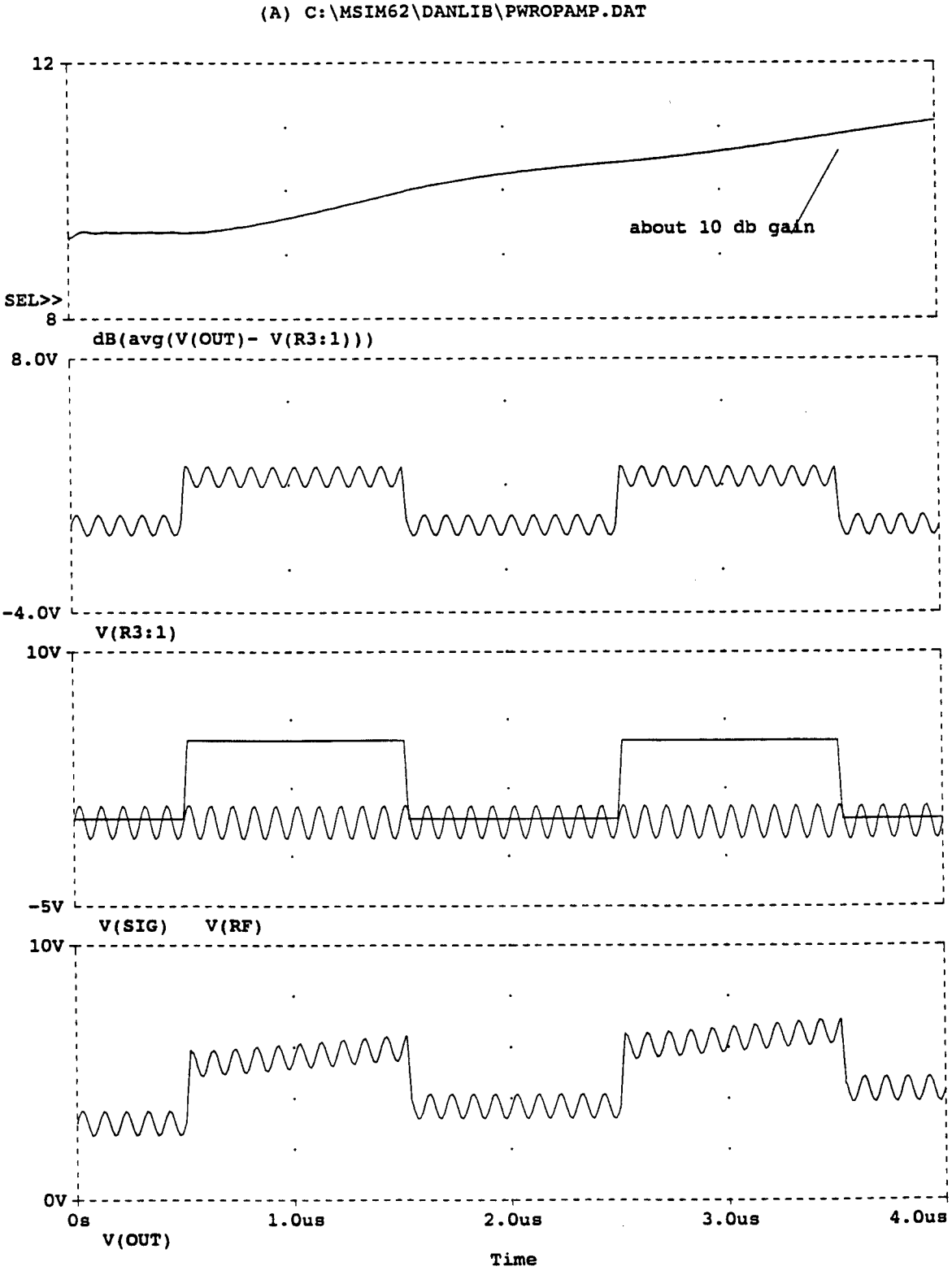
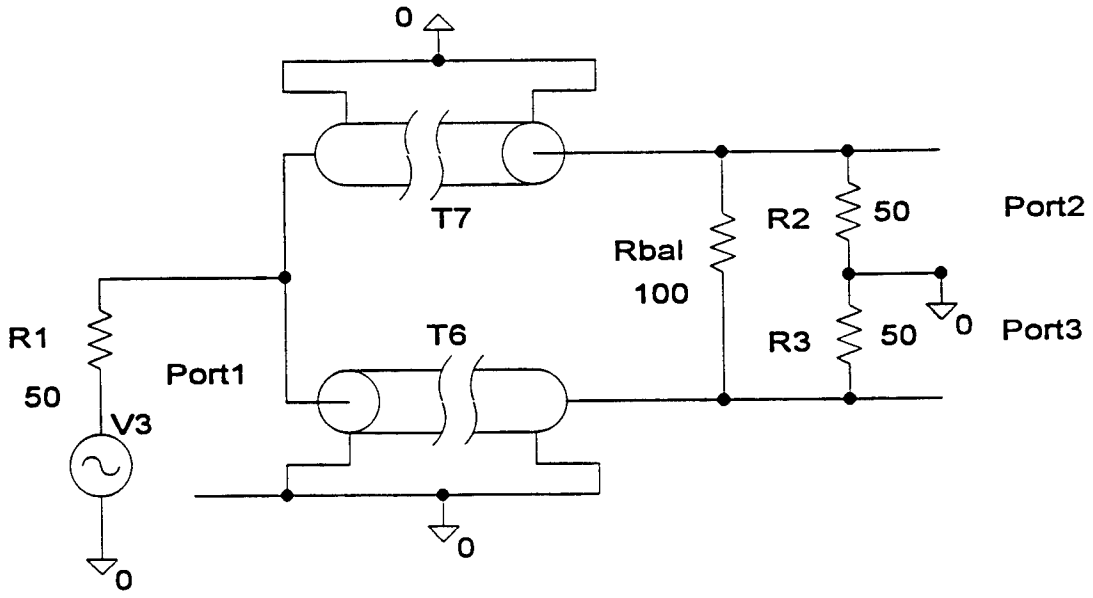


Figure 8-16 Time Domain Responses



Wilkinson 3-dB Power Coupler to Output Ports 2 and 3

(Baseline Transient Solution)

(A) C:\MSIM62\DANLIB\WILKNSN8.DAT

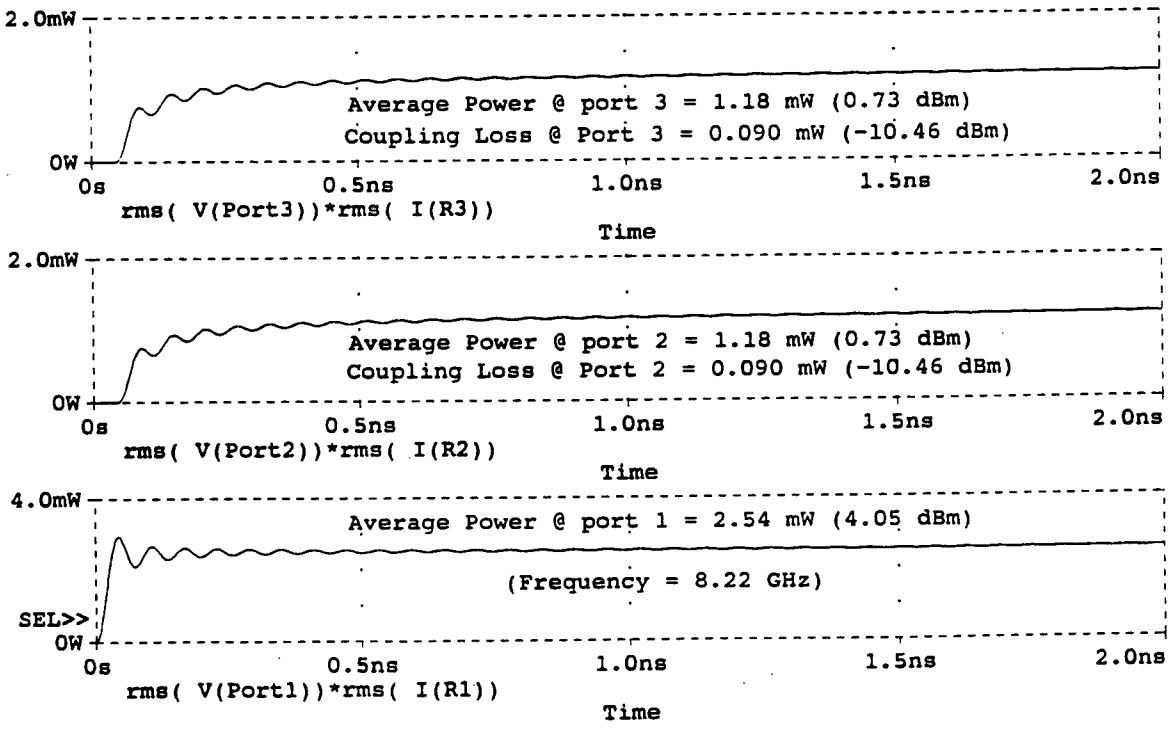
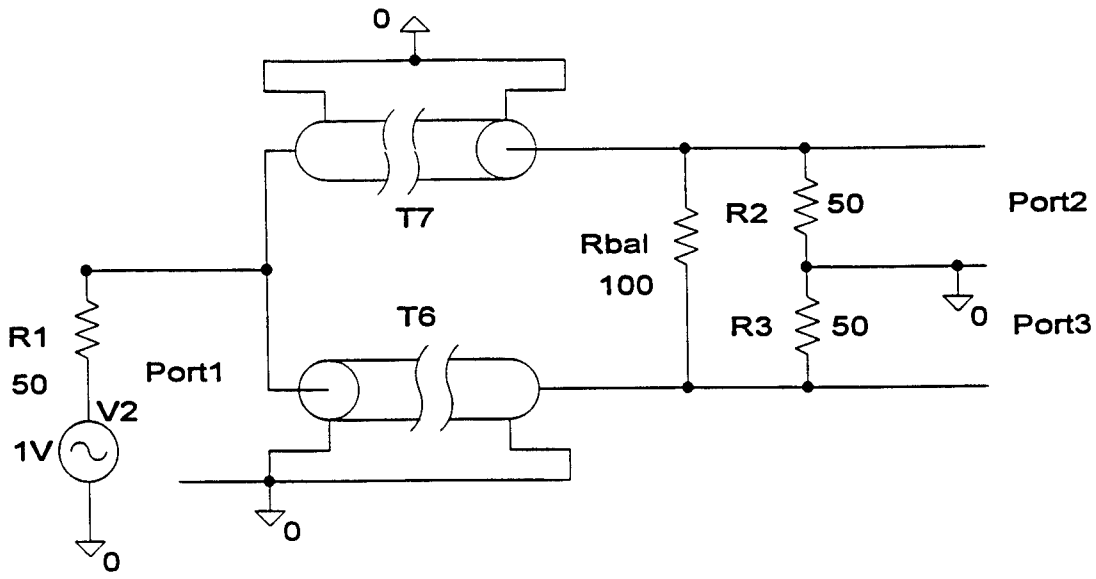


Figure 8-17 Baseline Wilkinson Coupler: Transient Solution



Wilkinson 3-dB Power Coupler to Output Ports 2 and 3

(Baseline Transfer Function Solution)

(A) C:\MSIM62\DANLIB\WILKNSN7.DAT

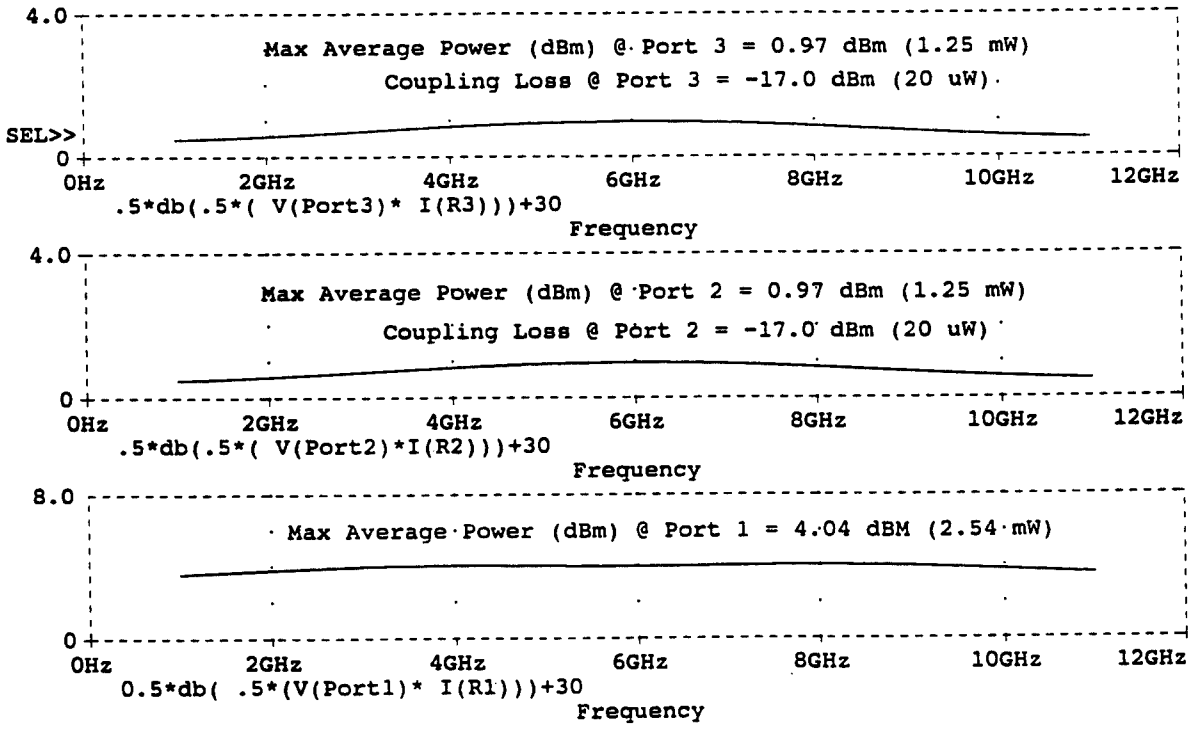
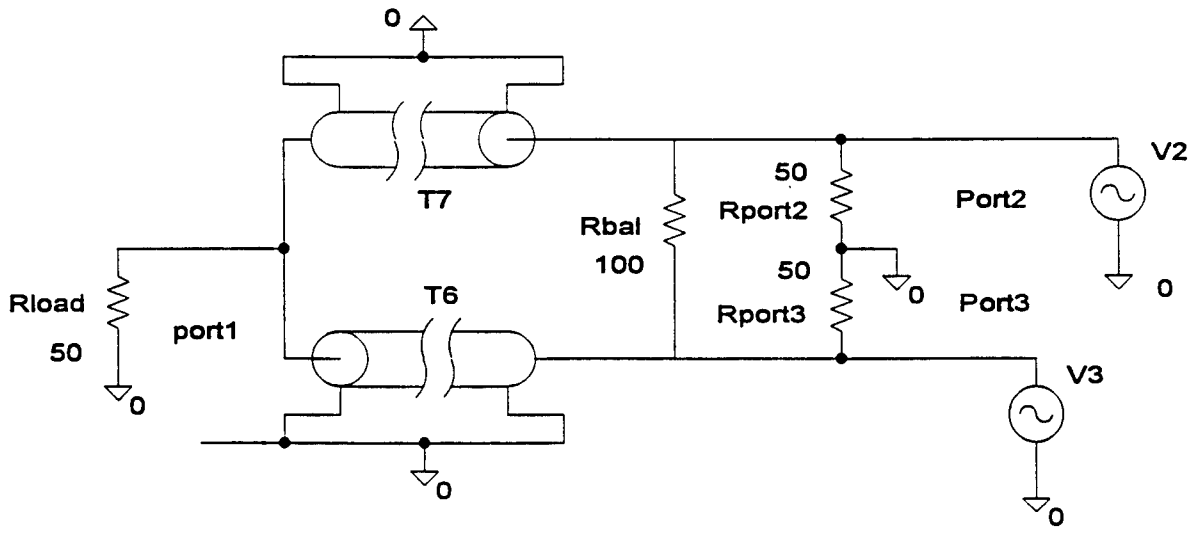


Figure 8-18 Baseline Wilkinson Coupler: Frequency Solution



Note: Average Powers @ ports 2 and 3 "double" average power into Rload

Wilkinson 3-dB Power Combiner
(Transient Solution)

(A) C:\MSIM62\DANLIB\WILKNSN4.DAT

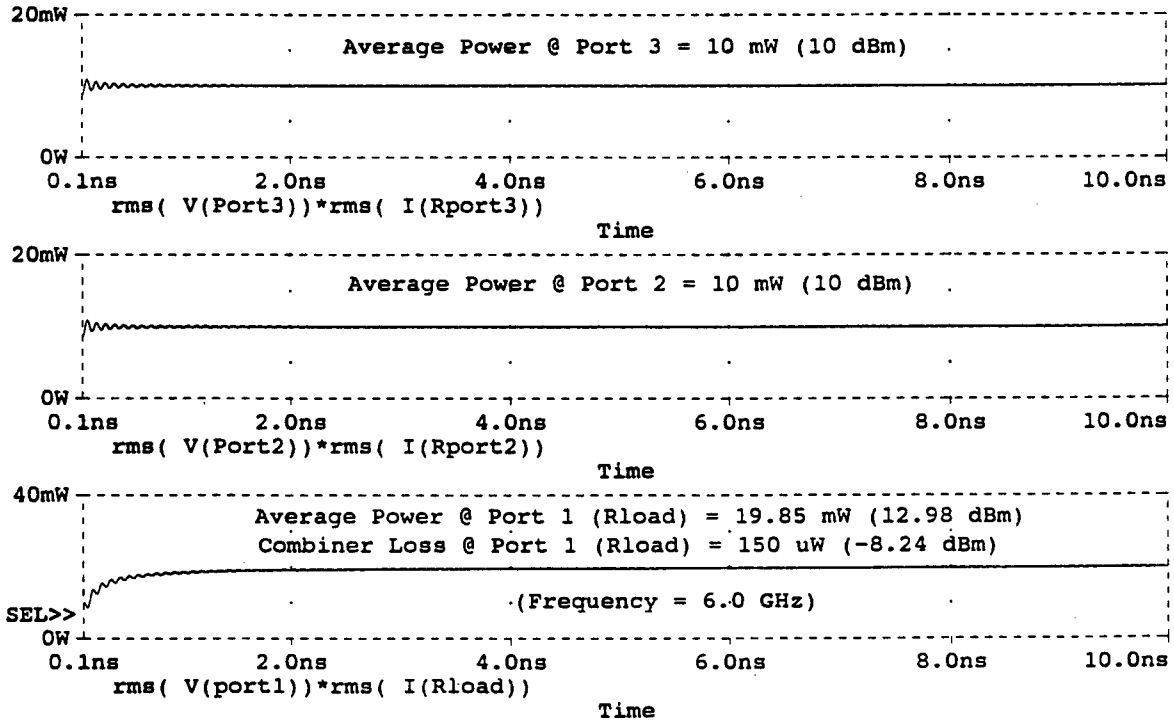
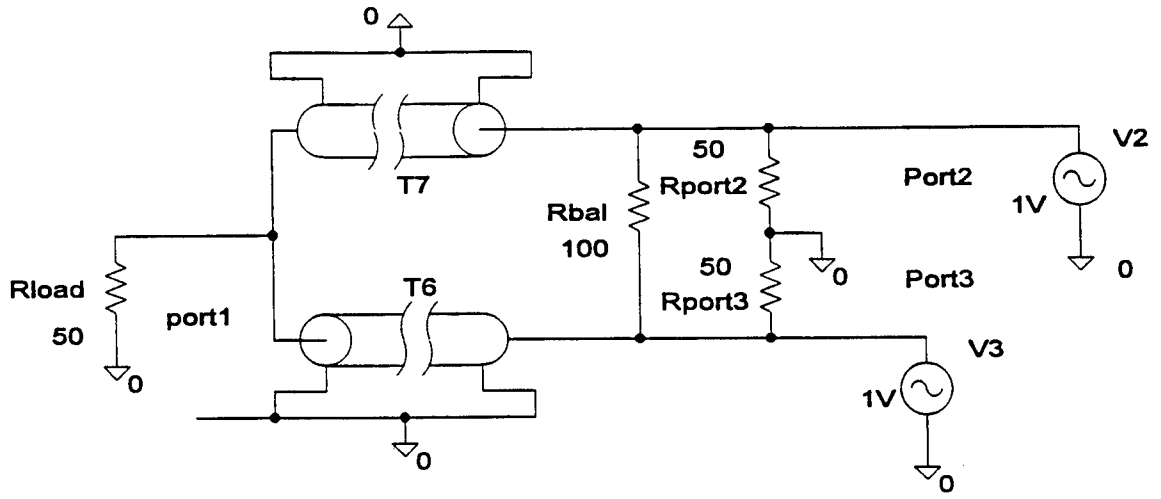


Figure 8-19 Wilkinson Power Combiner: Transient Solution



Note: Average Powers @ ports 2 and 3 "double" average power into Rload

Wilkinson 3-dB Power Combiner
(Transfer Function Solution)

(A) C:\MSIM62\DANLIB\WILKNSN3.DAT

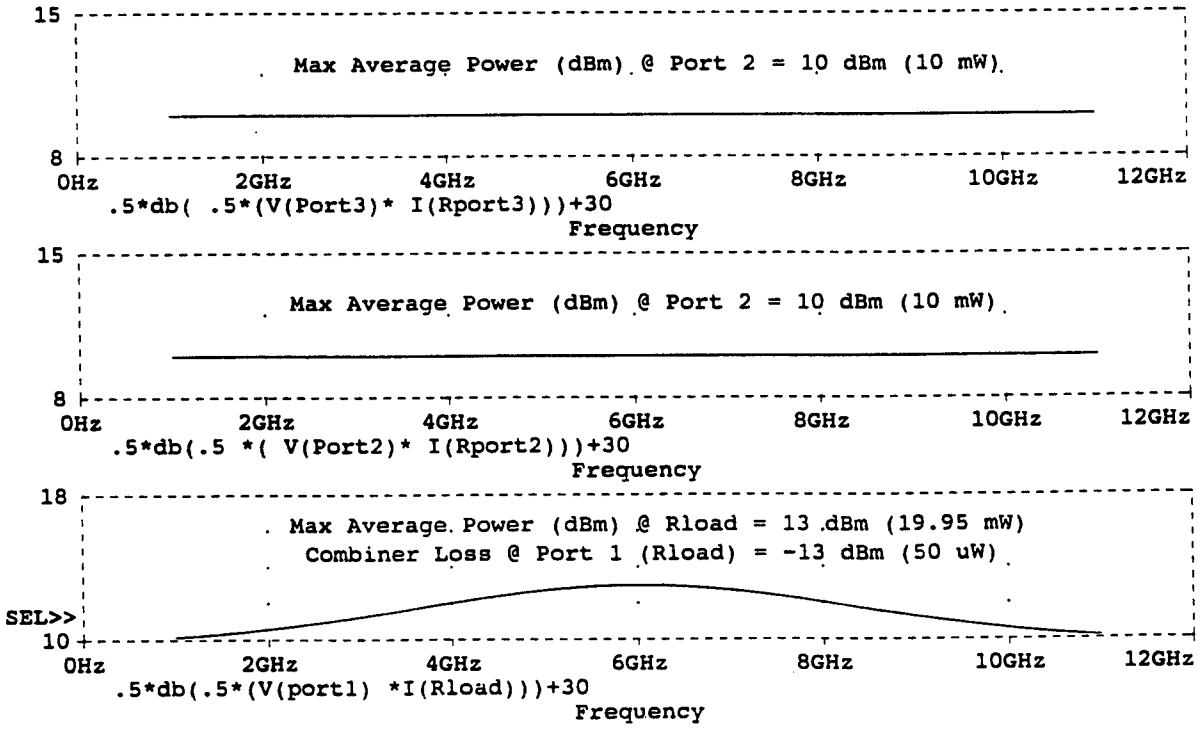


Figure 8-20 Wilkinson Power Combiner: Frequency Solution

9. SCATTERING PARAMETERS

Simulating performance of circuits should also include macromodels to accommodate high frequency, distributed parameter circuits as well as high speed digital circuits. These are usually characterized by scattering matrices. Before developing the necessary scattering macromodels, it is helpful to review some basic theory of scattering parameters. Consider figure 9-1 which shows a linear, time-invariant (LTI) 3-port. A 3-port is chosen to illustrate the fact that undesired EM signals into an n-port device or circuit can be viewed as an (n+1) port interaction. The added port is generally needed to account for the case of parallel coupling of an EM source with the desired signal source: series coupling does not usually need another port. We now develop some PSPICE macromodels needed to characterize a 3-port scattering matrix. An extension to the n-port case will become apparent in the following development.

Let (a1, a2, a3) and (b1, b2, b3) be sets of incident and reflected "waves" at ports 1, 2, and 3, respectively. The term "waves" is a descriptive metric which needs further clarification in the conceptual definition that follows. Obviously, ports 1, 2, and 3 must be rf driven for any wave incidence or reflectance to occur at all the ports. By convention, each component wave in sets (a1, a2, a3) and (b1, b2, b3) are made proportional to the incident and reflected powers at ports 1, 2, and 3, respectively. In other words, we choose proportionality constants for each port that will make $(a1)^2$, $(a2)^2$, and $(a3)^2$ equal to the incident powers at port 1, 2, and 3, respectively. In the same way, we choose proportionality constants for each port that will make $(b1)^2$, $(b2)^2$, and $(b3)^2$ equal to the reflected powers at ports 1, 2, and 3, respectively. These proportionality constants are related to the characteristic impedance (and admittance) of each port, i.e.; sqrt (Z_{0i}) and sqrt (Y_{0j}), respectively, and where indices "i" and "j" are the port designators.

It is possible to associate voltages and currents with the incident and reflected waves at all the ports of interest. As is commonly done in the development of other circuit Z, Y, H, etc. matrices,

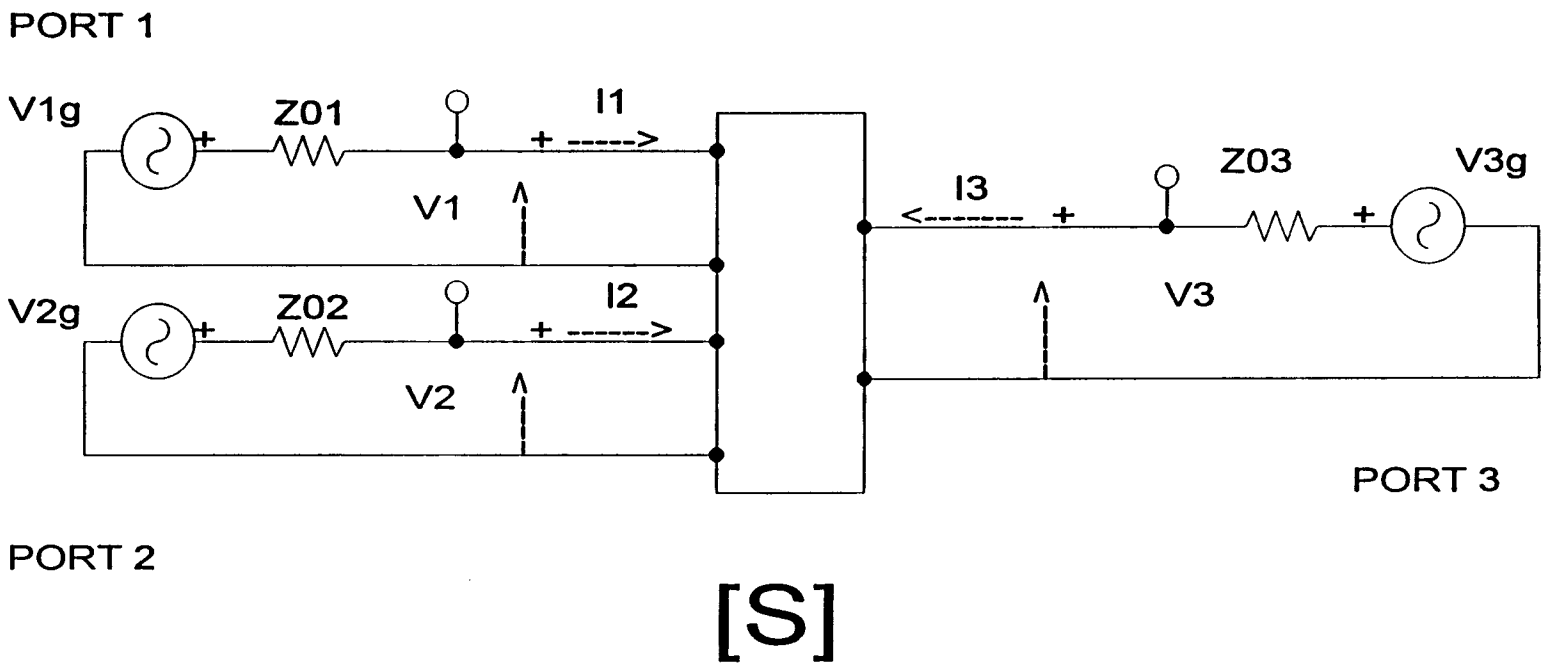


Figure 9-1 Scattering Matrix Definition: (LTI) 3-Port

SCATTERING MATRIX DEFINITION
LINEAR, TIME-INVARIANT 3 - PORT

we define the total voltages and currents at port k (k=1..3) as shown, where $V_k = V_{kincident} + V_{kreflected}$ and $I_k = I_{kincident} - I_{kreflected}$. A datum or ground port (k=0) is assumed. With these commonly used definitions and conventions, we eventually come to:

$$a = 1/2*(\text{sqrt } Yo)*V + 1/2*(\text{sqrt } Zo)*I \quad (1)$$

$$b = 1/2*(\text{sqrt } Yo)*V - 1/2*(\text{sqrt } Zo)*I \quad (2)$$

where V and I are column vectors for the port voltages and currents as defined in the above figure, and sqrt (Yo) and sqrt (Zo) are diagonal matrices for port characteristic impedances and admittances. A dimensional analysis of (1) and (2) will confirm that a's and b's are in fact related to the incident and reflected powers at the ports of interest. The constants of proportionality are the sqrt's of the ports' characteristic impedance and admittance.

We can now introduce the concept of a scattering matrix for the LTI 3-port which relates vectors a and b in a linear equation b = S*a, or:

$$\begin{aligned} b1 &= s11*a1 + s12*a2 + s13*a3 \\ b2 &= s21*a1 + s22*a2 + s23*a3 \\ b3 &= s31*a1 + s32*a2 + s33*a3 \end{aligned} \quad (3)$$

For a given LTI network, the scattering parameters (s_{ij}) can be found in terms of either incident and reflected voltages or currents. In general, voltage derived and current derived S-parameter matrices are different. While their diagonal elements are equal, their off-diagonal terms are shown to be different. These two S-parameter matrices, voltage and current derived, are made equal only when all their port impedances and admittances are each set equal to the same constants which are usually chosen to be the characteristic impedances and admittances of the ports. These constants are also known as the S-matrix "normalizing constants" because they are commonly used to normalize the

port voltages and currents to the characteristic impedances and admittances of their respective ports. For example, for most rf systems, we usually choose Zo = 50 ohms and Yo = 20 mS, so that sqrt (Zo) elements and sqrt (Yo) elements are set equal to +8.5 dB and -8.5 dB, respectively.

To compute or "measure" the S-parameters with PSPICE macromodels, we need to find s11 = b1/a1 when a2 = a3 = 0; s22 = b2/a2 when a1 = a3 = 0; and s33 = b3/a3 when a1 = a2 = 0. Note, that to make the a's equal to zero means the incident waves at such ports are made zero. This implies no sources at those ports. The particular port is then simply passive; its voltage generator is short-circuited and the port terminated in its own characteristic impedance. Similarly, to find s12, s13, s21, s23, s31, s32, we need to find s12 = b1/a2 when a1 = a3 = 0; s13 = b1/a3 when a1 = a2 = 0; s21 = b2/a1 when a2 = a3 = 0: s23 = b2/a3 when a1 = a2 = 0; s31 = b3/a1 when a2 = a3 = 0; and s32 = b3/a2 when a1 = a3 = 0. Again, the a's are made zero by simply short-circuiting the voltage generators at the ports of interest. The approach taken is simply to find or generate a voltage related to the input and output impedance mismatches (for s11, s22, and s33), and to find or generate a voltage related to the unity voltage driven, forward and reverse transfer voltages (for s12, s13, s21, s23, s31, and s32).

Consider synthesizing a macromodel for determining s11. Again, referring to figure 9-1 and recalling the previous definitions of scattering parameters, we use equation (1-3) to get: s11 = b1/a1 = (V1 - Zo*I1)/(V1 + Zo*I1), where we have set the port characteristic impedance Zo1 to be equal to the normalizing number Zo, made ports 2 and 3 passive, and terminated each port in Zo2 = Zo3 = Zo. So now,

$$s11 = (Zin1 - Zo)/(Zin1 + Zo) \text{ where } Zin1 \text{ is simply } V1/I1 \text{ at port 1.}$$

or (4)

$$s11 = (2*Zin1 - (Zin1 + Zo))/(Zin1 + Zo) = 2*Zin1/(Zin1 + Zo) - 1.$$

Thus, all that is needed now is to find a sub-circuit to compute or "measure" the input impedance

divider at port 1 in terms of Zin1 and (Zin1 + Zo), subtract unity, and set the normalizing Zo as 50 ohms to make ports 2 and 3 passive. We shall return to its implementation shortly.

Next, consider s22 and s33. Using the same reasoning, we arrive at similar relations:

$$\begin{aligned} s11 &= 2*Zin1/(Zin1 + Zo) - 1 \text{ with ports 2 and 3 each passive in Zo} \\ s22 &= 2*Zin2/(Zin2 + Zo) - 1 \text{ with ports 1 and 3 each passive in Zo} \\ s33 &= 2*Zin3/(Zin3 + Zo) - 1 \text{ with ports 1 and 2 each passive in Zo.} \end{aligned} \tag{5}$$

Thus, reflection coefficients s11, s22, s33 (and reflection coefficients s_{kk} , in general) all use sub-circuits which have the same topology!

For off-diagonal S-parameters Sij where i is not equal to j, we consider s12 = b1/a2 when a1 = a3 = 0; i.e., ports 1 and 3 are passive; or

$$s12 = (V1 - Zo*I1)/(V2 + Zo*I2).$$

Now at port 2, V2 + Zo*I2 = +Vg2 and at port 1, Vg1 = 0 or V1 = -I1*Zo. So that,

$$s12 = 2*V1/Vg2.$$

Thus, to measure s12, we need simply to measure the output voltage V1 at port 1 when port 2 is driven with its Vg2 set equal to one volt, and ports 1 and 3 are each made passive in Zo. For the remaining off-diagonal S-parameters, similar reasoning leads to the following algorithms:

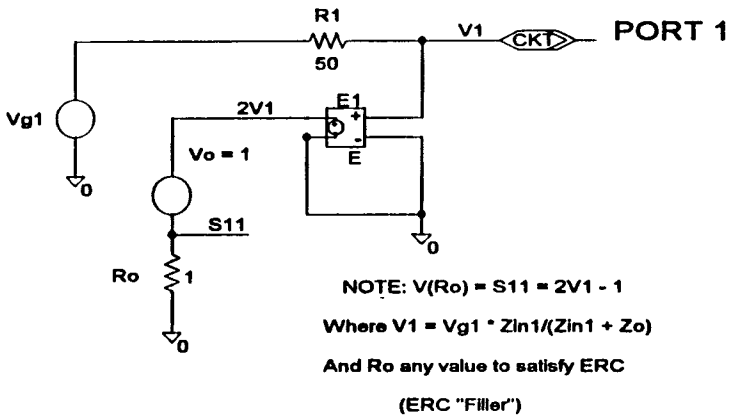
$$\begin{aligned} s12 &= 2*V1/Vg2 \text{ with ports 1 and 3 each passive in Zo} \\ s13 &= 2*V1/Vg3 \text{ with ports 1 and 2 each passive in Zo} \\ s21 &= 2*V2/Vg1 \text{ with ports 2 and 3 each passive in Zo} \\ s23 &= 2*V2/Vg3 \text{ with ports 1 and 2 each passive in Zo} \\ s31 &= 2*V3/Vg1 \text{ with ports 2 and 3 each passive in Zo} \\ s32 &= 2*V3/Vg2 \text{ with ports 1 and 3 each passive in Zo.} \end{aligned} \tag{6}$$

In general, to measure transmission coefficients s_{ij}, we need to drive port j with its voltage generator Vgj = 1, terminate the remaining ports in 50 ohms, and look at the voltage response V_i at

port i. Thus, transmission coefficients s12, s13, s21, ... (and transmission coefficients s_{jk} , in general) all use sub-circuits which have the same topology! To measure reflection coefficients s_{kk}, we need to drive port k with its voltage generator Vgk = 1, terminate the remaining ports in 50 ohms, and look at the voltage response at port k. These simple algorithms in equations (5) and (6) can be easily implemented in PSPICE macromodels. We only need two sub-circuits for the LTI 3-port; one for the diagonal terms s11, s22, and s33; and one for the off-diagonal terms s12, s13, s21, s23, s31, and s32. Each sub-circuit will adopt the unique reference designators that are compatible with whatever port notation is used in the particular schematic application.

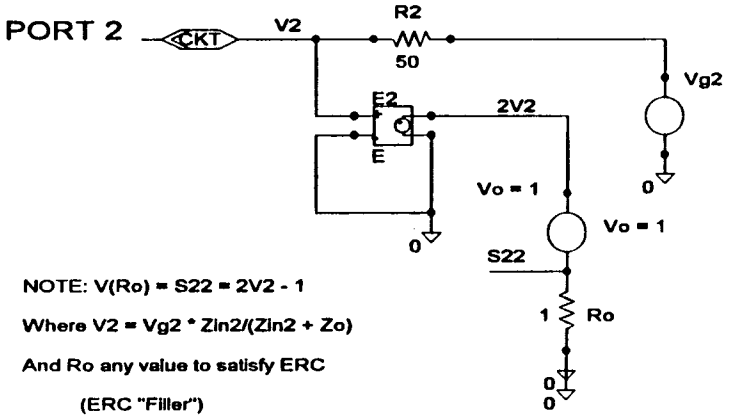
To implement the S-parameter algorithms in sub-circuits, we first consider the diagonal terms s_{kk} , where k = 1, 2, and 3. We have already shown that s_{kk} = 2*Zink/(Zink + Zo) - 1, where Zink is the unknown input impedance at port k when the other remaining ports are made passive and each terminated in Zo. In a 2-port application, for example, finding s11 at port 1 would require having its Vg1 source active, taping off a response voltage V1 at port 1, doubling it, and subtracting unity. Note that V1 is also the voltage response across the Zin1 "element" of a voltage divider formed with Zo and driven by Vg1. In other words, V1 equals Vg1 * Zin1/(Zin1 + Zo). Then, if we double the voltage V1 at port 1 and subtract a unity voltage, we will have the desired sub-circuit for s11. The desired sub-circuit to measure s11 is shown in figure 9-2 (a) where a voltage dependent, voltage source E1 with a gain of 2 is used to realize the needed doubler. Other suitable analog behavioral models (ABM) for a multiplier could also be used for this function. Elsewhere in this report, we used a variety of E devices, including multipliers and summing ABM blocks.

In the sub-circuit shown in figure 9-2 (a), note that a voltage equal to s11 is measured across the Ro resistor which is a "dummy" element (i.e., it can have any nonzero value) to satisfy ERC constraints in PSPICE. To measure s22 and s33 S-parameters, we would use iterated sub-circuits of identical topology. For example, for a 2-port application, a sub-circuit configuration needed to



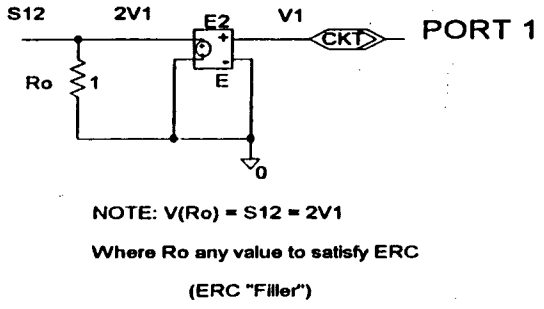
(a)

Coupler to Measure S11



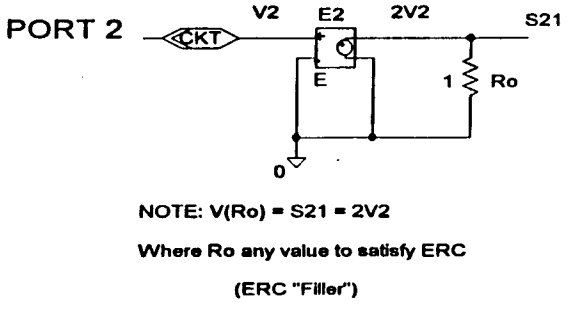
(b)

Coupler to Measure S22



(c)

Coupler to Measure S12



(d)

Coupler to Measure S21

Figure 9-2 Scattering Parameter Couplers

When connected to port 2, it is topologically the same circuit used to measure s11.

Next, we consider the implementation of the diagonal terms s_{ij}, where i is not equal to j. The algorithm for s_{ij} is particularly simple. We have already shown that sij is equal to 2*Vi/Vgj with the remaining ports (not equal j) each passive in Zo. Thus at port j, we set its voltage generator Vgj = 1, terminate the remaining ports in 50 ohms, and look for the voltage response at port i. For a 2-port application, for example, s12 is measured by the circuit shown in figure 9-2 (c), where the s12 is twice the voltage response at port 1 when port 2 is driven by its source Vg2 . Again, a voltage controlled, voltage source E2 of gain 2 was used to realize the required doubler and Ro is the filler element needed to satisfy ERC. Measuring s21 follows in the same way as measuring s12: figure 9-2 (d) shows the resulting sub-circuit. Again, when it is connected to port 2, it is topologically the same sub-circuit used to measure s12. While the S-parameter algorithms derived above were not empirically validated in this study, they are consistent with previously published results [1].

The reader is reminded again that using these identical sub-circuits in the same application or schematic will require that each sub-circuit adopt unique (or part) reference designators so that they are compatible with whatever port notation is used for the particular schematic application. In most cases, PSPICE will automatically do this or output an error message to the contrary. Finally, it should be pointed out that these sub-circuits can also be renamed to special symbol files and saved in user defined or default symbol libraries. They are then made available to the PSPICE schematic editor in the same way as the other circuit primitives are available for use in any other applications' schematics.

To illustrate use of these S-parameter macros, the following figures are included. Figure 9-3 is a baseline UHF amplifier1, figures 9-4 and 9-5 show its configurations for determining s11 and s21 measurements and the resulting performance characterizations. Figures 9-6 thru 9-8 show UHF amplifier1 configured for s22 and s12 measurements, and the resulting performance characterizations.

Note, the latter figures use DC voltage sources V22 for s11 and V29 for s22 to effect the unity voltages needed for subtraction in equation (5). Next, figures 9-9 thru 9-13 show the same UHF amplifier1 configured again for s11 and s21 measurements, and the resulting responses but now using AC voltage sources instead of DC unity sources. These unity AC sources are V8 for s11 and V15 for s22. Figures 9-11 thru 9-13 show UHF amplifier1 configured for s22 and s12 measurements, and resulting responses; again, using an AC unity source V15 for s22. There are some observed differences in responses between AC and DC sources which are not explained at this time. Figure 9-14 and 9-15 show other performance related data on this UHF amplifier1.

Figure 9-16 and 9-17 show a low-noise UHF amplifier2 schematic, its net list, and some overall results. Figures 9-18 thru 9-20 show a four pole, Butterworth band pass filter centered at 250 MHz, its net list, and configurations for S-parameter measurements. Figures 9-21 thru 9-27 show performance characteristics based on computed S-parameters. In literature on using S-parameters for time domain, performance characterization, there are instances where authors did not use correct modeling. In discrete (and other) circuits models, one must account for impedance mismatches at the input and output ports to determine the corresponding s11 and s22 parameters. Some authors simply use the total response voltages at the port nodes. They assume wideband impedance matches without correcting for the voltage divider (port input impedance and series source impedance) which has been shown to be directly related to the mismatches at these ports. The assumptions of matched ports may give erroneous results in computing s11 and s22. Readers should be alert to this caveat in reviewing contemporary literature.

[1] Unknown Corporate Author, "How to Obtain S-Parameter Data from Probe", MicroSim Source Magazine, April, 1994, MicroSim Corporation, 20 Fairbanks, Irvine, CA. 92718.

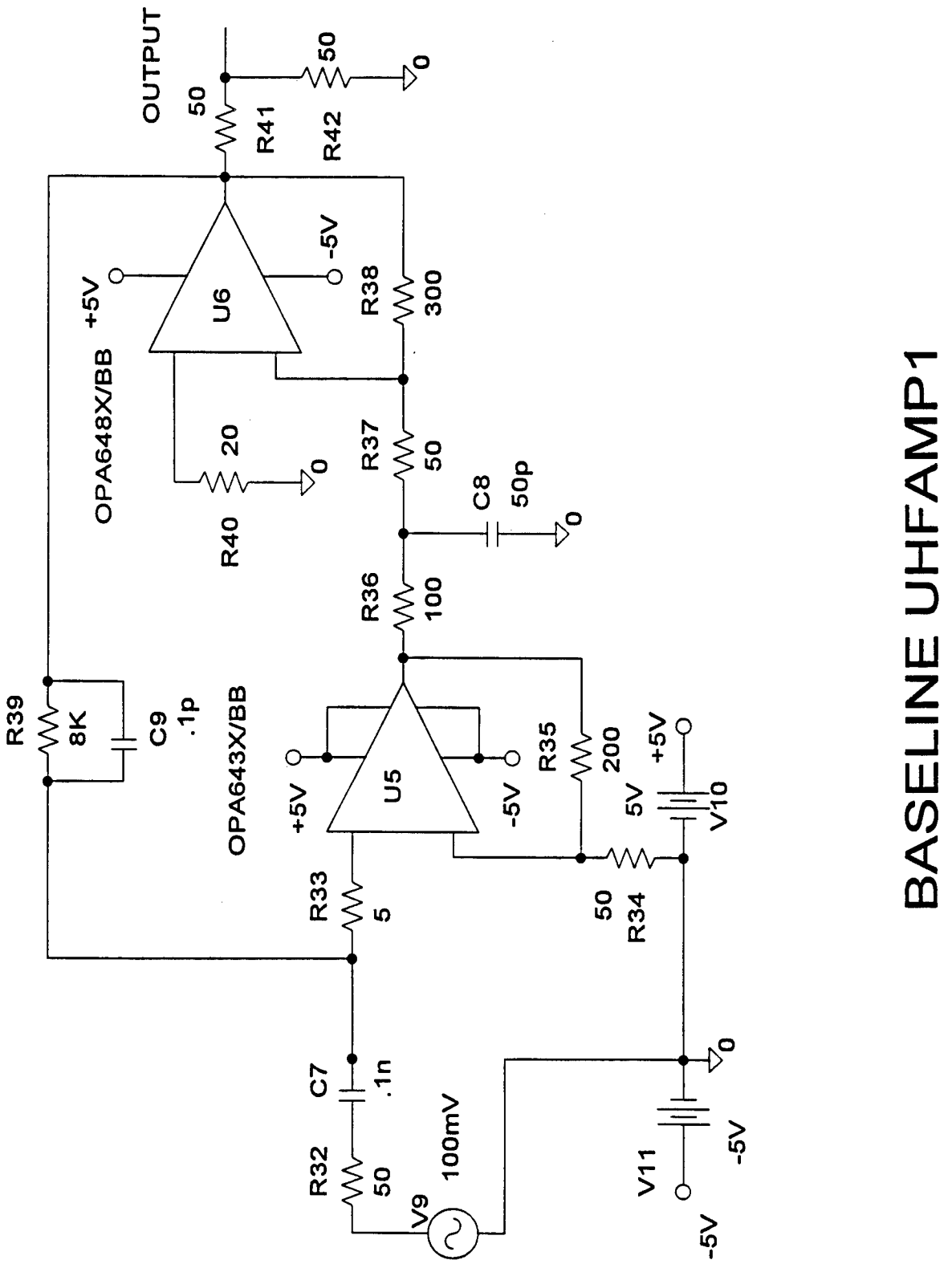


Figure 9-3 Baseline UHFAMP1 Amplifer

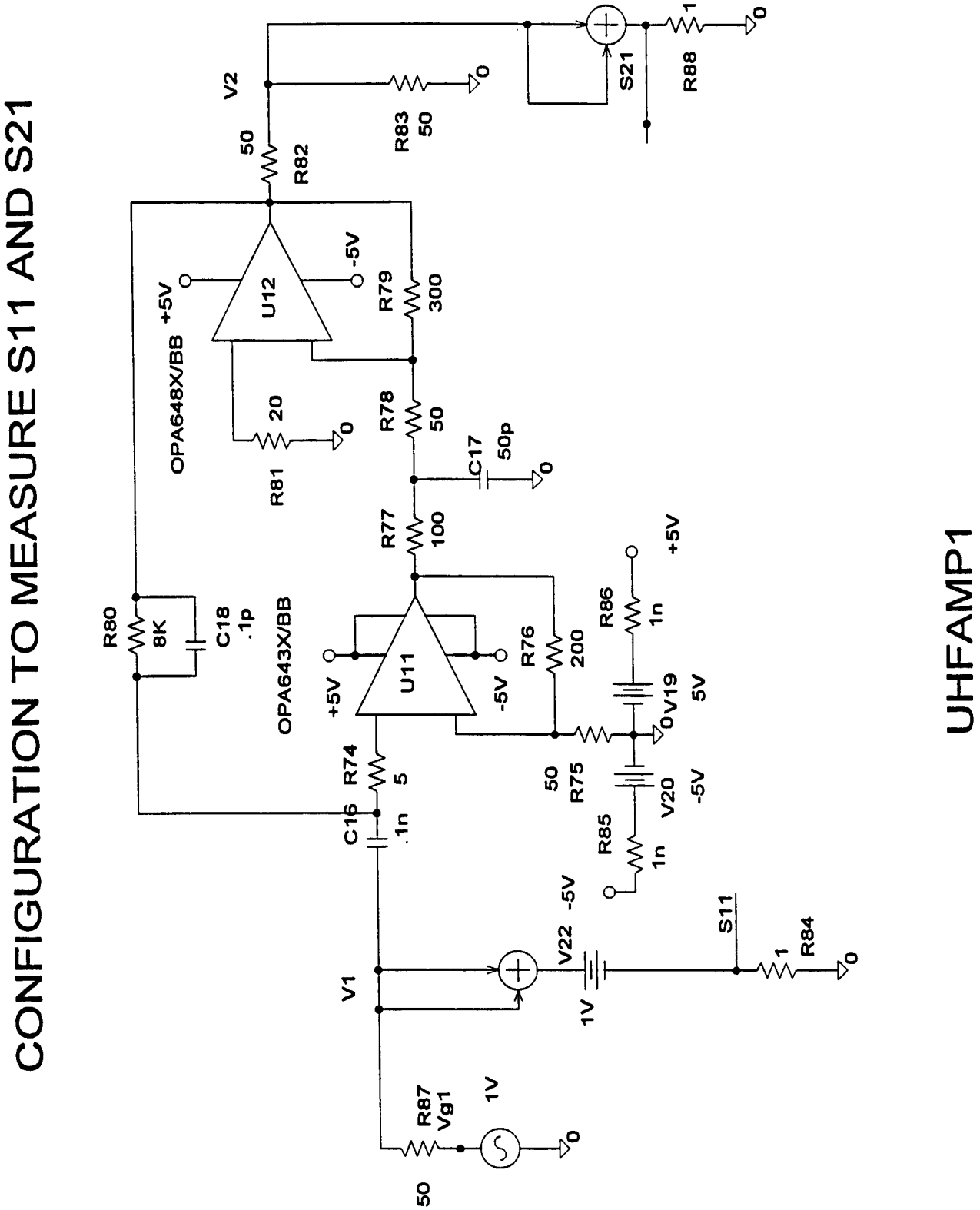


Figure 9-4 UHFAMP1: Configuration for S11 and S21

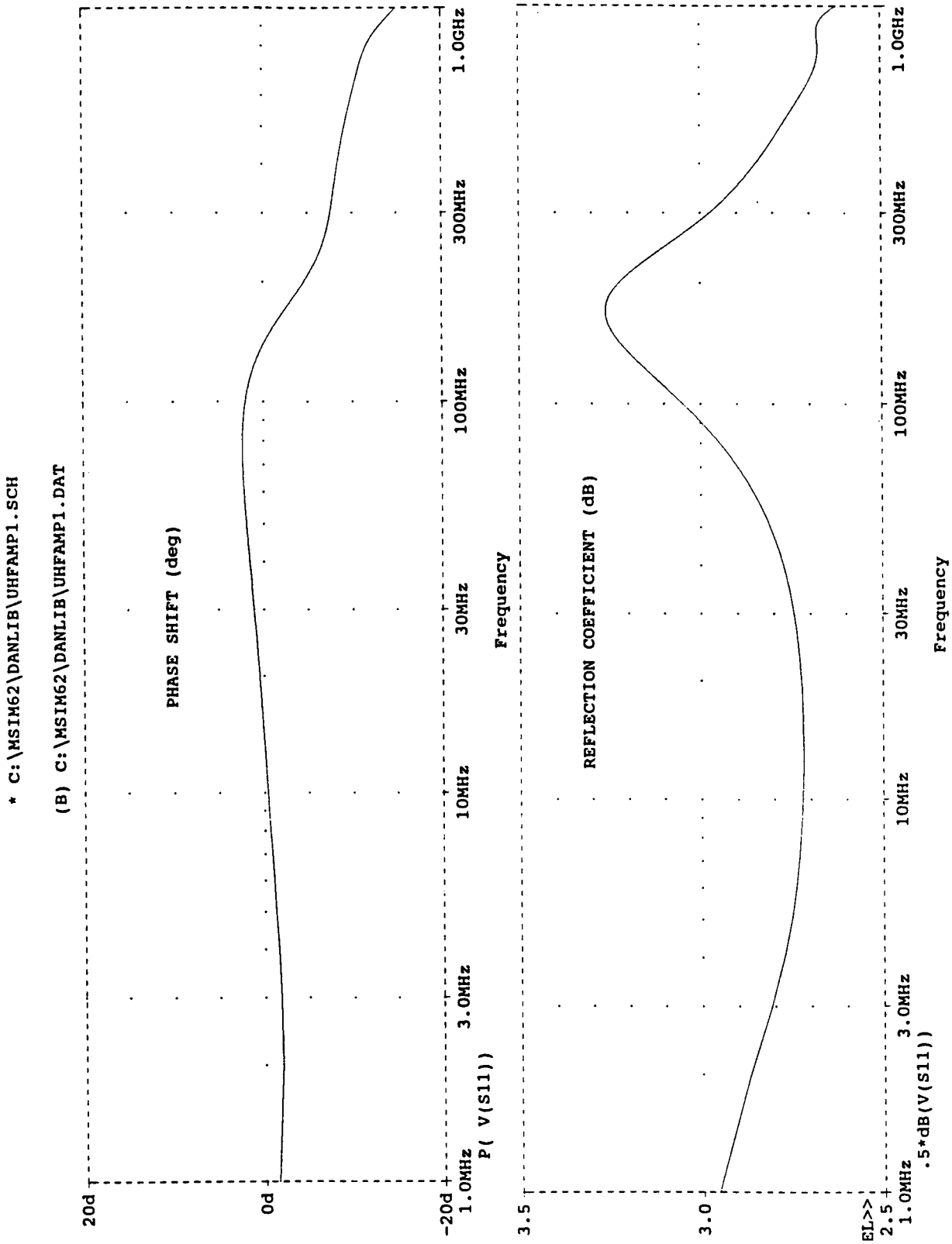


Figure 9-5 UHFAMP1: S11 Magnitude and Phase

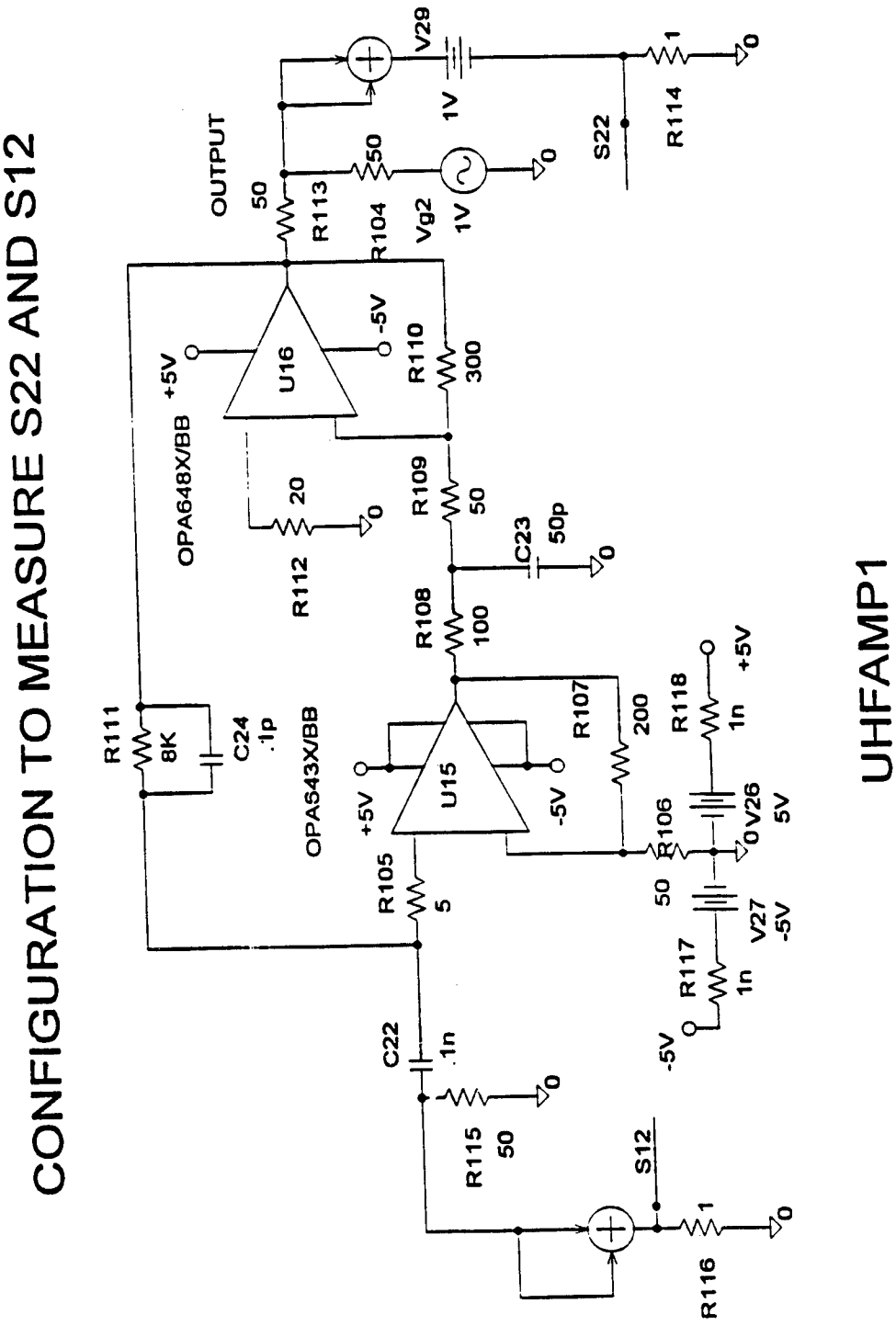


Figure 9-6 UHFAMP1: Configuration for S22 and S12

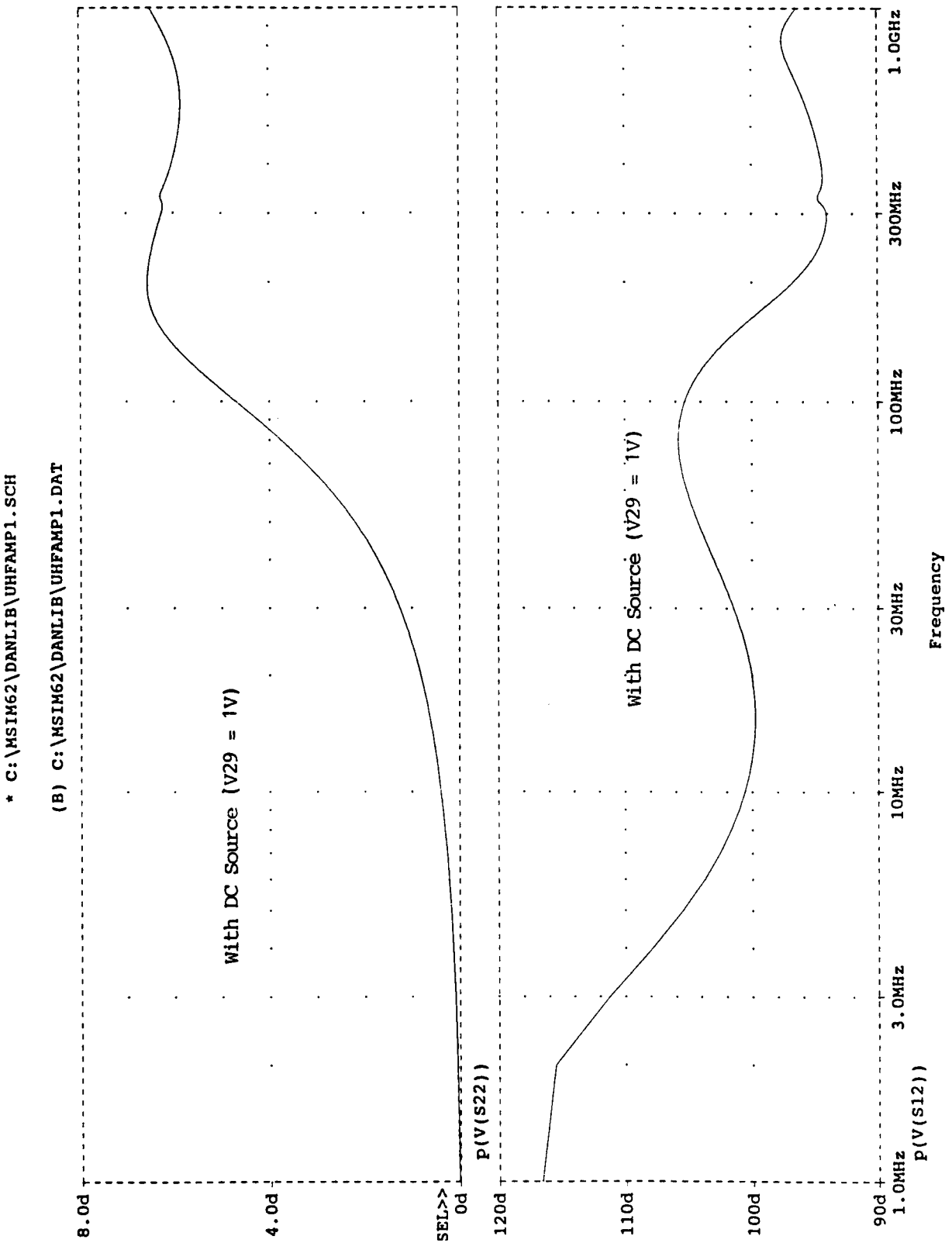


Figure 9-7 UHFAMP1: S22 and S12 Phase Plots Using DC Source (V29=1V)

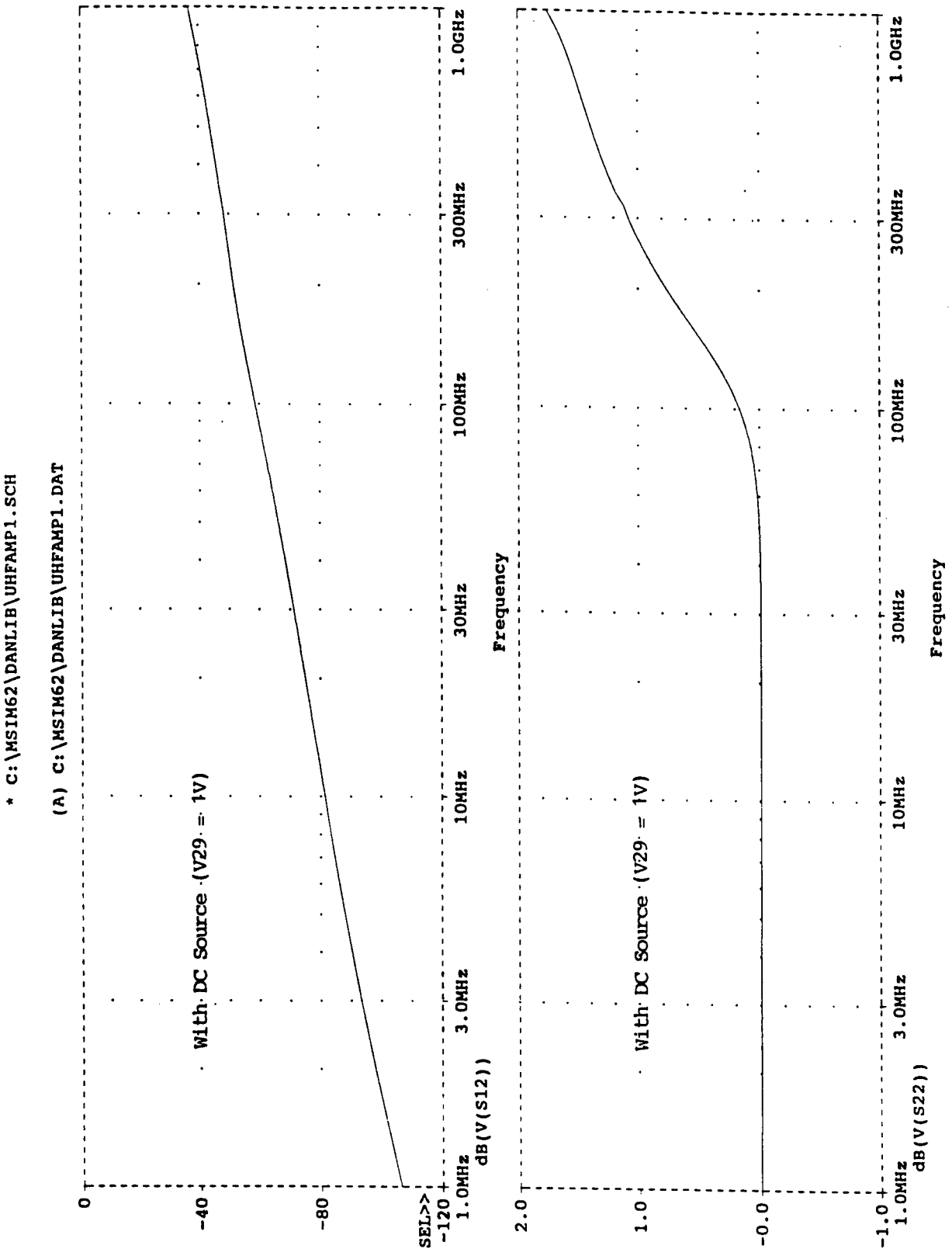


Figure 9-8 UHFAMP1: S22 and S12 Magnitude Plots Using DC Source (V29=1V)

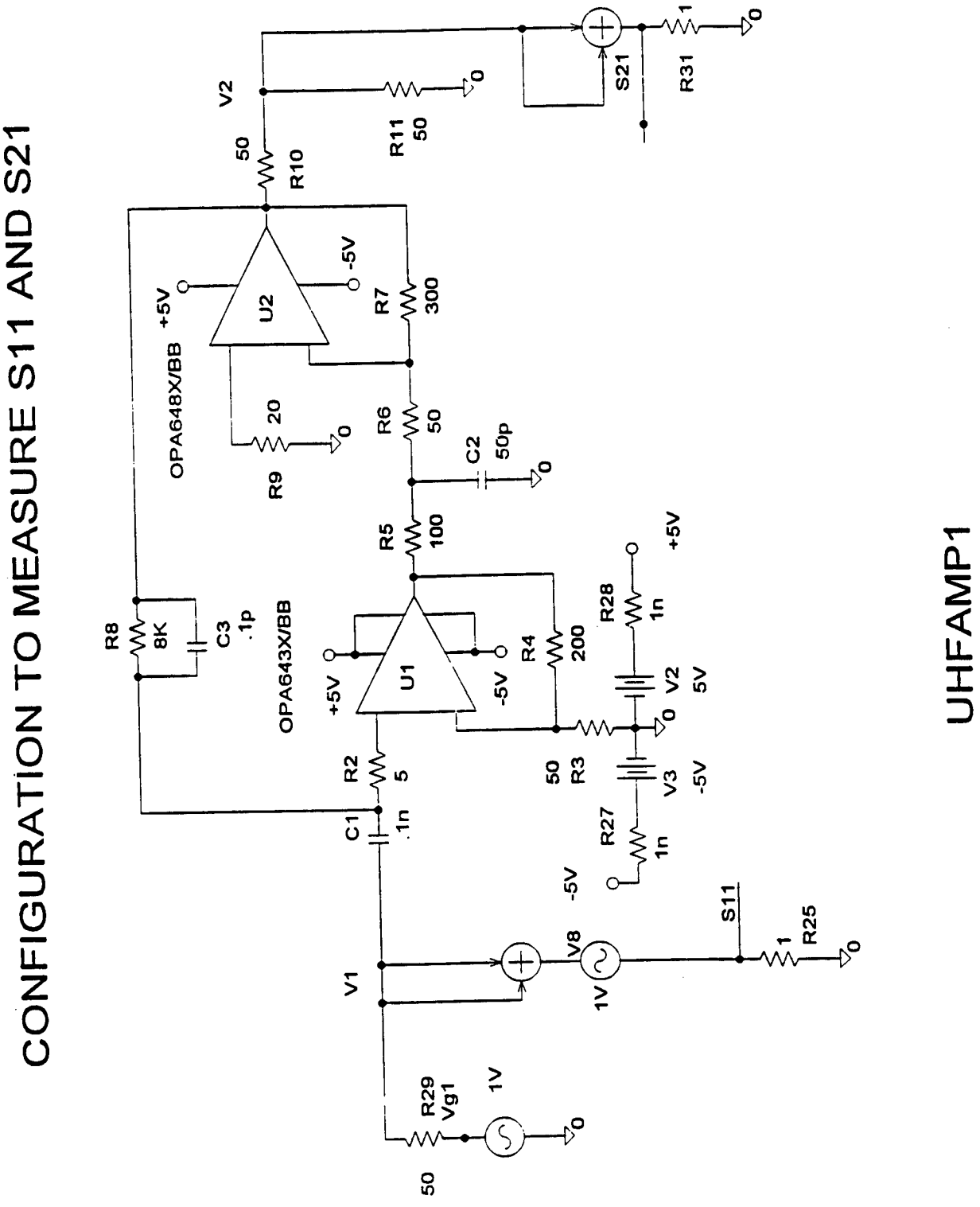


Figure 9-9 Modified UHFAMP1: Configuration for S11 and S21

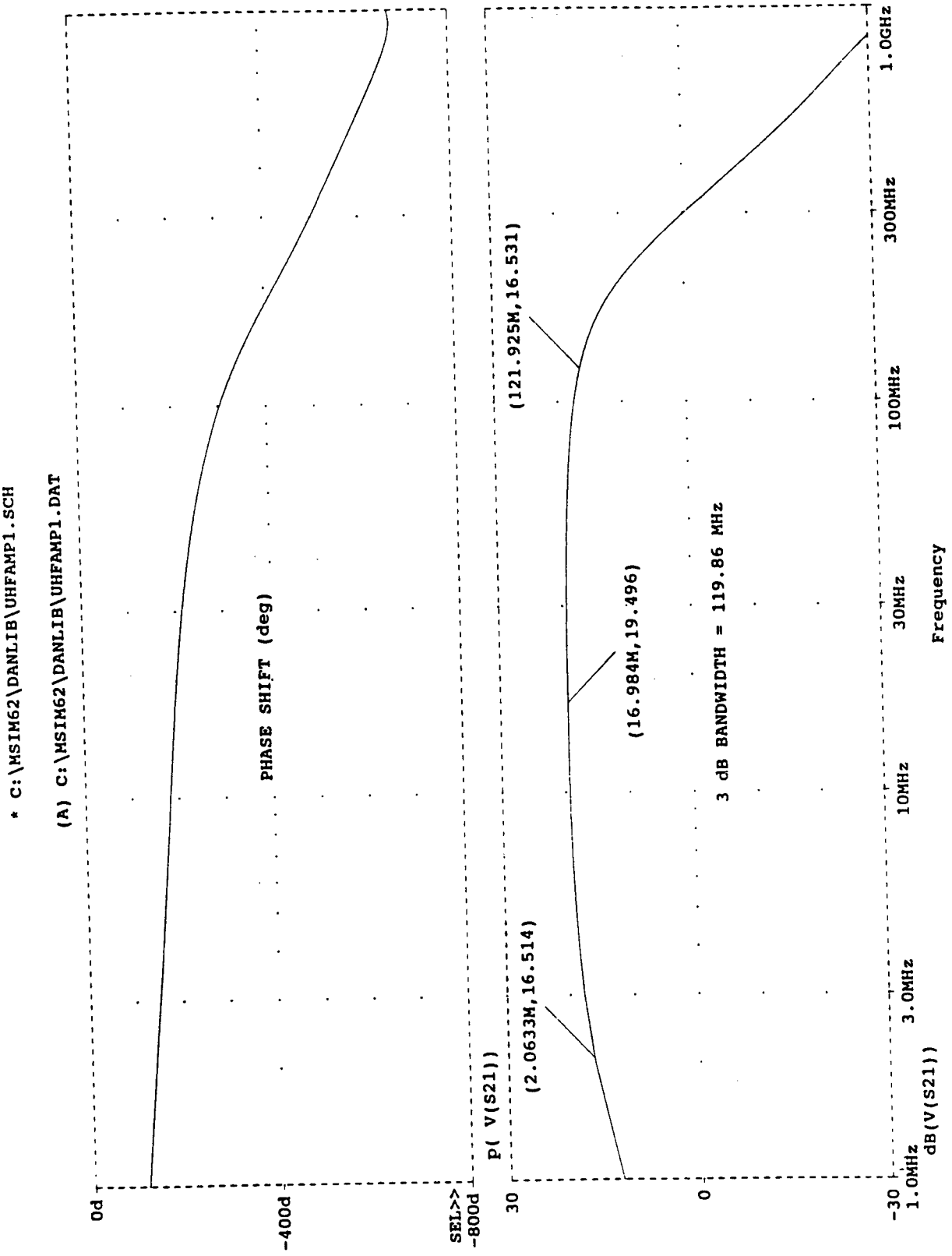


Figure 9-10 Modified UHFAMP1: S21 Magnitude and Phase

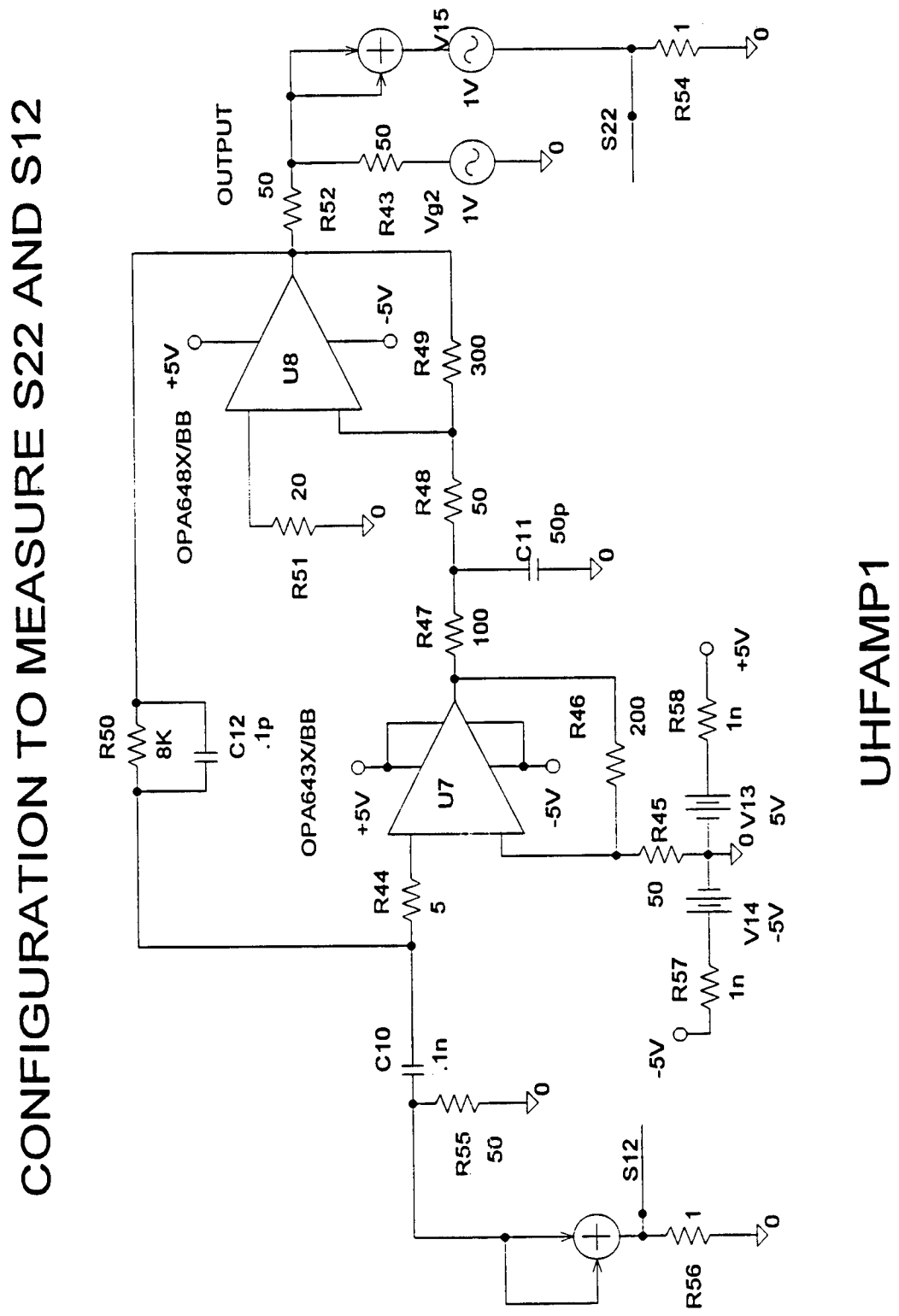


Figure 9-11 Modified UHFAMP1: Configuration for S22 and S12

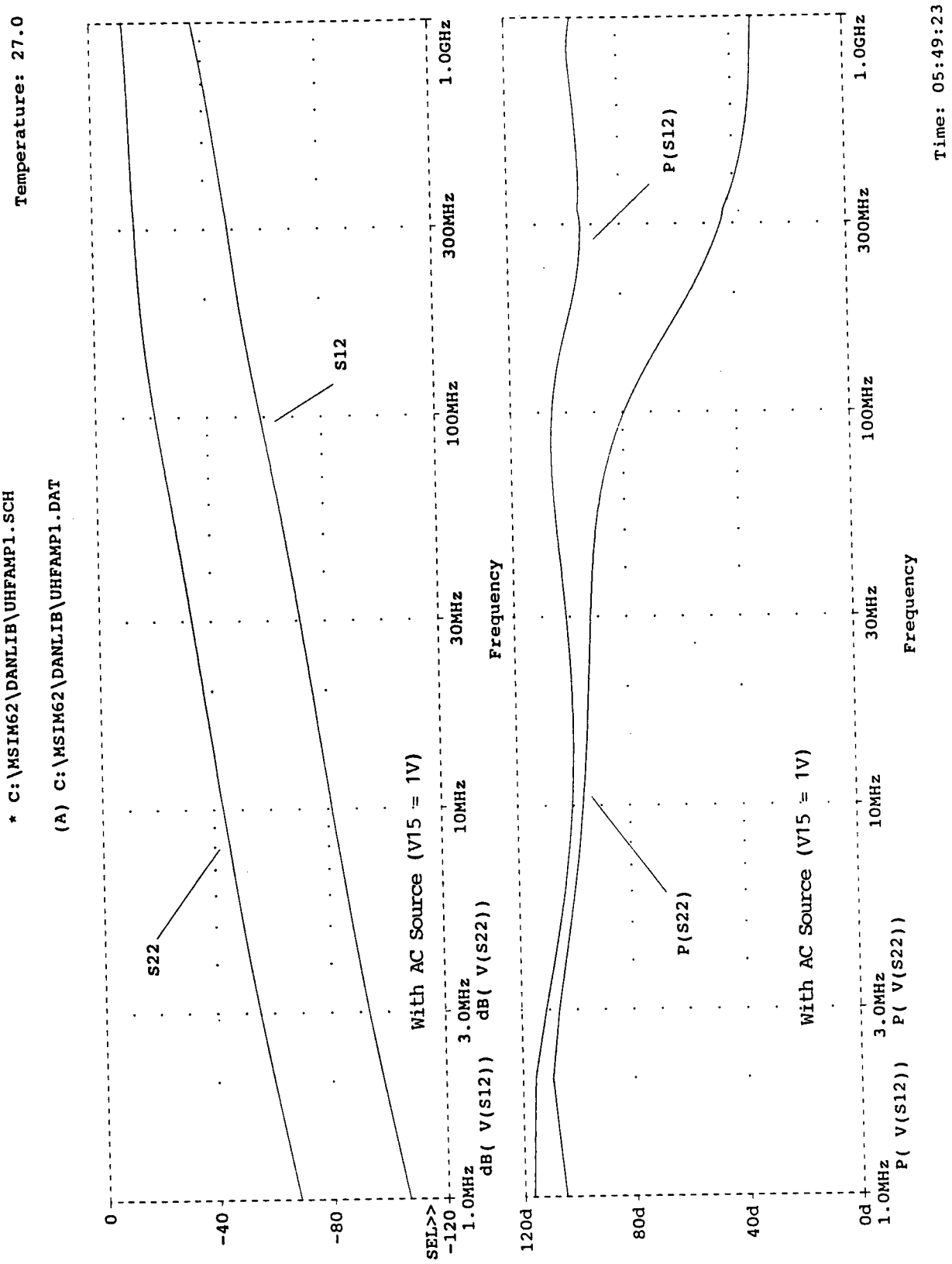


Figure 9-12 S12 and S22, Magnitude and Phase Using AC Source (V15=1V)

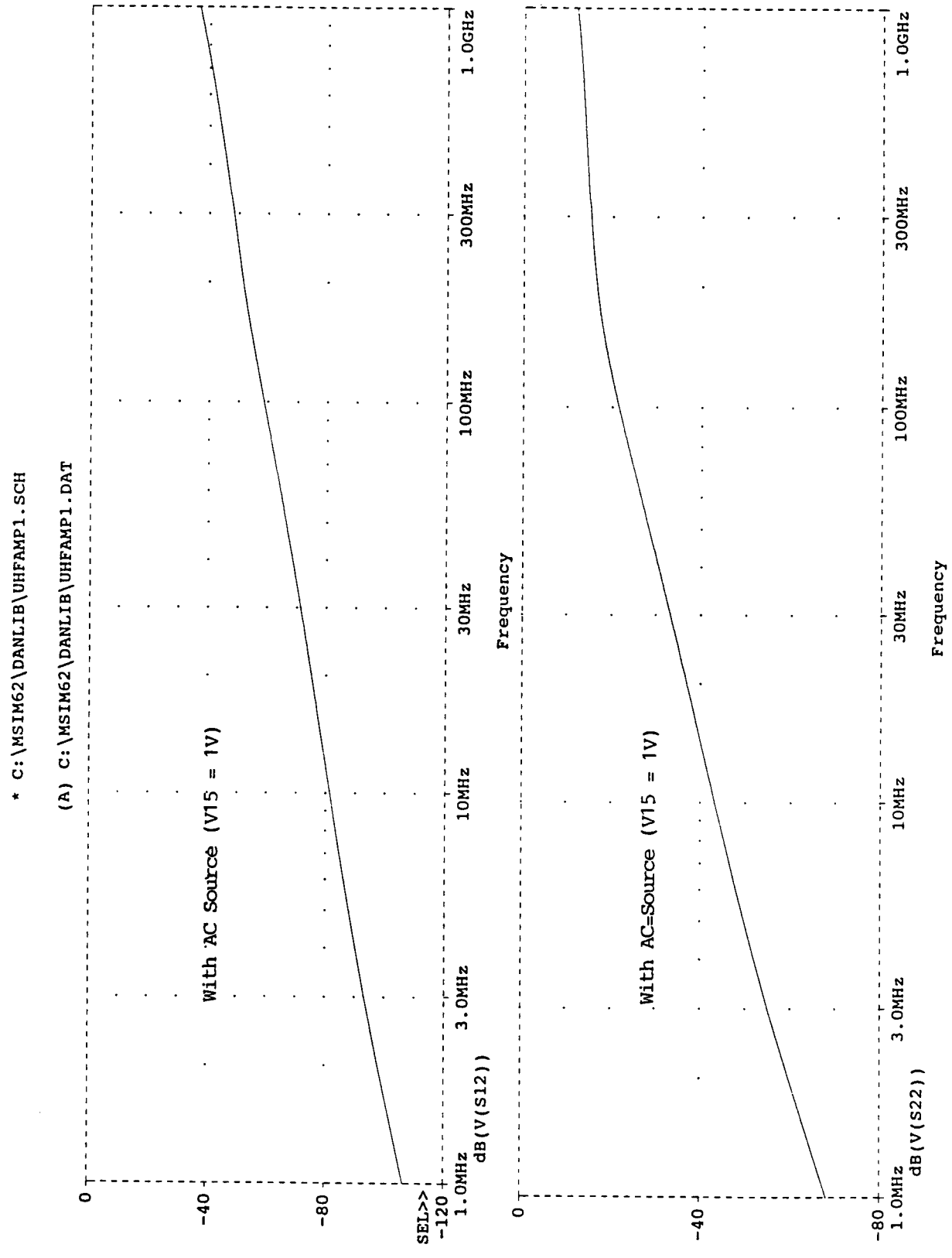


Figure 9-13 Magnitude S12 and S22 Using AC Source (V15=1V)

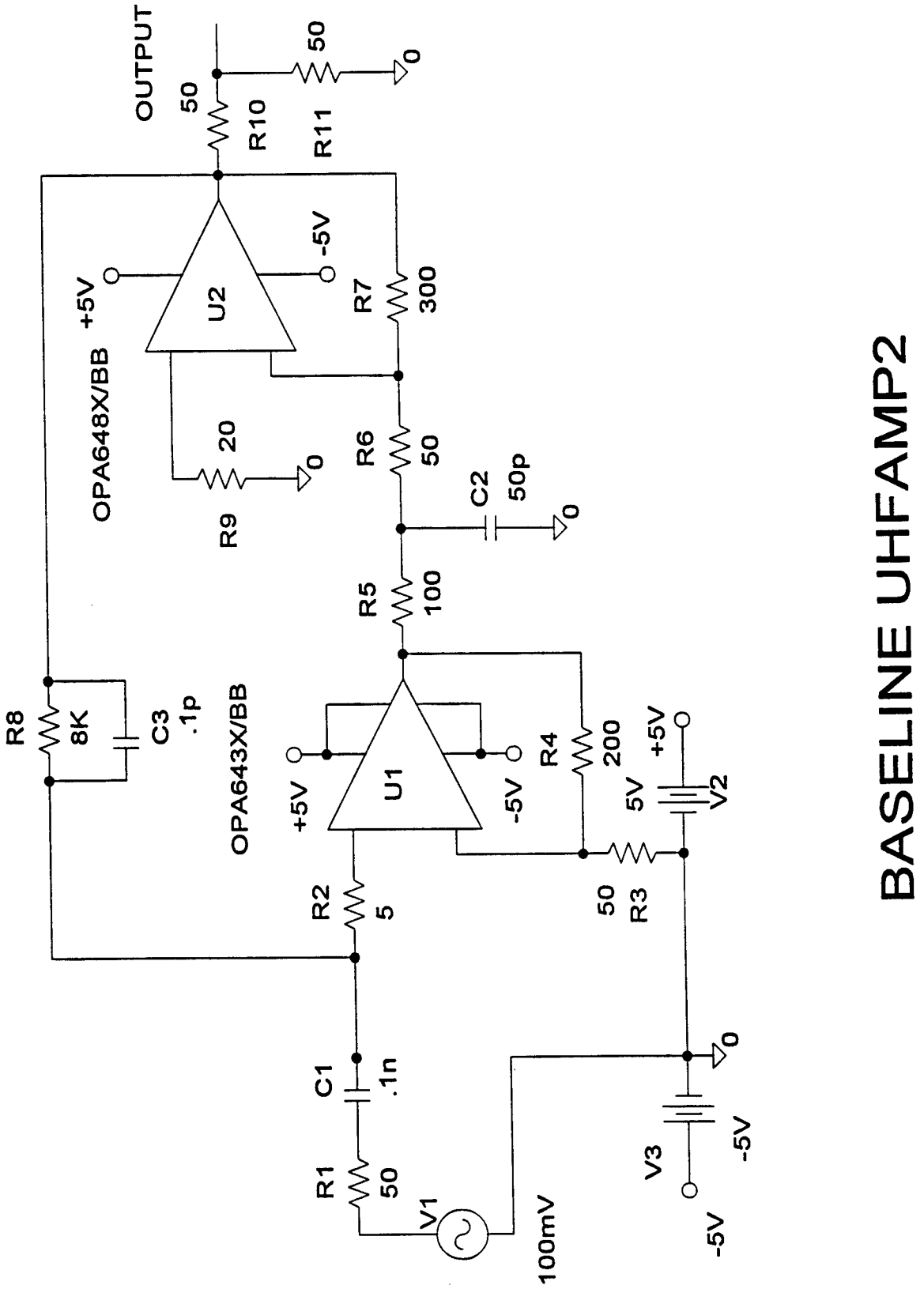


Figure 9-14 Baseline UHFAMP2

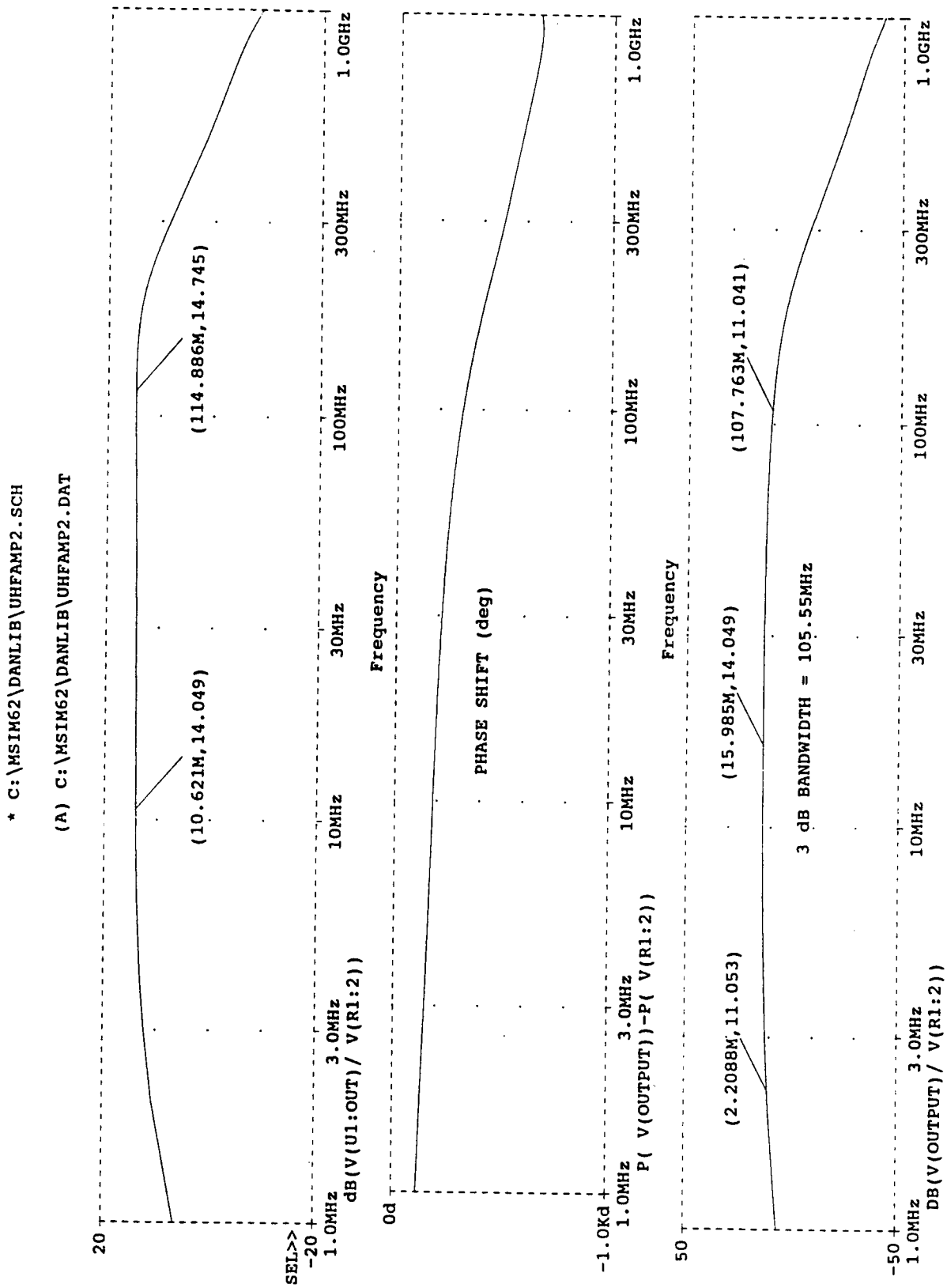
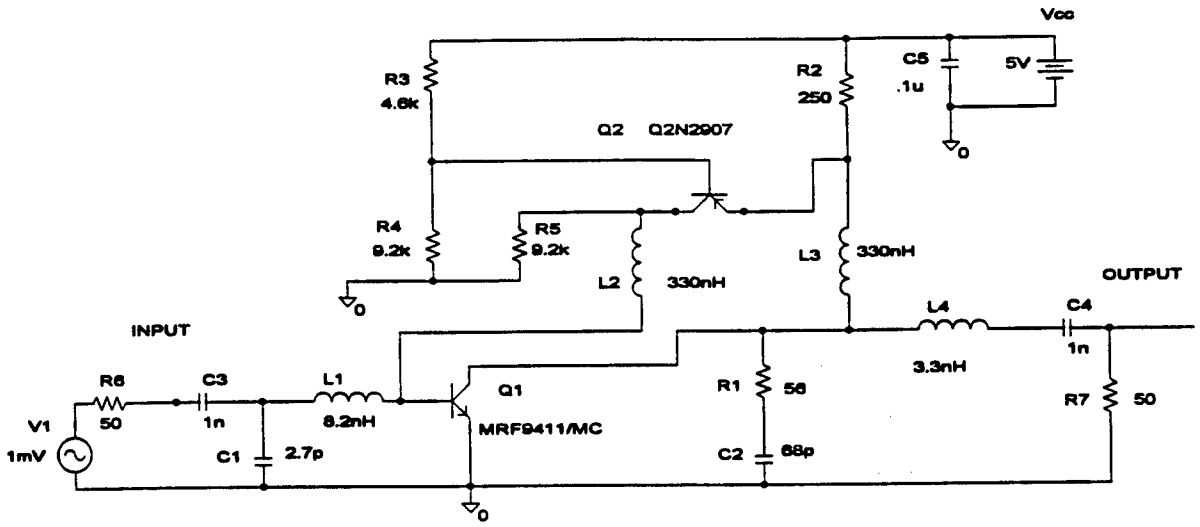


Figure 9-15 UHFAMP2: Amplifier Gain and Phase Shift



LOW NOISE UHF RF AMPLIFIER

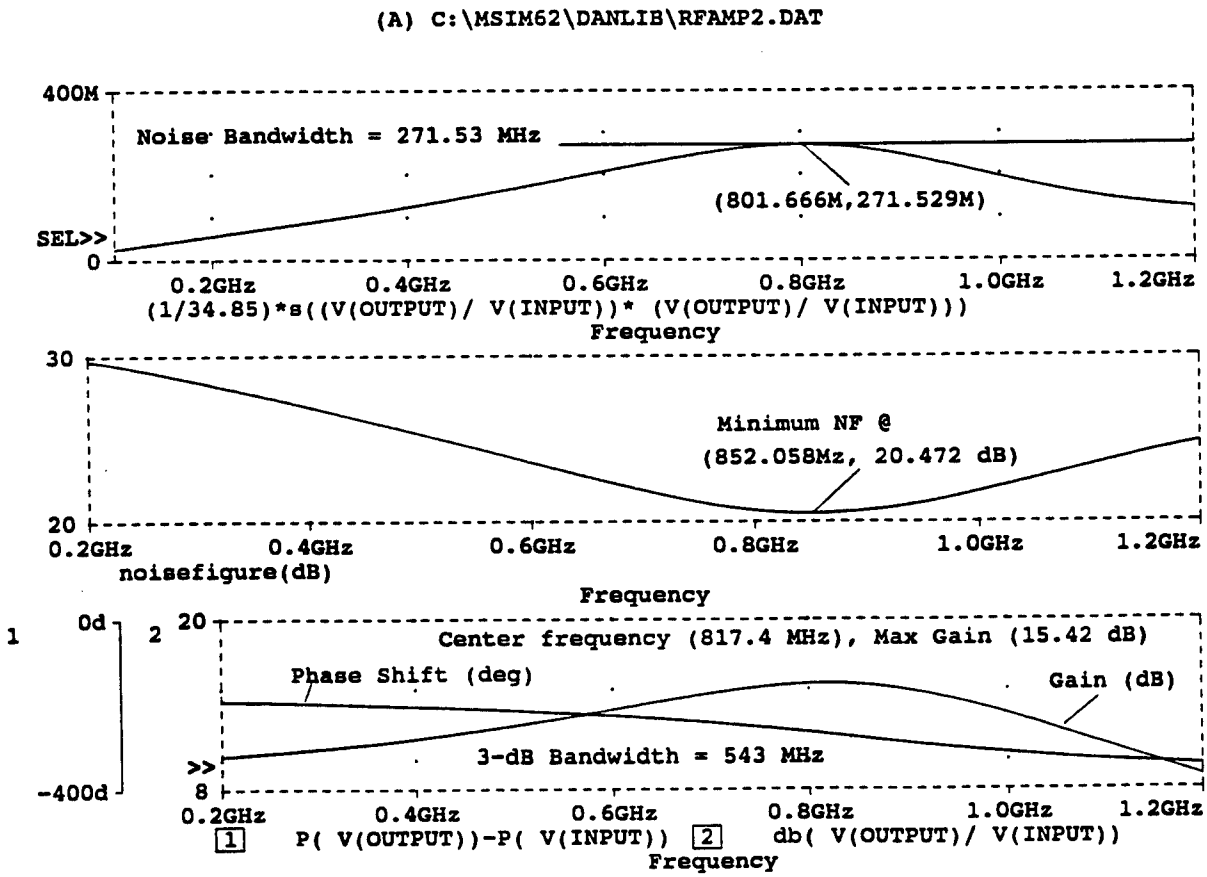


Figure 9-16 Low Noise Amplifier and Characteristics

```
* Schematics Netlist *
* LOW NOISE UHF RF AMPLIFIER (created          /DJK)*
* Modified and Tuned Often*


Q_Q1          $N_0002 $N_0001 0 MRF9411/MC
Q_Q2          $N_0004 $N_0003 $N_0005 Q2N2907
L_L1          $N_0006 $N_0001  8.2nH
L_L2          $N_0001 $N_0004  330nH
L_L3          $N_0002 $N_0005  330nH
L_L4          $N_0002 $N_0007  3.3nH
C_C1          0 $N_0006  2.7p
C_C2          0 $N_0008  68p
C_C3          INPUT $N_0006  1n
C_C4          $N_0007 OUTPUT  1n
C_C5          0 $N_0009  .1u
R_R1          $N_0008 $N_0002  56
R_R2          $N_0005 $N_0009  250
R_R3          $N_0003 $N_0009  4.6k
R_R4          0 $N_0003  9.2k
R_R5          0 $N_0004  9.2k
V_V1          $N_0010 0 DC 0V AC 1mV
R_R6          $N_0010 INPUT  50
R_R7          0 OUTPUT  50
V_V2          $N_0009 0 5V
```

Figure 9-17 Low Noise Amplifier Net List

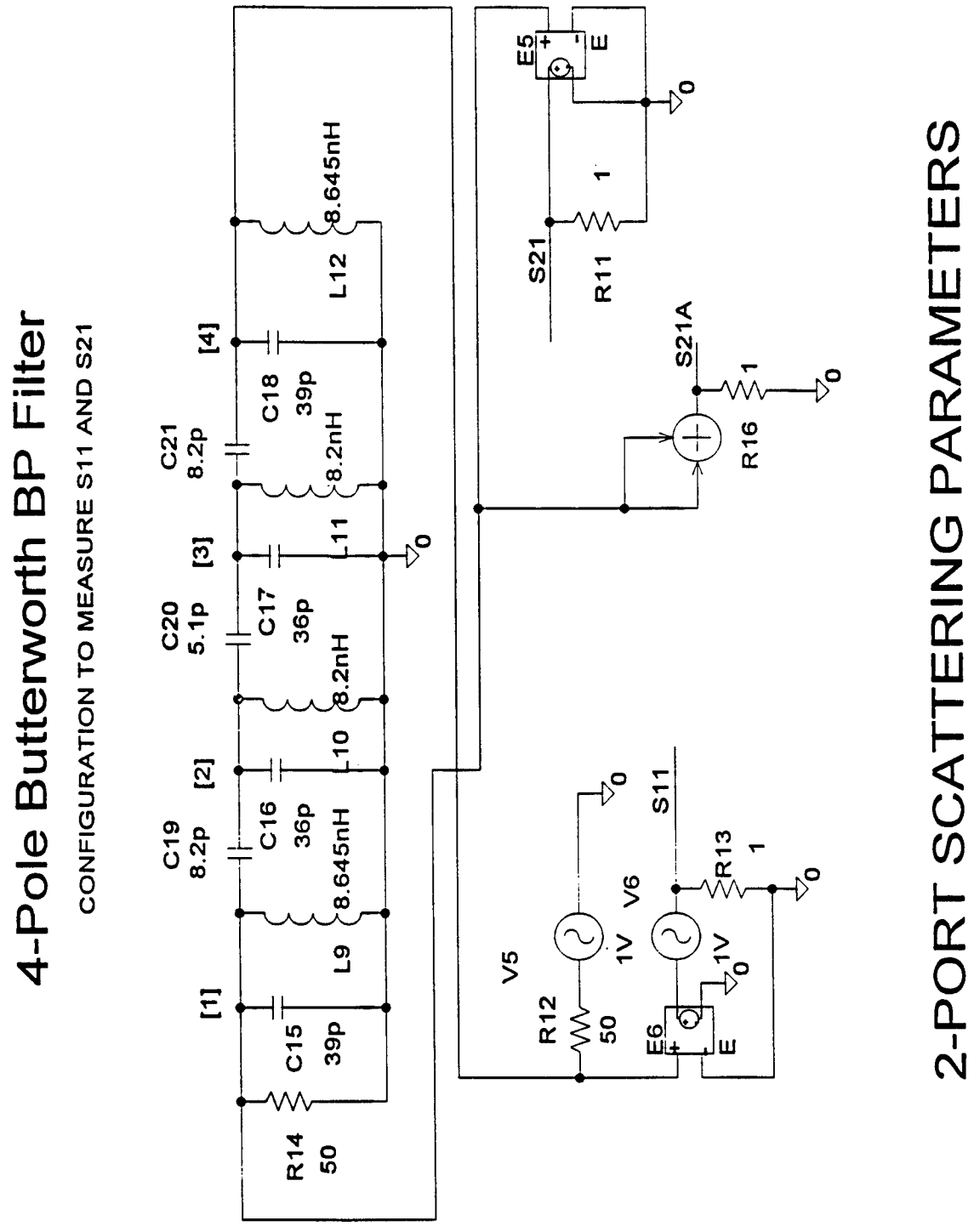


Figure 9-18 Configuration for S11 and S21 in Four Pole Butterworth BP Filter

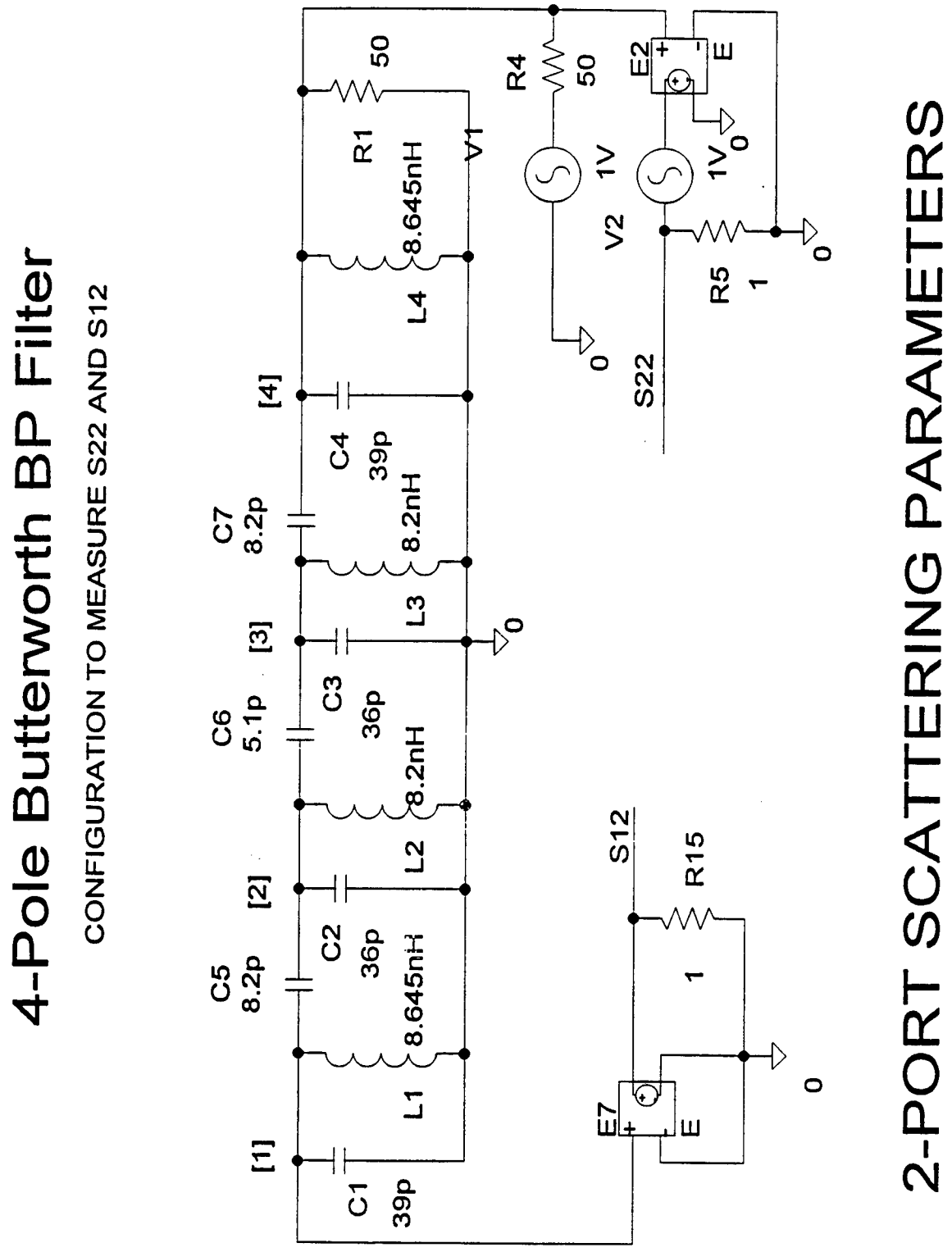


Figure 9-19 Configuration for S22 and S12 in 4-Pole Butterworth BP Filter

```
* Schematics Netlist *
* Created 12-14-95 DJKenneally*
* Modified*


C_C1          0 $N_0001  39p
C_C2          0 $N_0002  36p
C_C3          0 $N_0003  36p
C_C4          0 $N_0004  39p
C_C5          $N_0002 $N_0001  8.2p
C_C6          $N_0003 $N_0002  5.1p
C_C7          $N_0004 $N_0003  8.2p
L_L1          0 $N_0001  8.645nH
L_L2          0 $N_0002  8.2nH
L_L3          0 $N_0003  8.2nH
L_L4          0 $N_0004  8.645nH
R_R1          0 $N_0004  50
R_R4          $N_0004 $N_0005  50
R_R5          0 S22  1
E_E2          $N_0006 0 $N_0004 0 2
V_V1          $N_0005 0 DC 0V AC 1V
V_V2          $N_0006 S22 DC 0V AC 1V
E_E7          S12 0 $N_0001 0 2
R_R15          0 S12  1
C_C15          0 $N_0007  39p
C_C16          0 $N_0008  36p
C_C17          0 $N_0009  36p
C_C18          0 $N_0010  39p
C_C19          $N_0008 $N_0007  8.2p
C_C20          $N_0009 $N_0008  5.1p
C_C21          $N_0010 $N_0009  8.2p
L_L9          0 $N_0007  8.645nH
L_L10          0 $N_0008  8.2nH
L_L11          0 $N_0009  8.2nH
L_L12          0 $N_0010  8.645nH
E_E5          S21 0 $N_0007 0 2
R_R11          0 S21  1
R_R12          $N_0010 $N_0011  50
R_R13          0 S11  1
E_E6          $N_0012 0 $N_0010 0 2
V_V5          $N_0011 0 DC 0V AC 1V
V_V6          $N_0012 S11 DC 0V AC 1V
R_R14          0 $N_0007  50
E_SUM1          S21A 0 VALUE {V($N_0007)+V($N_0007)}
R_R16          0 S21A  1
```

Figure 9-20 Four Pole Butterworth BP Filter Net List

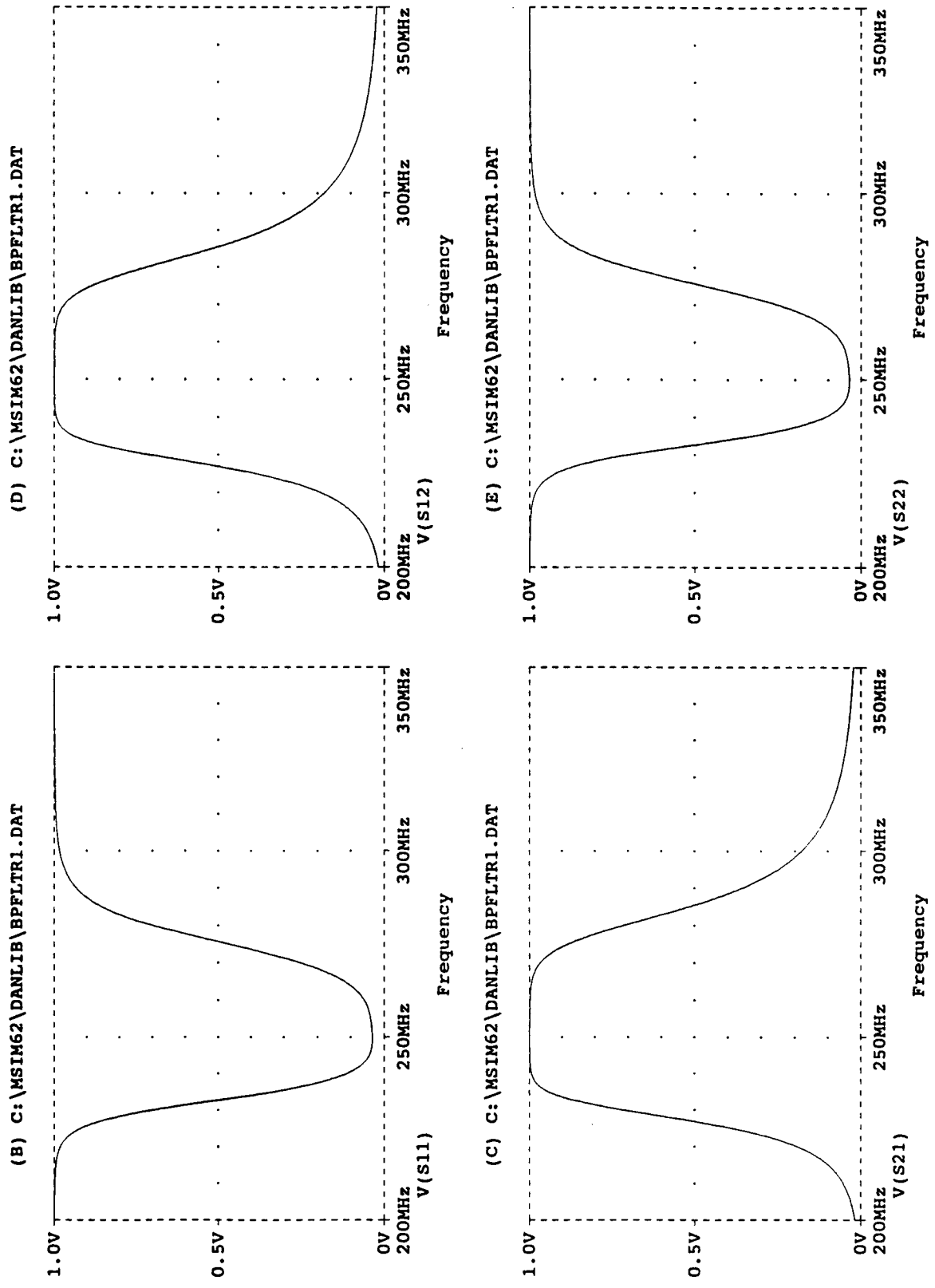


Figure 9-21 Four Pole Butterworth BP Filter S-Parameters

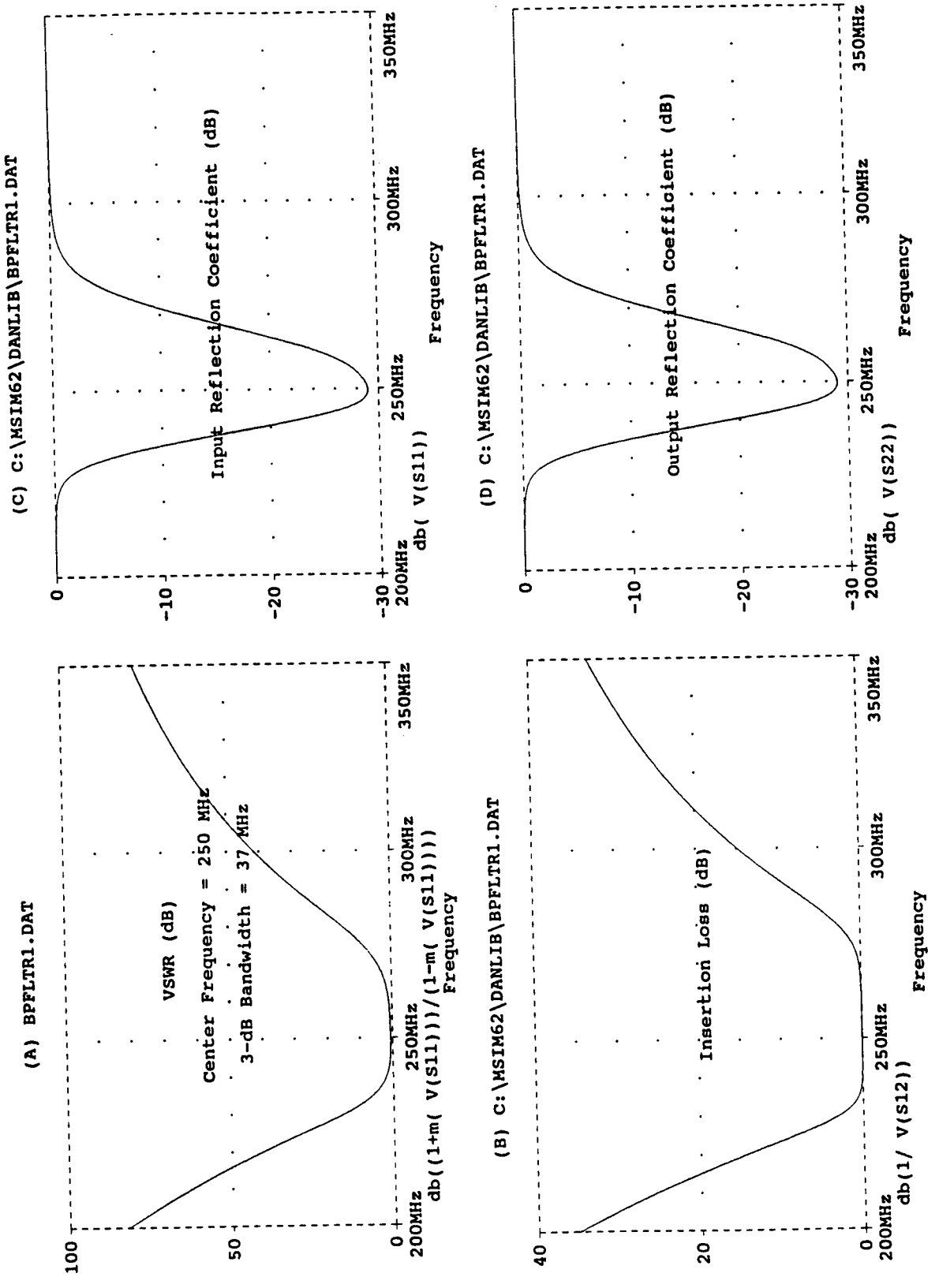


Figure 9-22 Four Pole Butterworth BP Filter: S-Parameter Derived Performance Characteristics

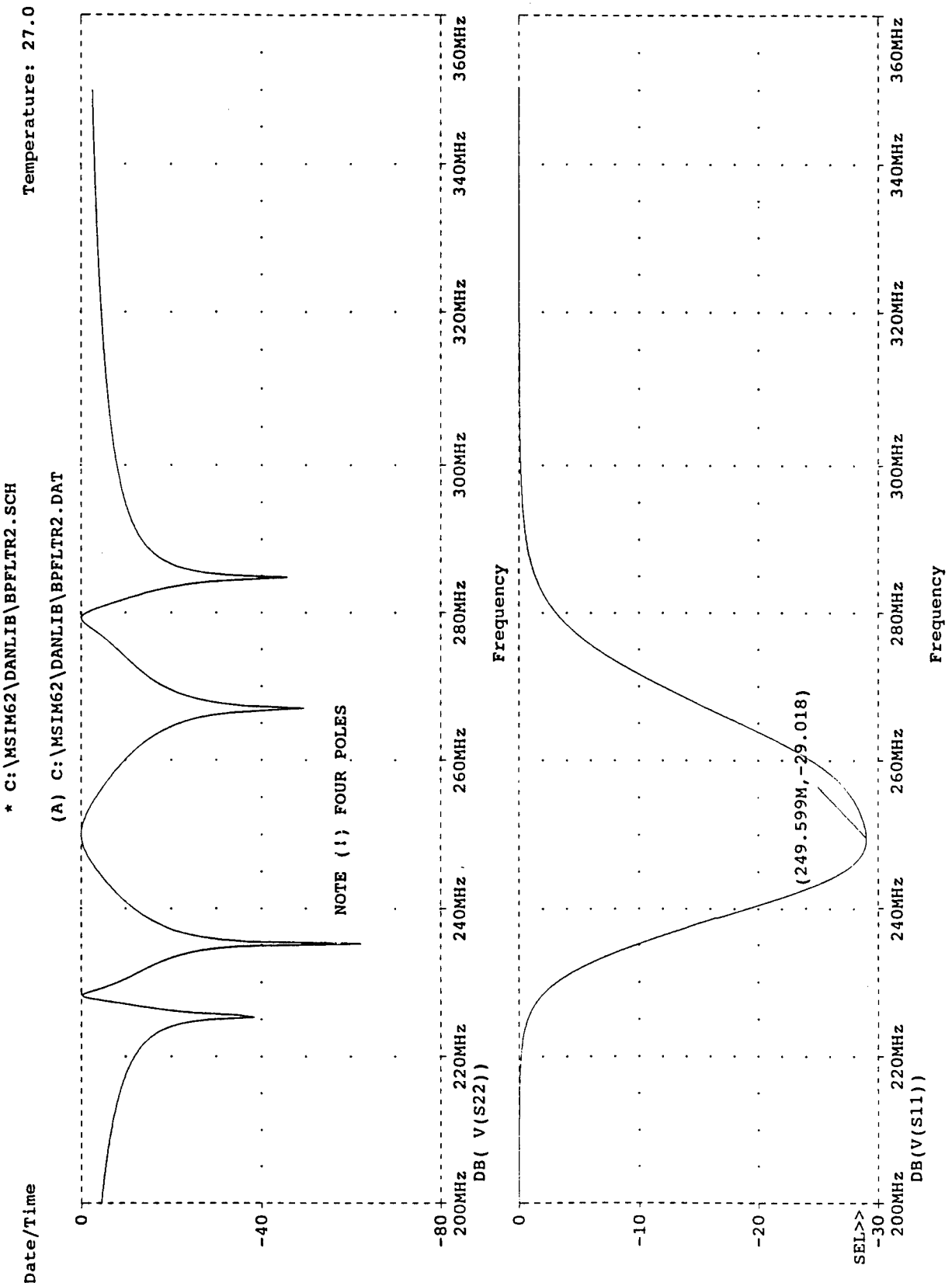


Figure 9-23 Four Pole Butterworth BP Filter: Magnitudes S11 and S22

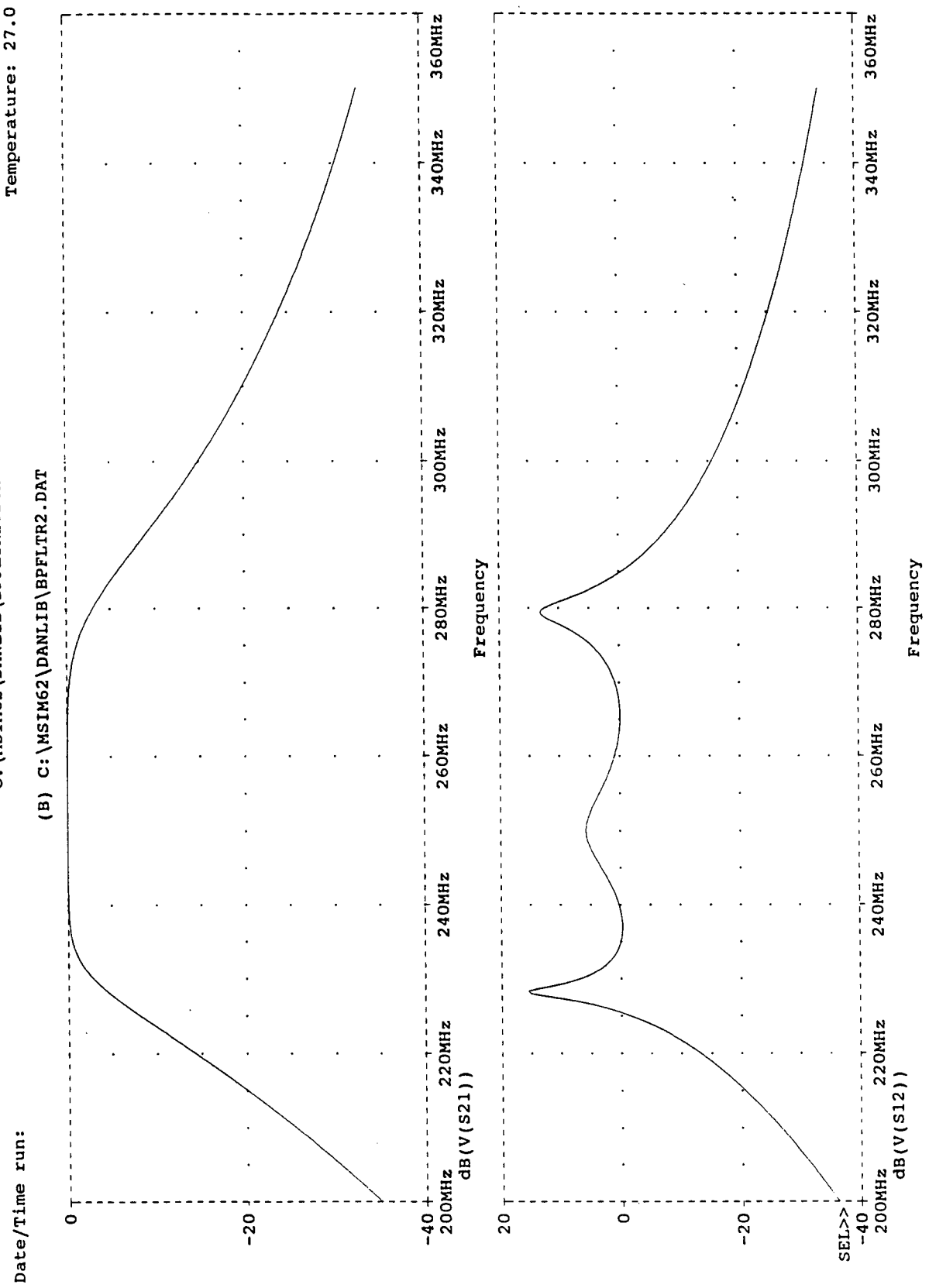


Figure 9-24 Four Pole Butterworth BP Filter: Magnitudes S12 and S21

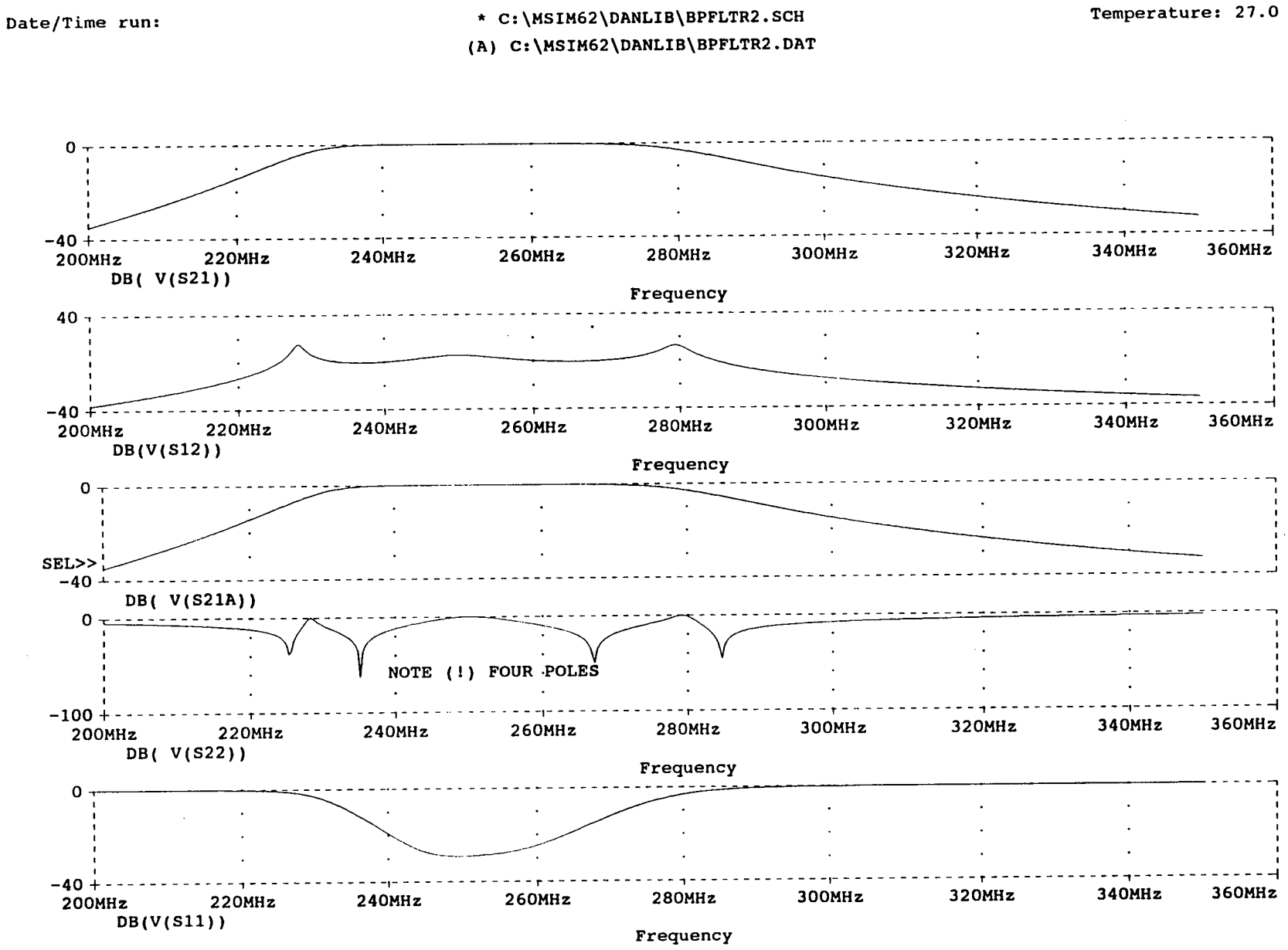


Figure 9-25 Four Pole Butterworth BP Filter: S-Parameter Related Performance

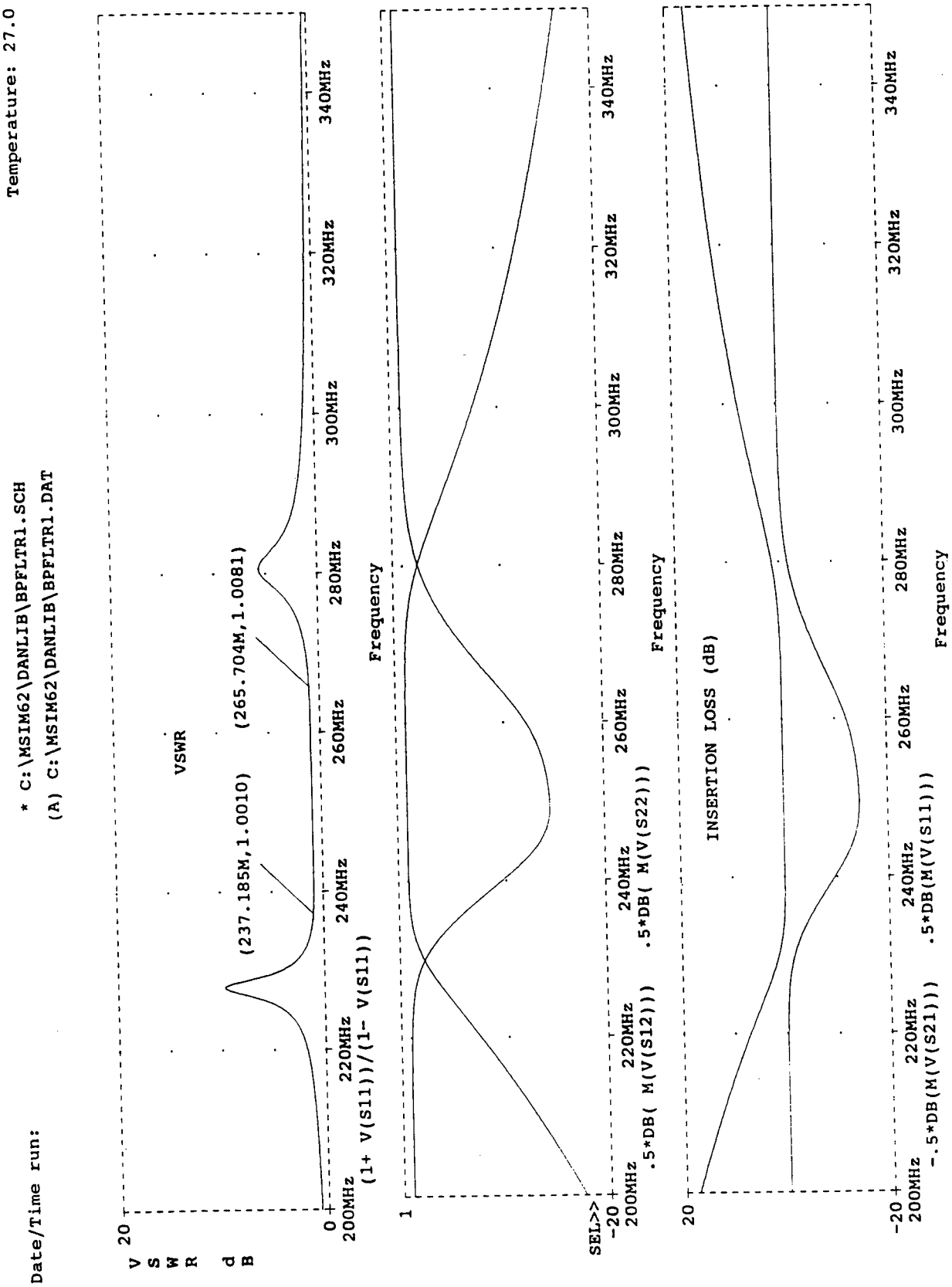


Figure 9-26 Four Pole Butterworth BP Filter: VSWR Related S-Parameters

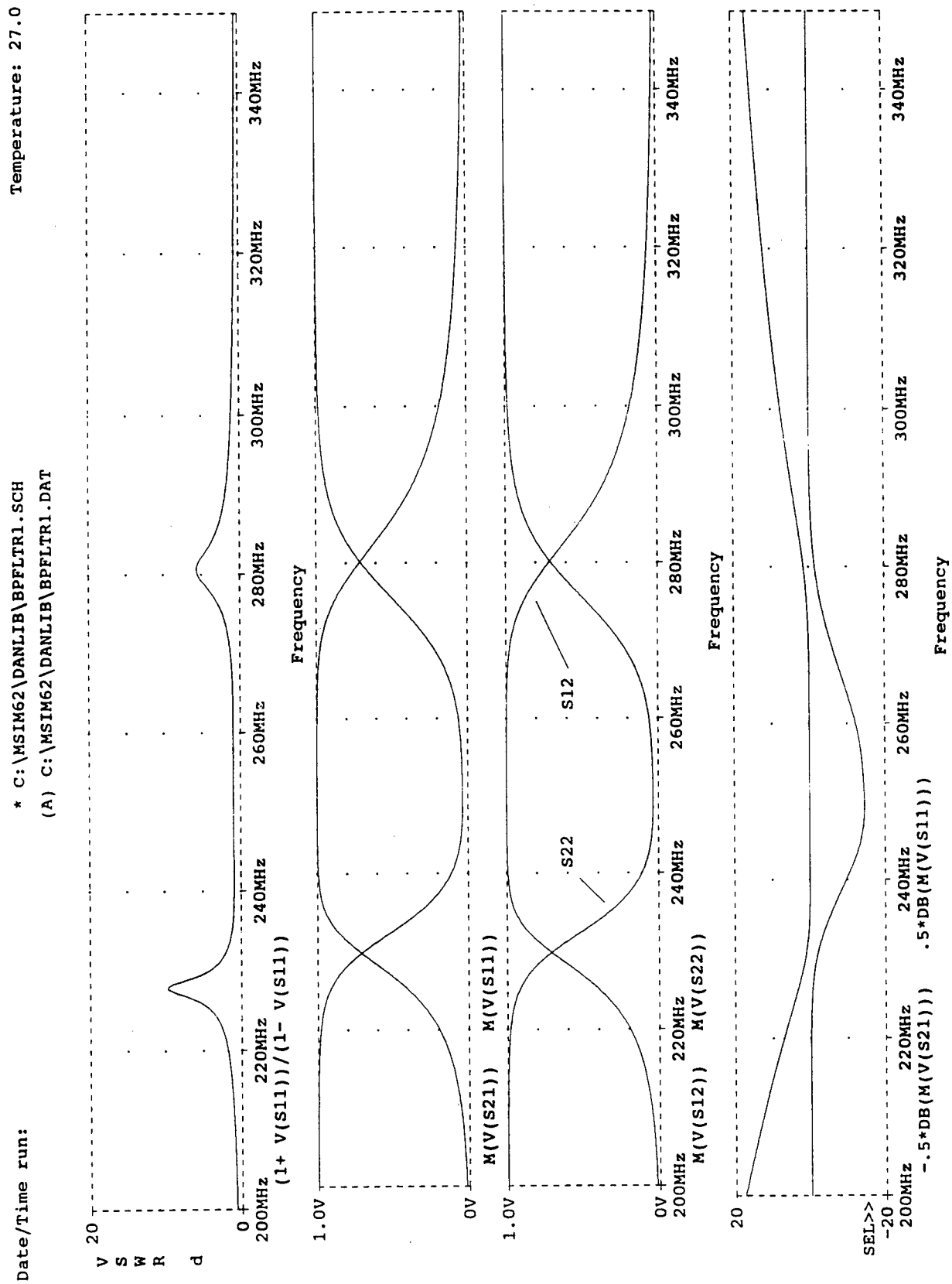


Figure 9-27 Four Pole Butterworth BP Filter: Other Related S-Parameters

10. CONCLUSIONS AND RECOMMENDATIONS

Measuring, modeling, and validating performance of Air Force electronic systems and aircraft in challenging electromagnetic environments are important initiatives in the Electromagnetic Systems Engineering Division (ERS) of the Rome Laboratory. This includes electromagnetic measurements and computer-aided modeling of system and circuit susceptibilities to EM environmental effects on both the functional and reliability performance. In this context, functional performance and reliability effects may be caused by the unintended coupling of electromagnetic fields and signals from the EM environment directly through intended (and unintended) apertures and antennas on operating systems, and by coupling onto intrasystem cabling and, subsequently, by coupling into the accessible ports of victim circuits and devices. In either case, possible resulting effects are distorted waveforms, digital upsets and latch-ups, raised noise floors, bit errors, instability, and other related symptoms of functional performance degradation and possible onset of failure.

Valid assessments of EM effects in circuits must include laboratory and analytical metrics. For example, computational metrics tailored to EM assessments require developing, adapting or redesigning time domain PSPICE macromodels (or algorithms) in order to compute and track EM responses of interest. Specifically, we need PSPICE macros in PROBE format that can determine:

a) RMS power and energy at selected ports and nodes;

b) Input impedances looking towards load or generator;

c) Power gain referred to some source or node pair;

d) Insertion Loss between selected ports or node pairs;

f) Harmonic distortion;

g) S-parameters from time domain waveform data;

h) VSWR at selected ports;

i) Noise generators and noise figure;

j) Sensitive eye pattern generators to threshold bit errors rates;

k) Signal power combiners.

In this program, a suite of macromodels that enhance circuit assessments of EM effects was successfully developed and tested. Thevenin and Norton source configurations were used as equivalent circuits to model coupling of intrusive EM fields into victim device ports. Both digital and linear ICs were used as victims to benchmark performance of the candidate macros. Three ICs of representative families, however, were specifically selected for bench marking because they are used extensively in current and planned Air Force Systems. In addition, other contemporary linear ICs and OpAmp's were used in various circuit configurations to demonstrate use of (EM) assessment macromodels developed here.

These macromodels (i.e., macros or sub-circuits) were used to "measure" circuit responses at output and other ports when any other (arbitrary) ports were cw driven by EM sources. Specific macros were designed that measure average power, peak power, scattering parameters, digital eye patterns, digital bit error thresholds, noise figure, and other EM metrics of degradation. Demonstrations of these macros using the PSPICE simulator and selected ICs, under a variety of EM fields coupling scenarios, suggest convincing evidence that macromodels developed in this program perform as intended. A shortfall in these demonstrations is that they were limited in frequency range due to program time constraints. While the macromodels presented in this report were tailored for a PSPICE (Version 6.2) circuit simulator, it is felt that they are general enough in format and in application to be easily adapted to most other contemporary simulators.

From performance data on EM assessment macros developed and demonstrated here, we conclude that these EM macromodels in PSPICE provide useful sub-circuits, analog behavioral models, and related algorithms to enable assessments of EM environmental effects in ICs. Among these are circuit level macros that can:

a) combine desired signal power with EM effects power,

b) measure average, rms, and peak power levels,

c) simulate and shape noise spectra,

d) measure noise spectral densities and noise figure,

e) generate eye patterns to determine digital upset thresholds,

f) measure S-parameters of passive and active devices, and

g) measure input impedance, VSWR, insertion loss, and gain.

It is recommended Rome Laboratory continue this and related circuit CAD simulation work to develop an entire software suite of EM assessment tools and macros in a single "CAD package", and to specifically focus on the following macromodeling and related initiatives:

a) widen the macro frequency range of interest up to 6 GHz or higher,

b) develop and verify realistic EM field coupling models,

c) include IC gain compression and expansion (EM)effects,

d) refine and exploit eye patterns as EM effects diagnostic tools,

e) develop noise modeling as an EM effects diagnostic tool,

f) include an electrostatic discharge model in the suite of EM assessment tools.

In addition to the CAD work cited above, it is recommended that Rome Laboratory conduct related measurements programs to demonstrate and validate all or some of the EM assessment macros developed in this effort. Of special interest, are the Wilkinson Power Combiner and the Eye Pattern Generator macros. Because of their obvious novelty and demonstrated utility for performing more sensitive and accurate assessments of EM effects in ICs, it is strongly recommended they be given priority in any new Rome Laboratory initiatives, either CAD modeling or experimental. Since these new macros have good technical and commercial merit as new candidate products for technology transfer to civilian use, considertions of such technology transfer are also recommended.

11. BIBLIOGRAPHY

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*U.S. GOVERNMENT PRINTING OFFICE: 1998-610-130-61135

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